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Design And Implementations Of LUT Based Approximate Adders For Fpgas

Murthy C, Dr. Madhusudhan K N,

M tech student, Assistant Professor
Department of Electronics and Communication Engineering,
BMS college of Engineering, Bengaluru, India

Abstract: In this project, high speed, power efficient adders were designed at the cost of accuracy. The proposed design fixes the LSP of the implementation which will truncate half of the adder area and there by reduces the power consumption along with that the propagation delay can be minimized to half of it and further can be optimized by inner stage input-output pipelining to the parallel prefix adder to increase its speed. The MSP utilizes the accurate computation utilizes LUT's as resources and reduces the parameters by slightly increasing the error of approximate adders. Compared to the existing LEADx and APEx now our suggested adder is efficient in parameters and the design and simulation and effectiveness of the proposed method is synthesized using Xilinx Vivado.

Index Terms - Approximate computing, approximate adder, FPGA, low speed, low power, LUT, Parallel prefix adders

I. INTRODUCTION

For error-tolerant applications like video coding, approximate computing is a novel design strategy that compromises accuracy for performance, size, and/or power consumption. The nature of video compression is error-tolerant because the output must only be at a quality that allows for a satisfactory user experience. Approximate computing hence has a great deal of potential to enhance hardware implementations' performance, area, and/or power consumption. Because of their quick time to market, increased flexibility, and run-time re-configurability, FPGAs are a great platform for many different applications, ranging from high-performance computing systems to small-scale embedded devices. In contrast to their ASIC counterparts, FPGA-based systems usually consume more power and/or energy, even though they support specialized hardware accelerators and co-processors. Thus, in addition to using conventional energy optimization methods, there is necessary to investigate novel approaches to energy-efficient computation that are specific to FPGA-based devices. The Approximate Computing paradigm is one such appealing trend that is resurfacing as a result of Dennard scaling, the collapse of Moore's law, and the growing desire for high-performance and energy efficiency. In order to make notable improvements in critical path delay, area, power, and/or energy consumption, approximate computing trades the accuracy and precision of intermediate or final computations. Applications that have intrinsic application resilience that is, the capacity to generate workable output even when portions of their computations are erroneous due to approximations benefit from this trade-off. This property is demonstrated by a wide range of applications in the recognition, mining, and synthesis areas, such as image and video processing, data mining, machine learning, etc. From logic and architectures at the hardware layer to compilers and programming languages at the software layer, existing approximation computing techniques and principles can be applied to different stages of the computing stack. Approximations at the hardware and software layers have been the subject of much research. Both functional approximation and voltage over-scaling are the two main approximate computing parameters used at the hardware level.

II. PREVIOUS RESEARCH ON LUTs BASED APPROXIMATE ADDERS FOR FPGAs.

This work aims at improving the performance of portable multimedia devices by applying approximate computation methods that give reduced power consumption precedence over perfect numerical precision. These gadgets are frequently used for multimedia processing, where users are willing to put up with small output errors in exchange for substantial energy savings. Historically, this field of study has usually depended on voltage over scaling and different algorithmic or architectural techniques to reduce mistakes. But by lowering logic complexity at the transistor level specifically, by using approximation adder cells, which provide shorter critical pathways and reduced complexity this work presents a fresh strategy. Using these approximation adders, the suggested approach builds multi-bit arithmetic units and shows how successful it is in real-world applications such as picture and video compression methods. Additionally, mathematical models are created to measure the power consumption and accuracy trade-offs present in various approximation methods. The study also highlights their use in discrete cosine transforms and finite impulse response filters, among other digital signal processing architectures, showing significant power savings up to 69% when compared to conventional implementations that employ accurate adders. Additionally, the study presents a novel Internal-Self-Healing (ISH) method intended to enhance current self-healing strategies in approximation computing. As opposed to traditional techniques, which necessitate paired, parallel modules in multiples of two, ISH permits internal error correction in asymmetric or irregular data paths without imposing such limitations. This development is especially helpful for applications where error cancellation procedures can greatly improve overall performance, such as approximation multiply-accumulate (xMAC) processes. In particular, for complicated applications like radio-astronomy calibration processing, the study's unique 2 × 2 approximate multiplier design solves overflow difficulties and shows better effectiveness over conventional error-restricted techniques. Regarding FPGA-based computing, the paper recommends optimized approximation parts designed for FPGA designs with LUTs. To create efficient designs, the method takes propagation delay and LUT count into account in addition to gate count and logic levels. We synthesize and test a variety of approximatively multipliers (8-bit and 16-bit) and adders (up to 64-bit) that outperform the state-of-the-art in terms of worst-case error, LUT utilization, and performance metrics. The goal of making these designs publicly available as Verilog netlists is to spur additional study and advancement in the field of FPGA-based approximation computing. The paper also discusses the drawbacks of current FPGA softcore multiplier IP cores that are tailored for particular uses like analyzing images and videos. It suggests low-latency, generalized area-optimized architectures that take advantage of quick carry chains and LUT structures found in FPGA architecture. In comparison to vendor-provided solutions like as the Xilinx LogiCORE IP, the proposed designs both unsigned and signed show notable decreases in LUT utilization and critical path delay with negligible loss in output accuracy. These gains are verified by real-world accelerator application implementations, which increase both area efficiency and performance. The creation of the Majority Approximation Adder (MAA), an FPGA-based approximation adder that combines exact and approximate computing components to produce lower error rates than advanced approximate adders, is a significant contribution of this research. Compared to current FPGA-based alternatives, MAA shows a significantly lower mean error distance (MED) through Monte-Carlo simulations, with less power consumption and space consumption. This design philosophy is versatile and applicable to various computing architectures, as demonstrated by its application in order to ensure worst-case error guarantees, the study concludes with a systematic approach to approximation system design that makes use of Look-Up Table (LUT)-based netlist transformations supplemented by property checking techniques like SAT. With this rigorous strategy, designers may take into account elements like layout size and computing efficiency and balance output quality with error tolerance across a variety of design scenarios. In conclusion, the study's research highlights the increasing importance of approximation computing techniques for signal processing and multimedia applications that aim to maximize power efficiency. The study offers significant insights and useful solutions to improving the effectiveness of integrated systems through approximation techniques by creatively addressing problems in transistor level complexity reduction, internal error correction mechanisms, FPGA optimization, and systematic approximation design.th FPGA and ASIC implementations.

III. CONCLUSION AND FUTURE WORK

This work focuses on using approximate computing methods, which place power savings ahead of exact numerical precision, to increase the efficiency of digital systems. The study presents a number of innovative techniques and strategies in a number of digital hardware design disciplines. First, the work suggests a generalized architectural template for approximate adders called the Optimal Lower Part Constant-OR Adder (OLOCA). Comparing OLOCA to earlier best-in-class architectures, error and hardware cost measures show notable gains. For example, compared to current Lower OR Adder (LOA) techniques, a 16-bit version employing OLOCA yields a 58% reduction in Mean Squared Error (MSE) and a 13.8% decrease in Average Delay Power (ADP). Additionally, using LUT6 resources, the research presents a technique for creating effective approximate adders customized for Xilinx FPGAs. Significant savings are achieved in area (34%), power consumption (41%), and delay (38%), indicating the suitability of this method for FPGA-based applications like image processing. Furthermore, a Type II Error-Tolerant Adder (ETAII) is suggested, highlighting notable power reductions and enhanced functionality in comparison to traditional adders. Applications in DSP systems for mobile devices, where stringent accuracy requirements are subordinated to high-speed performance and low power consumption, are best suited for ETAII. The research also introduces the HOAANED approximation adder, which is intended for use in both FPGA and ASIC implementations. Comparative analyses demonstrate how well HOAANED optimizes crucial path latency, power consumption, and resource use. HOAANED's capacity to improve Peak Signal-to-Noise Ratio (PSNR) in reconstructed images while lowering delay by 11% and power consumption by 10% in FPGA implementations is demonstrated by real-world applications in digital image processing. Moreover, the study goes into hardware video coding implementations and specifically suggests effective approximation methods for HEVC intra prediction. When compared to traditional methods, these strategies greatly reduce hardware area and memory needs while achieving small loss in PSNR and bitrate. The work offers effective designs for FPGA environments in the field of approximate multipliers, surpassing earlier studies in terms of electrical performance (delay, power, area), Power-Delay Product (PDP), and Power-Delay-Area Product (PDAP). The multipliers exhibit better latency in comparison to DSP-based multipliers and are assessed for their appropriateness in high-performance, low-power applications like image processing. The study also presents new Internal-Self-Healing (ISH) techniques for roughly Multiply-Accumulate (MAC) accelerators. By eliminating the requirement for paired computing units to enable error cancellation inside approximate circuits, ISH increases the applicability of approximate computing to irregular data paths and facilitates more successful quality-efficiency trade-offs. The article concludes with a discussion of approximation circuit synthesis that is iteratively optimized for LUT-based technologies. This systematic technique investigates ASIC design trade-offs and guarantees controlled propagation latency. Using other technologies, improving the approximate circuit designs' efficiency and versatility. All things considered, these developments highlight the increasing significance of approximation computing in striking a balance between computational efficiency and allowable degrees of inaccuracy, especially in fields where performance, power consumption, and area utilization are crucial considerations. The research findings provide important insights for future improvements in approximate computing approaches and are backed by mathematical analyses, experimental validations, and useful applications across a range of digital system designs.

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