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Design And Layout Implementation Of Miller Compensated Two Stage Op-Amp

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Abstract: This project focuses on designing and implementing a Miller compensated two-stage operational amplifier (Op-amp). Through comprehensive literature review and SPICE simulation, the Op-Amp's performance will be optimized. Expected outcomes include a fully characterized Op-Amp circuit and finalized layout design. This project aims to deepen understanding of analog circuit design principles, testing and its applications. It provides valuable hands-on experience in integrated circuit design**.**

Index Terms - Introduction, Components, Literature Review, Methodology, Key-Insight, Design Methodology, Design, Conclusion, References.

I. INTRODUCTION:

Very Large-Scale Integration (VLSI) and Analog Integrated Circuit (IC) design represent important fields within Electronics engineering, encompassing the creation and optimization of complex electronic systems on semiconductor substrates. VLSI involves the integration of millions (or even billions) of transistors and other electronic components onto a single chip, enabling the development of advanced digital and Analog circuits with high performance, low power consumption, and small form factors. Analog IC design, a subset of VLSI, focuses specifically on the design of Analog circuits, which are essential for processing real-world signals such as audio, video, and sensor data. Due to their widespread use and importance in modern electronics, the design and optimization of Op-amps are of high significance in both VLSI and Analog IC design. In the context of this project proposal, the implementation of a Miller compensated two-stage Op-amp is an important for us within the realm of Analog IC design. By delving into the design and layout implementation of this fundamental circuit component, the project aims to deepen understanding of Analog circuit design principles and also provide hands-on experience in VLSI methodologies and techniques. Through this project, we want to explore the relationship between theory and practice, contributing to the advancement of our understanding of Analog integrated circuitry and VLSI.

II. PROJECT KEY COMPONENTS:

1. *Design and Analysis*: Develop and optimize the design of the Miller compensated two-stage Op-Amp. Analyse the Op-amp performance in terms of gain, bandwidth, and stability, ensuring compliance with design specifications.
2. *Schematics*: Create detailed schematic diagrams of the Op-amp circuit, including all necessary components and connections, based on the optimized design obtained from the analysis.
3. *Layout*: Convert the schematic design into a physical layout using industry-standard layout design tools like Cadence. Optimize the layout for minimal parasitic effects and adherence to design rules (DRC) and constraints.
4. *Bench Testing*: Conduct bench testing to evaluate its performance under real-world operating conditions and compare it with an Ideal Op-amp behaviour. Measure key performance parameters such as Gain bandwidth, input/output impedance, Slew-Rate, Noise, CMRR and distortion.

5. *Validation*: Validate the performance of the fabricated Op-Amp through comparison with simulated results and theoretical expectations. Identify any deviations and tune the design to achieve desired performance.

III. METHODOLOGY:

1. *Requirements Analysis*: Identify the operational requirements such as gain, bandwidth, and power consumption.
2. *Schematic Design*: Create the schematic diagram of the two-stage operational amplifier, including the differential input stage, gain stage, and compensation network.
3. *Transistor Sizing*: Determine the sizes of transistors in each stage based on desired performance criteria and technology specifications.
4. *Biasing Design*: Design the biasing circuits to establish operation points for all transistors within the saturation region.
5. *Compensation Network Design*: Design the Miller compensation network to ensure stability and adequate phase margin across the desired bandwidth.
6. *Simulation and Analysis*: Use simulation tools like Cadence Virtuosos to verify the performance of the amplifier, analyzing key metrics such as gain, bandwidth, phase margin, and transient response.
7. *Layout Design*: Implement the circuit layout on the silicon substrate, considering layout guidelines, parasitic elements, and DRC.
8. *Optimization*: Iterate on the design, making adjustments to optimize performance metrics such as gain-bandwidth product, power consumption, and noise figure.

IV. KEY INSIGHTS:

1. **Hesham Omran lecture on the gm-Id design methodology demystified**
   1. **Contribution**: Focuses on the application of the gm/Id methodology in designing two-stage op-amps.
   2. **Key Points**: Demonstrates the effectiveness of gm/Id in optimizing design parameters for enhanced performance.
2. **Reda, Ahmed & Wahba, Ahmed (2010)**. CMOS two-stage amplifier design approach
   1. **Contribution**: Provides a comprehensive overview of design approaches for CMOS two-stage amplifiers.
   2. **Key Points**: Discusses various design strategies and their implications on amplifier performance, offering a broad perspective on design choices.

V. CIRCUIT DIAGRAM:

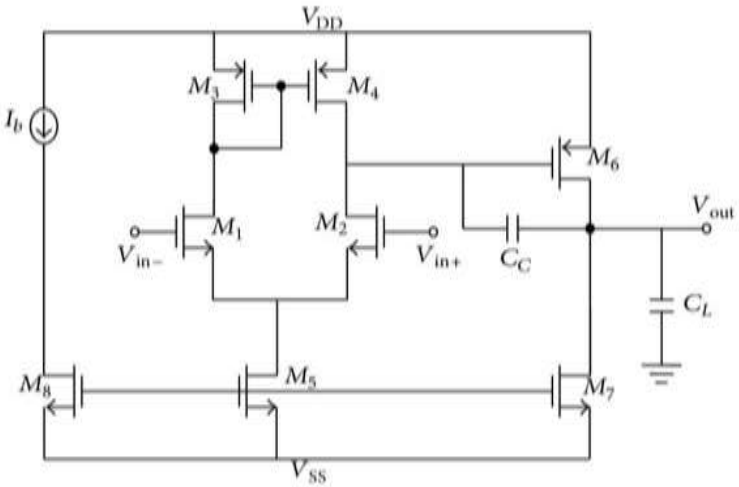

Fig1: Circuit Diagram of Miller Compensated Two Stage Op-Amp

VI. DESIGN METHODOLOGY:

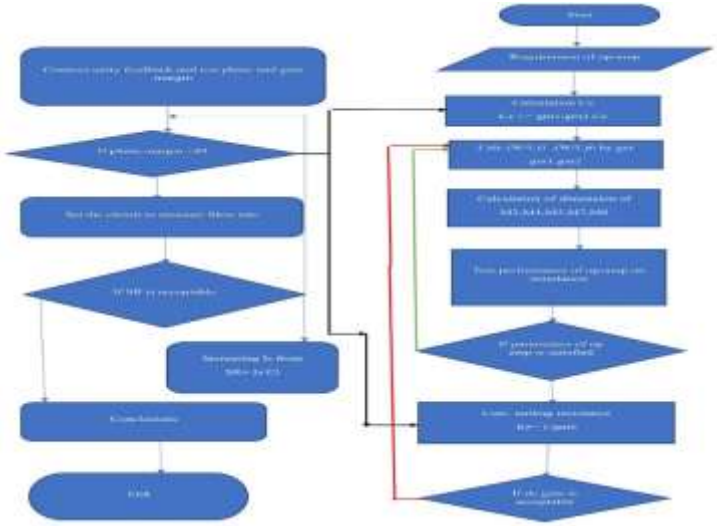

Fig2: Design Methodology of Op-amp

Specifications:

DC Gain: 60dB
Phase Margin: 60 degrees
CMRR: 50dB
PDK: 90nm(gpdk90)
Unity Gain Bandwidth: 5MHz
Slew Rate: 10V/µsec.

VII. DESIGN OF OP-AMP:

This is an Operational Amplifier so all the MOSFETs operate in saturation region to provide maximum Gain.

1.THE ASPECT RATIO OF DIFFERENTIAL PAIR

- gm1 is the one that contributes to the gain and bandwidth of the error amplifier so
- ***gm1,2 = 2*pi*(GBW*CL)***
- ***(W/L)1,2 =gm1^2/(µnCox*2I1)***

2.THE ASPECT RATIO OF CURRENT MIRROR:

- Before finding the W/L3,4 we need to find the Vt max of current mirrors and Vtnmax, Vtnmin of Differential pairs.
- For Simplicity I've used the mosfet nfet_01v8_lvt and pfet_01v8_lvt whose Vt doesn't change much unlike nfet_01v8 and pfet_01v8.
- ***Vsg3 = Vdd - Icmr(+) + Vtn1min***
- ***(W/L)3,4 = 2I3/(µpCox(Vsg3-Vtpmax)^2)***

3.THE ASPECT RATIO OF BIASING MOSFETS:

- ***(W/L)5,6 = 2I5/(µpCox(Vdsat5^2))***

4.THE ASPECT RATIO OF SECOND STAGE:

- The Aspect Ratio of M7can be calculated as:
- ***I6=(W/L)6*I4(W/L)4***
- ***(W/L)6=I6*(W/L)5/I5***

6.THE ASPECT RATIO OF M8 CAN BE CALCULATED AS:

- ***gm6=10gm1***
- ***gm4=sqrt(2I4*µp*Cox(W/L)4)***
- ***(W/L)6=gm6*(W/L)4/gm4***

VIII. ASPECT RATIO OF MOSFETS:

M1, M2	**1.2**
M3, M4	**1.5**
M5, M8	**5.2**
M6	**16**
M7	**28**

IX. SCHEMATICS:

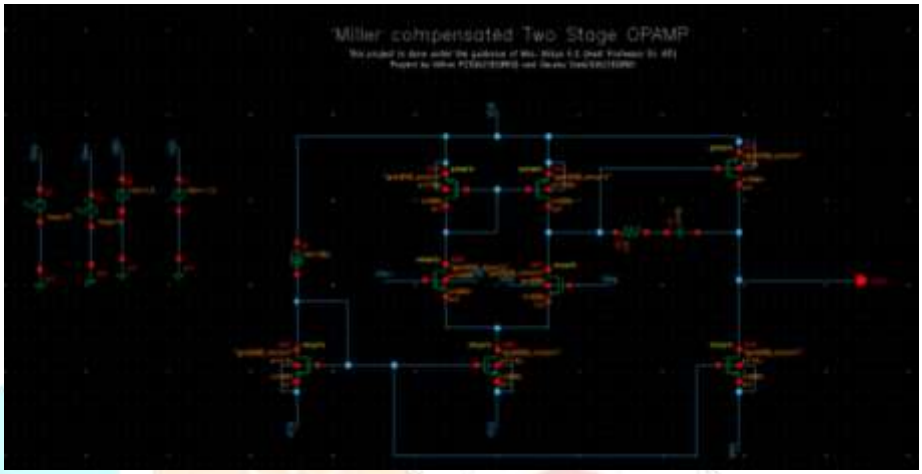

Fig3: Miller compensated Op-Amp schematic in Cadence Virtuoso

X. PLOTS:

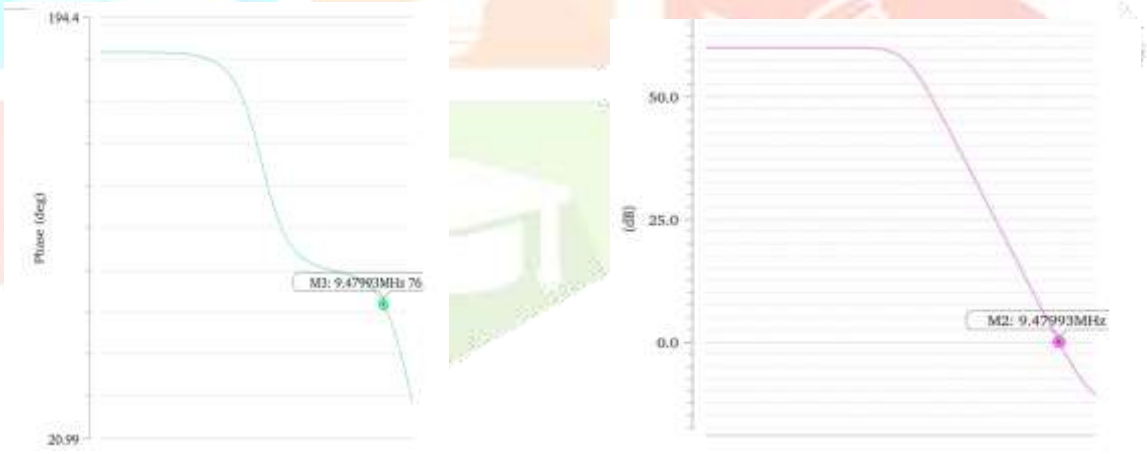

Fig4: AC Response Two stage OpAmp

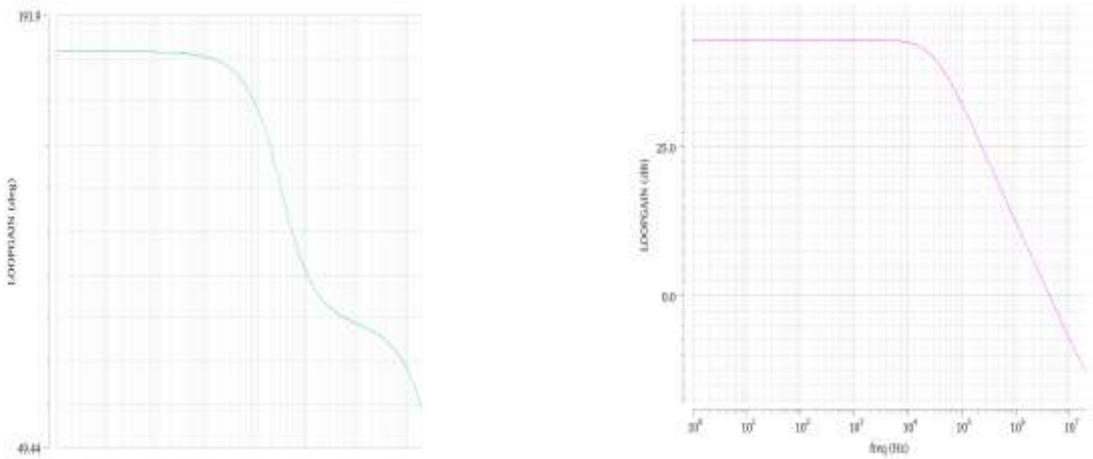

Fig5: Stb Analysis Two stage OpAmp

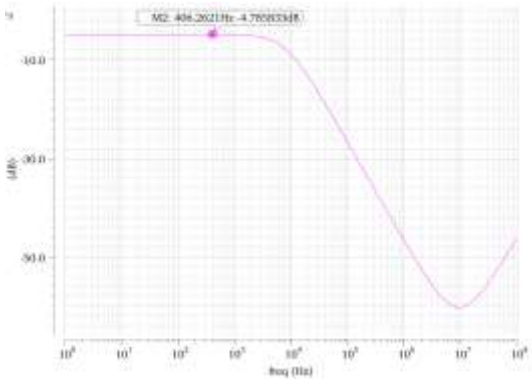

Fig6: CMRR of Two stage Op-Amp

Fig7: Stb summary Two stage OpAmp

XI. STABILITY SUMMARY OF OP-AMP:

1. Phase Margin: 83.3 degree.
2. Unity Gain Bandwidth of the Loop: 4.249MHz.
3. Device is exceptionally stable.

XII. ACHIEVED SPECIFICATION OF OP-AMP:

Design Specification	Values	Achieved Specifications	Improvement
DC Gain	60dB	63dB	5%
Phase Margin	60 degrees	83 degrees	41%
CMRR	50dB	68dB	36%
Unity Gain Bandwidth	5MHz	9MHz	80%
Slew Rate	10V/usec	9.9V/usec	Same

XIII. CONCLUSION:

We've chosen CADENCE VIRTUOSO software and a 90nm process design kit (PDK) for our IC design project. This will enhance our skills in IC Design and proficiency in Cadence. Our aim is to apply theoretical knowledge to real-world projects and gain insight into IC design used in various applications in companies. This paper presents a detailed design and analysis of a miller-compensated two-stage operational amplifier. We plan to conduct bench tests on different aspects of our designed Op-amp and analyze the results. Additionally, we aim to explore various implementations of the Op-amp to deepen our understanding of Op-amp circuits.

XIV. REFERENCES:

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