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Implementation of Optimized Reversible ALU for DSP Applications

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ABSTRACT

The test of force dissemination in electronic items using chips, stressing the requirement for productive power-decreasing models to bring down support costs. It distinguishes installed gadgets, graphical processors, and DSP processors as especially impacted by low power concerns. The Number juggling Rationale Unit (ALU) is singled out as a basic part in these frameworks, entrusted with consuming negligible power and space while keeping up with fast tasks and precision. The paper proposes the plan and execution of an ALU utilizing reversible rationale doors as a way to lessen power utilization. Reversible rationales are known for their capacity to limit energy dispersal. The goal is to look at the power utilization and area of customary ALUs with those utilizing reversible rationale entryways empowering a complete assessment of their proficiency and viability in tending to drive dissemination challenges the two structures are created utilizing Verilog HDL Utilizing the Artix-7 AC701 Evaluation Platform and Xilinx VIVADO.

Index Terms: Reversible logic gates, Field Programmable Gate Array (FPGA), Quantum cost, Arithmetic Logical Unit (ALU).

I. INTRODUCTION

In hardware implementations and digital signal processing (DSP) applications where high-speed multiplication is essential, the Vedic multiplier is frequently utilized. Despite the Vedic multiplier's increased popularity due to its effectiveness, its use may be limited by the system's particular needs and the trade-offs between power, speed, and area. One prominent Vedic multiplier that is referenced is "Urdhva Tiryakbhayam," which stands for both across and vertical.[2] This multiplier is well-known for being straightforward and effective at performing challenging multiplication calculations. Vedic multipliers have the potential to speed up multiplication tasks, which makes them useful for applications such as digital signal processing (DSP). Furthermore, several iterations of Vedic multipliers are investigated in order to minimize power dissipation an important factor in embedded systems. Vedic multipliers are generally marketed as having the ability to speed up and simplify multiplication operations across a range of computational applications. This work's goal is to address the functional blocks' design. In the design of a digital system, an arithmetic logical unit is a crucial subsystem. It functions as both the arithmetic and logic portion of a combinational logic unit, which is a crucial component of a computer processor.[12] From processors to application-specific integrated circuits (ASICs), very large-scale integrated circuits (VLSI) usually need ALUs with different fixed bitwidths and full precision bit-widths. ALU is becoming more compact and sophisticated these days in order to facilitate the creation of processors and computers that are both smaller and more powerful. Computer, digital signal processing, and networking applications have increased demand for processors with high performance, low power consumption, and compatibility. Logic operations like AND, OR, NOT, and XOR, as well as arithmetic operations like multiplication, addition, division, and subtraction, require a variety of processor types for different types of applications.

REVERSIBLE LOGIC GATES:

The reversible logic gates are used for reducing power consumption and loss of data. Reversible computing is the application principle of recycling to computing.[1] Because inputs can be reconstructed from the output. Reversible logic can be defined as the logic in which the number of output lines is equal to the number of input lines i.e., the i-input and o-output Boolean function F(X1, X2, X3,....Xn) is said to be reversible if and only if (i) I is equal to o and (ii) Each input pattern is mapped uniquely to output pattern. So that the gate can run forward and backward i.e., input can be retrieved from output.

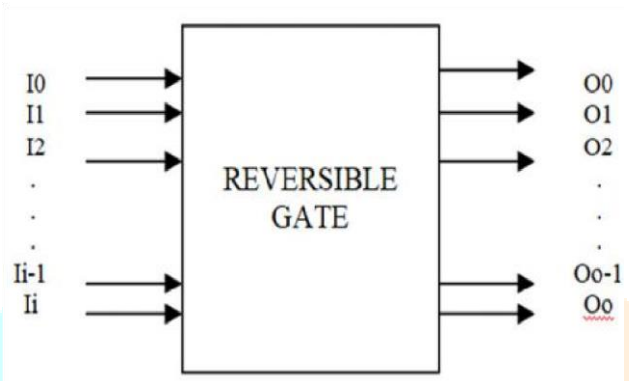
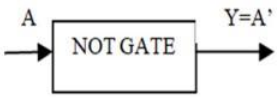


Fig 1: An n x n Reversible Gate

Reversible rationale jam data, a property took advantage of in planning reversible rationale doors, which are then used to make combinational circuits. This paper centers around installing reversible ALU (Number juggling Rationale Unit) utilizing different reversible rationale entryways and contrasts its presentation and a traditional ALU. The planned circuit is carried out on a Xilinx board for assessment and testing purposes.

NOT GATE:

It is a simple 1 x 1 reversible logic gate with zero quantum cost. Block diagram and Truth table are shown in figure

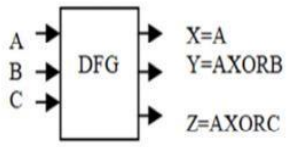


A	Y
0	1
1	0

Fig 2: NOT Gate and its truth table

FEYNMAN GATE OR CNOT GATE (FG):

It is a 2 x 2 reversible gate with quantum cost 1. It is also called as Controlled NOT gate. Block diagram and Truth table are shown in figure

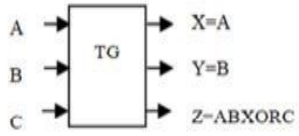


A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig 3: DFG and its truth table

TOFFOLI GATE (TG):

It is a 3 x 3 reversible gate with quantum cost 4. Block diagram and Truth table are shown in figure

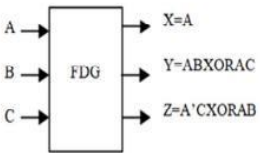


A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Fig 4: TG and its truth table

FREDKIN GATE (FDG):

It is a 3 x 3 reversible gate with quantum cost 5. Block diagram and Truth table are shown in figure

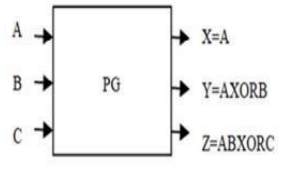


A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig 5: FDG and its truth table

PERES GATE (PG):

It is a 3 x 3 reversible gate with quantum cost 4. Block diagram and Truth table are shown in figure

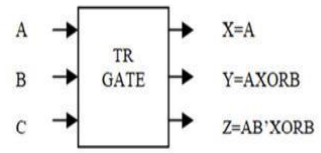


A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig 6: PG and its truth table

TR GATE:

It is a 3×3 reversible gate. Block Diagram and Truth table are shown in the below Figure.



A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

Fig 7: TRG and its truth table

II. LITERATURE REVIEW

Reversible logic has received great importance in the recent years because of its in-cogitative feature of reduction in power dissipation which is the key requirement in low power digital designs. It has wide applications in advanced computing, low power CMOS design, optical information processing,[8] DNA computing, bio information, quantum computing and nanotechnology. In this paper a new reversible gate is proposed called SG gate. The encoding and decoding logic has been explained with the help of an algorithm and example. This paper proposes a full adder, N bit adder and an N*N bit reversible multiplier using SG gate. The partial products can be generated with the help of a AND gate. A4 bit architecture of the proposed reversible adder and multiplier is also designed. Thus, this paper provides the initial threshold to building of more complex system which can execute more complicated operations using reversible logic.

Reversible logic has extensive applications in emerging nanotechnologies, such as quantum computing, optical computing, ultra low power VLSI and quantum dot cellular automata. In the existing literature, designs of reversible sequential circuits are presented that are optimized for the number of reversible gates and the garbage outputs. The optimization of the number of reversible gates is not sufficient since each reversible gate is of different computational complexity, and thus will have a different quantum cost and delay. [13]While the computational complexity of a reversible gate can be measured by its quantum cost, the delay of a reversible gate is another parameter that can be optimized during the design of a reversible sequential circuit. In this work, we present novel designs of reversible latches that are optimized in terms of quantum cost, delay and the garbage outputs. The optimized designs of reversible latches presented in this work are the D Latch, JK latch, T latch and SR latch.

The usual general-purpose computing automaton (e.g., a Turing machine) is logically irreversible—its transition function lacks a single-valued inverse. Here it is shown that such machines may be made logically reversible at every step, while retaining their simplicity and their ability to do general computations. This result is of great physical interest because it makes plausible the existence of thermodynamically reversible computers which could perform useful computations at useful speed while dissipating considerably less than kT of energy per logical step. In the first stage of its computation the logically reversible automaton parallels the corresponding irreversible automaton, except that it saves all intermediate results, thereby avoiding the irreversible operation of erasure.[3] The second stage consists of printing out the desired output. The third stage then reversibly disposes of all the undesired intermediate results by retracing the steps of the first stage in backward order (a process which is only possible because the first stage has been carried out reversibly), thereby restoring the machine (except for the nowwritten output tape) to its original condition. The final machine configuration thus contains the desired output and a reconstructed copy of the input, but no other undesired data. The foregoing results are demonstrated explicitly using a type of three-tape Turing machine. The biosynthesis of messenger RNA is discussed as a physical example of reversible computation.

We review the history of the thermodynamics of information processing, beginning with the paradox of Maxwell's demon; continuing through the efforts of Szilard, Brillouin, and others to demonstrate a thermodynamic cost of information acquisition; the discovery by Landauer of the thermodynamic cost of information destruction; the development of the theory of and classical models for reversible computation; and ending with a brief survey of recent work on quantum reversible computation [5].

It is argued that computing machines inevitably involve devices which perform logical functions that do not have a single-valued inverse. This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function. This dissipation serves the purpose of standardizing signals and making them independent of their exact logical history. [4]Two simple, but representative, models

of bistable devices is subjected to a more detailed analysis of switching kinetics to yield the relationship between speed and energy dissipation, and to estimate the effects of errors induced by thermal fluctuations.

III. REVERSIBLE COMBINATIONAL CIRCUITS AND REVERSIBLE ALU

Reversible Combinational circuits:

Any circuit's combinational circuit output is dependent upon the input values as of right now. The output is independent of both the input value and the preceding output value at all times. In this study, we design combinational circuits with reversible logic-based decoders, such as adders, subtractors, comparator multiplexers, etc.

4□32 Reversible Logic gate: When a 32-bit ALU is used, reversible logic gates are used to guarantee that every operation carried out by the ALU is reversible, which implies that the input can be uniquely determined given the output. Minimizing energy dissipation and guaranteeing information retention are crucial for specific applications in low-power computing, quantum computing, and information processing.[11] Create a set of operations (such addition, subtraction, logical AND, OR, XOR, etc.) using reversible gates such as Toffoli gates, Fredkin gates, or other reversible gate equivalents in order to design a 32-bit ALU employing reversible logic gates. Because of these gates, efficient computation without information loss is possible because every action carried out inside the ALU can be reversed.

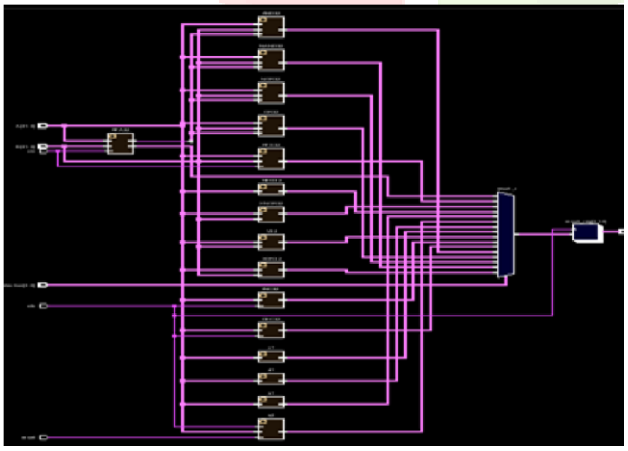


Fig 8: 32-bit ALU Using reversible Logic Gates

Full Adder/Subtractor:

A digital circuit that can add and subtract binary values is called a full adder/subtractor. It has three inputs: a carry-in (Cin) from a previous stage or operation [1], and two inputs (A and B) that represent the numbers to be added or subtracted. Two outputs are generated by the circuit: a carry-out (Cout) and a sum (S).

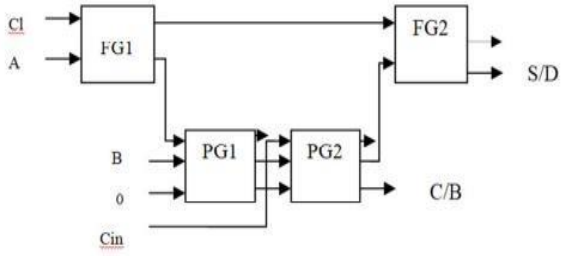


Fig 9: Full Adder/Subtractor

For addition: The sum output (S) is the result of adding A, B, and Cin together modulo 2 (i.e., S = A XOR B XOR Cin).The carry-out (Cout) represents the carry that occurs when adding A, B, and Cin, and is given by Cout = (A AND B) OR (Cin AND (A XOR B)).

For subtraction: The result of subtracting B from A (or vice versa) while taking into account the borrow (Borrow) from the previous stage the opposite of the borrow that would occur in a binary subtraction operation is represented by the sum output (S).The carry-out (Cout), which is the opposite of the carry-out that would take place in a binary subtraction operation, indicates whether a borrow from the current stage is necessary.

Vedic 32-bit Multiplier:

An effective method for multiplying two 32-bit binary values is the Vedic 32-bit multiplier, an arithmetic algorithm based on concepts from ancient Indian mathematics. By dividing the multiplicand and multiplier into smaller, more manageable pieces, it breaks down the multiplication procedure into smaller, more manageable parts.[8] Then, it uses addition, subtraction, and shifts to compute the product. This strategy seeks to maintain inherent parallelism while minimizing the amount of operations required, perhaps providing quicker multiplication than traditional techniques. By utilizing its parallel processing capabilities and simplicity, the Vedic multiplier offers a computationally efficient substitute for applications that necessitate quick multiplication.

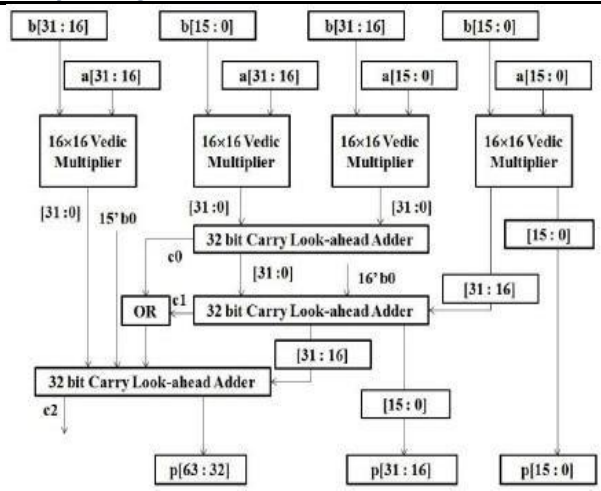


Fig 10: Vedic 32-bit Multiplier

ARITHMETIC LOGIC UNIT (ALU):

Arithmetic Logic Unit (ALU): This device executes different operations in response to particular control signals. The ALU's functioning is determined by these control signals, which are 4-bit values. Two sets of 32bit input data can be handled by the ALU, which can also output 32-bit data.[10] The arithmetic and logical operations that the ALU is capable of performing are outlined in Table , where each operation is mapped to a distinct set of control signals. This design offers flexibility and variety in digital processing jobs by enabling a wide range of computations, including logical operations (AND, OR, XOR, etc.) and arithmetic operations (subtraction, addition, etc.

IV.SIMULATION RESULTS

Existing Method:

The ongoing ALU executes assorted activities directed by control signals. These activities depend on unambiguous control signals, with the ALU arranged to oblige 4-cycle control signals, alongside two arrangements of 32-bit input computerized information and 32-bit yield advanced information. Table represents the variety of number-crunching and intelligent tasks completed by the ALU, each relating to particular control signals.

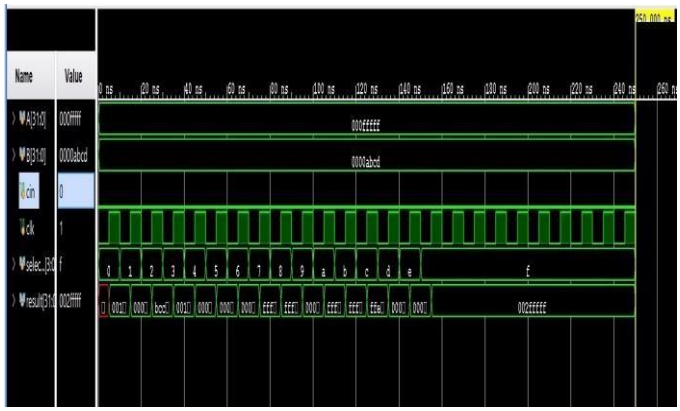


Fig 12: Simulation of ALU

Proposed Method:

The purpose of a 32-bit reversible ALU (Arithmetic Logic Unit), a specialized CPU part in computers, is to minimize energy dissipation while executing arithmetic and

logical operations on 32-bit binary integers.[9]

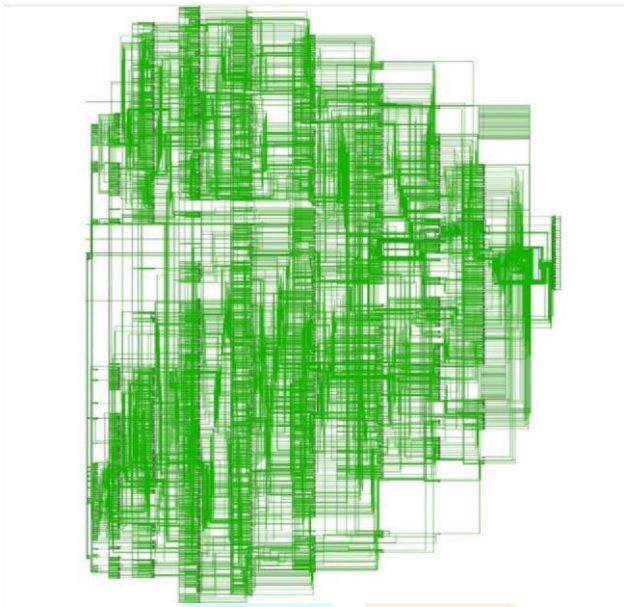


Fig 11: Technology Schematic of ALU

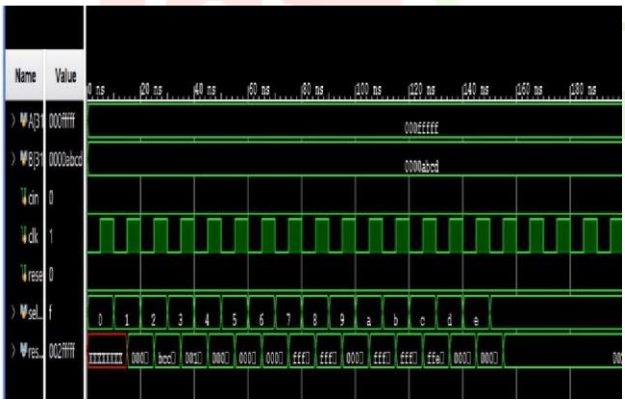


Fig 13: Technology Schematic of Reversible ALU

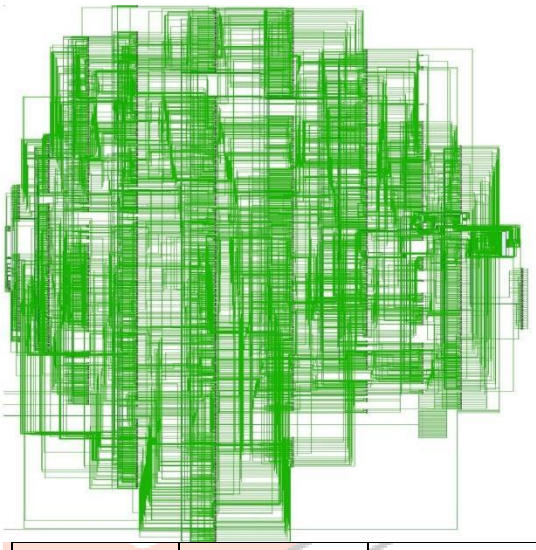
Fig 14: Simulation Result of Reversible ALU

V.COMPARATIVE STUDY

The comparison between the existing method and the proposed method (pipeline) of the 32 bit

Parameters	**Existing method**	**Proposed method (Pipelining Method)**
Area (LUT)	6755	5700

Reversible ALUs allow operations to be reversed, allowing for efficient energy utilization, in contrast to regular ALUs that irreversibly change inputs into outputs. Reversible logic gates are used to do this, guaranteeing that no data is lost during calculation. A reversible ALU's major objective is to lower power consumption without sacrificing accuracy or speed, which qualifies it for use in situations where energy economy is vital.



Delay (ns)	615.360	413.073
Power (milli watts)	210.314	163.724

Table: Comparison

VI. CONCLUSION

Reversible logic gates are used in the Reversible ALU proposed for various DSP applications, and it is implemented using the Verilog hardware description language. The ISIM simulator is used to simulate the design, and Xilinx VIVADO 2018.3 is used for synthesis. When compared to traditional ALUs, the ALU reduces area and power consumption by utilizing reversible logic in combinational circuits. These combinational circuits also provide flexibility in implementing different digital circuits, which improves overall performance.

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