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Novel Algorithm For DWT-SPIHT Based Medical Image Compression

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Abstract: — With more than 1.3 billion people living in India, the country's health care system still has a ways to go before it can adequately serve this sizable population with dependable and reasonably priced medical treatment. Telemedicine is one of the growing technologies that might facilitate access to medical services for the rural population. Since medical images take up a lot of storage space and transmission time is a bottleneck for real-time telemedicine requirements, developing algorithms and implementing them on VLSIs is crucial for processing images and videos quickly. In this work, fast and robust algorithms and their VLSI architectures have been designed for medical image compression supporting both 2D and 3D medical images.

***Index Terms* -** DWT, IDWT, SPHIT, MATLAB, FPGA, Telemedicine, FFT Analysis.

I. Introduction

One of the most exciting developments in clinical medicine is telemedicine, which allows doctors to discuss and examine patients remotely using medical data via the phone, the Internet, or any other network. Human imaging is now feasible at scales ranging from a single molecule to the entire body thanks to technological advancements [1]. Through the use of computer simulations and the anatomical data gathered with new imaging technologies, researchers are now able to create fully functional representations of specific patients. Physicians will be able to view both the appearance and the functioning of a patient's organs, even at the tiniest dimensions, thanks to these images [2, 3].

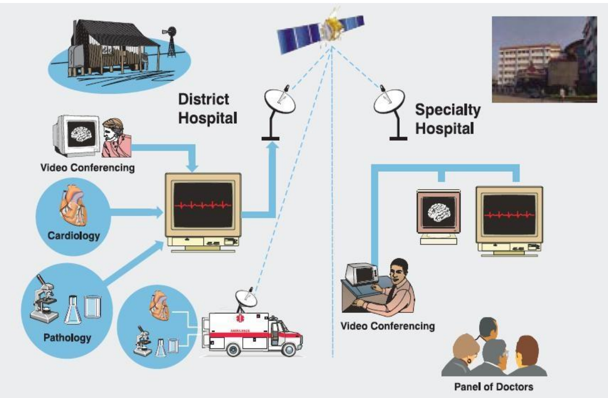


Figure 1 Outline of TelemedicineNetwork

Storing, analysing, dispersing, comprehending, and utilising the massive amount of data connected with thousands of photographs is a significant difficulty in the field of telemedicine. The various image acquisition devices include CT (Computer Tomography), SPECT (Single Photon Emission Computer Tomography), MRI (Magnetic Resonance Imaging), and PET (Positron Emission Tomography) [4]. These devices use high-end sensors to acquire images from patients, which are then analysed by specialised doctors for further diagnosis [5]. The obtained images, which are in two and three dimensions, offer details about the human body in both place and time. The need for more data storage space rises along with the need for high-resolution medical imaging.

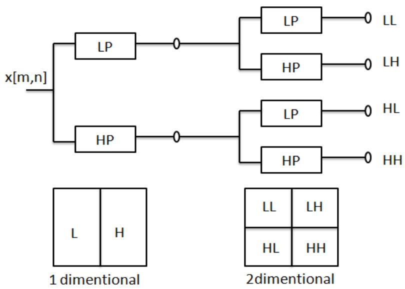
The main health centre and specialist centre do ctors communicate with each other through video conferences while attending to patients. Patients in the primary health clinic receive recommendations and medication from a panel of doctors who are located remotely[5,6,7]. Important telemedicine challenges are: Deficient infrastructure, Experts (disparate distribution) are not available for diagnosis at every place, Low patient-to-doctor ratio (big population), Standards control the compression of picture and video sequences to guarantee worldwide interoperability across several platforms.

The Moving Picture Experts Group (MPEG), JPEG 2000, H.263, and JPEG are a few of the standards that offer instructions for compressing pictures and video clips. 2D DWT computes multi-level sub bands for picture data compression [14,15]; the sub bands are quantized before the 2D sub bands are encoded using SPIHT encoding. 3D input data (time-shifted sequences of 2D pictures) are used to compute 2D DWT, which yields the sub bands. Additionally, as illustrated in Fig. 1.4, a third dimension—namely, time—is computed for the 3D. The 3D SPIHT technique is used to encode the sub-bands of the deconstructed 3D data in order to compress the input data. The receiver decodes the encoded data after it has been transferred over a communication channel[11].

creation of innovative architectures that support FPGA realisation and 2D DWT/IDWT computing. The design has been synthesized using Xilinx ISE targeting on a Virtex FPGA. The design was optimized for area, power and speed performances. 3D DWT/IDWT and SPIHT architectures have been developed based on parallel processing algorithm and a pipelined architecture has been implemented on FPGA platform. The proposed architecture has been validated on Virtex 5 FPGA.

II. NOVEL ALGORITHM FOR DWT-SPIHT BASED

Various aspect ratios are used in medical photographs to choose which region of interest to choose and which compression algorithm to use. This paper suggests a novel approach that, before compression, preprocesses the input image with a uniform aspect ratio. In this work, a variety of DWT filters, including Haar, Biorthogonal, and Daubechies Wavelets, have been utilised to compress and decompress medical images, and appropriate filters have been chosen for the purpose. Comprehensive analysis is also done on filter selection and how it affects the compression ratio. A MATLAB code for the suggested algorithm has been created. The suggested compression algorithm has been validated using a variety of medical photos,



and the generated algorithm is appropriate for telemedicine applications.

Figure 2.2 -Dimensional DWT

Wavelet based Image Compression

Two Wavelet-Based Compression Techniques Wavelet coding has gained a lot of traction because of its reliability in gearbox. Furthermore, compared to other transformations, blocking artefacts in reconstructed images are greatly reduced. The foundation of wavelet-based compression [59–62] is sub-band coding. Sub band coding entails dividing the image's frequency band into smaller bands, then precisely matching the bit rate of each coder to the band's statistics. A low pass filter and a high pass filter, which divide the image into low frequency and high frequency sub bands, make up a simple DWT. The two-dimensional picture decomposition is depicted in Fig. 5. Row decomposition is the first step, and column decomposition is the second.

Proposed Image Compression and Decompression System

Fig. 3 shows the traditional block diagram of an image compression and decompression system based on DWT and SPIHT. As seen there, the input image is first conv erted into numerous levels made up of sub bands using DWT. The subbands that have broken down are rearranged into a 1D array and then encoded using the SPIHT technique. After being delivered, the encoded bit stream is decoded using the inverse SPIHT method at the receiving end.

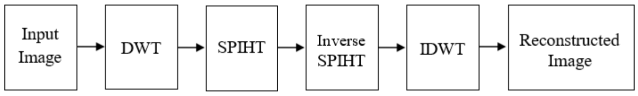


Figure 3 Basic Block Diagram of Image Compression and Decompression System

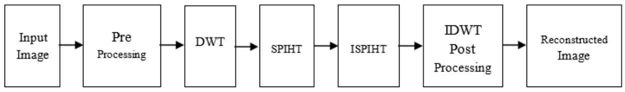


Figure4. Proposed Block Diagram for Image Compression System

Fig. 4 presents the suggested compression technique. According to this plan, the pre-processing module resizes the input image to N × N by using symmetric extension or zero padding. In order for the DWT to function on a symmetrically extended input image, symmetric extension is selected. An image's quality can be assessed using the Peak Signal to Noise Ratio. Equation 2 provides the definition of the PSNR.

A high PSNR indicates that the reconstructed image closely resembles the original. The performance of biorthogonal wavelet filters is demonstrated by the data plotted against PSNR in Fig. 3.8. On the x-axis, the numbers 0.1 to 6 imply the compression ratio increasing in bp, or in descending order. For different image sizes, PSNR is observed to grow from 10 dB to a maximum of 35 dB. In the case of 256x256 images, PSNR stays constant at 25 dB as bpp grows.

Design of High Speed DWT/ IDWT and SPIHT Architectures for Medical Image Compression

The three steps of image compression are encoding (SPIHT), quantization, and picture transformation using DWT. Through the use of a specialised DWT processor, 2D DWT is computed on the input image, producing four sub bands at each level of decomposition. Because the input image is made up of rows and columns, first level decomposition is obtained by applying DWT processing to the rows and then to the columns. Moreover, a 2D DWT processor is used to split the lowest subband into four smaller subbands. It is necessary to use 1D DWT to conduct N1 row decomposition if the input image has dimensions of N1 x N2.

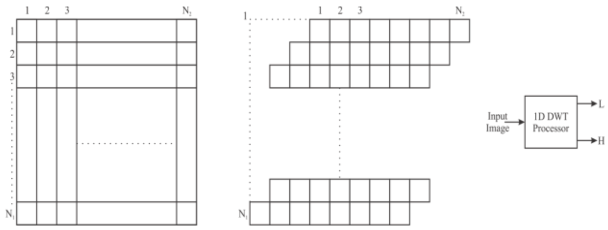


Figure5. Row Processing Logic of Input Image

Using Inverse DWT, the input image that has been broken down into subbands must be rebuilt. The array processor architecture covered in the previous section is used in the creation of the inverse DWT processor. Since a 9/7 wavelet filter was chosen, the LPF and HPF coefficients for the reconstruction procedure are 7 and 9, respectively. During decomposition, symmetric extension was applied to the input data. The symmetric extension is not needed for reconstruction. 64 samples that are kept in memory make up the matrix P that represents the deconstructed data.

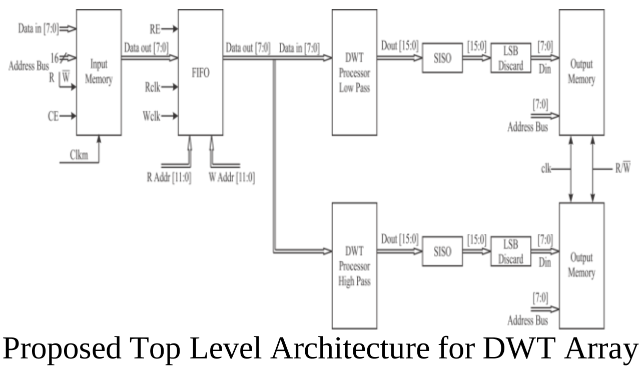


Figure 6 Proposed Top Level Architecture for DWT Array Processing

The decomposed sub band, represented by an 8 x 8 P matrix, is sent to the inverse HPF and LPF filters. Using the P matrix and the H matrix, which stand for the LPF reconstruction filter coefficients, V is derived.

The eight by eight P matrix is multiplied by the eight by eight H matrix to get the eight by eight V matrix. In order to create the reconstruction output matrix represented by R, the P matrix is additionally processed by the G matrix, which represents the HPF filter coefficients. Because there are nine filter coefficients for HPF reconstruction, a symmetric extension of one column is applied to the eight-by-eight input matrix P.

Consequently, the 8 x 8 P matrix is enlarged to 8 x 9, and the 9 x 8 filter coefficient matrix is likewise set for the reconstruction of HPF element.

SPIHT Architecture

The input image is broken down into subbands of different frequency components using DWT. Both high frequency and low frequency components are present in the decomposed sub bands. The higher sub bands are kept unchanged after one level of decomposition; the low sub band component is further broken down into four sets of sub bands using 2D DWT. All other subbands are regarded as children, whereas the lowest subband, which is the low frequency component, is regarded as the parent. SPIHT technique is used for compression of the disassembled image. The List of Significant Pixels (LSP), List of Insignificant Pixels (LIP), and List of Insignificant Sets (LIS) are the three lists used by SPIHT. These are coordinate-containing lists of the locations of the coefficients

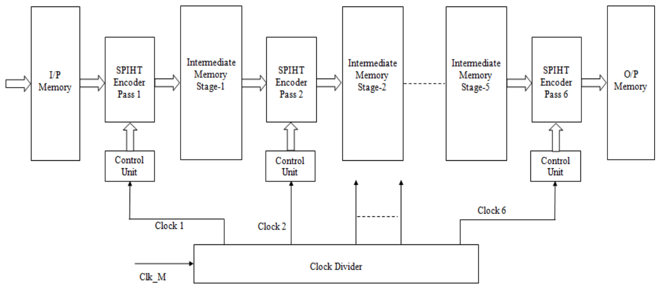


Figure 7 Proposed Top Level Pipelined Architecture for SPIHT Encoder

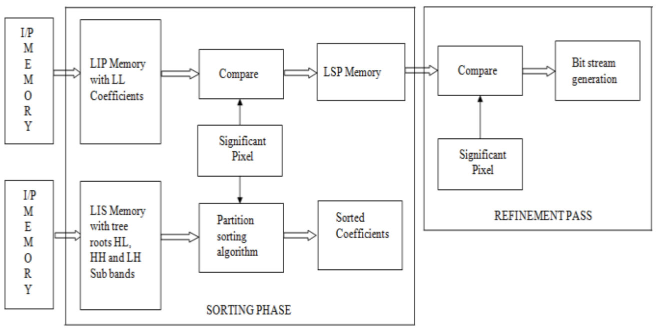


Figure 8 Architecture of SPIHT Encoder

the hierarchical sub bands that are created after two levels of 2-D DWT are kept in an input memory. The bit stream is produced by the SPIHT iteration 1 module, as shown in Fig. 8. In the second iteration, the threshold module further scales the sub bands for bit stream production. The necessary compression ratio determines the threshold levels. For LL and higher subbands, a configurable threshold is set in this work. Till there are elements in the input memory's sub bands that are greater than 10, the SPIHT encoder computes the bit stream periodically. To get the maximum compression ratio, a trial-and-error process is used to determine the number 10.

Parameters	**Resource utilization**
No. of slices	2389 out of 69120
No. of LUTs	3321 out of 69120
Max. Frequency	265 MHz
Power Dissipation	0.9 mW

Table 1 Synthesis Results of SPIHT Encoder

Targeting the Virtex-5 FPGA (XC5VLX 110T), the SPIHT encoder is synthesised using Xilinx ISE and programmed in Verilog. Fig. 9 displays the synthesis findings of the pipeline's first stage.
The SPIHT encoder's synthesis results on the Virtex-5 FPGA are displayed in Table 4.5. The power and time performances of the RTL code are optimised. The coded SPIHT method is functionally valid based on the simulation and synthesis results (simulation waveforms are not displayed due to the excessive number of iterations involved). Additionally, the design is enhanced for high-speed applications.

III. VLSI IMPLEMENTATION OF MEMORY EFFICIENT MULTIPLIER LESS 2D-DWT/IDWT ARCHITECTURE

Multiplication and accumulation units are used to implement the convolution algorithm-based DWT computation, as seen in Fig. 5.4. The input samples are processed sequentially in the traditional DWT

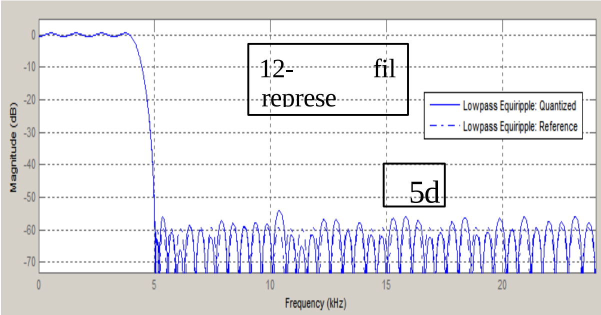


Figure 9. Frequency Responses of Filter Coefficients

architecture based on the convolution method by multiplying them by the filter coefficients A[N] and adding the samples to compute Y[n]. For low pass and high pass, the DWT filters have nine and seven filter coefficients, respectively.The top level architecture of the suggested memory efficient multiplier less 1D-DWT processor is depicted in Fig. 10

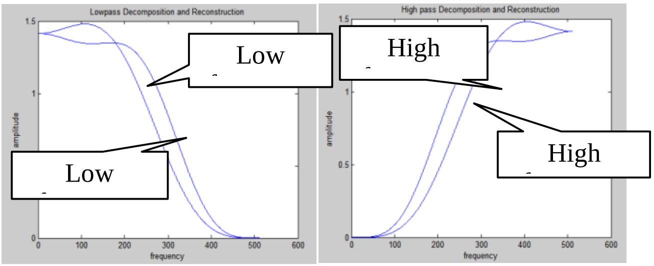


Figure 10. Effects of Quantization

The multiplexer unit rearranges the data for the 1D-DWT computation column wise and reorders the intermediate samples into the output memory for the 2D-DWT computation. The input data flow and the output sample computation utilising the convolution method and the LPF and HPF filters are depicted in Fig. 5.6. The processing unit receives fresh data every clock cycle, which is multiplied by the low pass filter coefficients. The processing unit output is ignored for the first eight clock cycles since the input samples are absent during this time. Nine clock cycles represent the lag since YL8 is the first out sample.

IV. RESULTS

Modelsim and Xilinx ISE are the tools used to obtain the simulation and synthesis outputs, respectively. The other inputs are reset and clock, and the input xi consists of eight bits. After scaling, the outputs are 16-bit signed approximation coefficients (ai) and detailed coefficients (di). The outputs are expressed in the complement notation of 2. For every value of i, the matching values of ai and di were obtained in a single clock cycle.
Model Sim was used to simulate the DWT verilog code for i between 0 and 63, yielding the corresponding values of ai and di. The results for various values of i with inputs X0 = 0 and X1 = 1 are displayed in Fig. 10

Since x2i-4 is the smallest value of x, both ai and di are equal to 0 when i is less than 2. The inputs are first saved before the output is evaluated since the outputs require all of the input values. Ai and di are obtained during each clock cycle; that is, when i = 1, a1, and d1 are obtained. The following cycle yields a2, d2, and so forth. It was discovered that the theoretical and practical values computed matched. The contrast between the theoretical and actual values obtained is displayed in Table 1. When the formulae for ai and di were substituted in for the values of x, it was discovered that, for i = 2, the highest deviation was +/- 8 for ai = 9140 and di = - 1275.

A redesigned technique that takes advantage of the symmetric property to cut the number of computations in half is used to realise the DWT processor. Shift left operations are used to realise the filter coefficients that are acquired after quantization and are rounded off to the nearest power of two. Verilog was used to implement the altered method for 1D- and 2D-DWT processors. The outcomes show gains in area and speed performances with no loss, making them appropriate for almost lossless picture compression. The tool's numerous constraint settings allow for the verification of the synthesised findings. The default settings were yielding the best outcomes. In this study, the power report and timing report in terms of slices have been prepared and reported.

V. CONCLUSION

Since shift operations are used in place of multipliers, it is evident from the comparison of results that the suggested architecture uses a relatively small amount of resources. When compared to the Conventional Convolution based DWT Processor, the operating frequency of 298 MHz is greater and the power dissipation is lower. Since shift operations are utilised for multiplication, data synchronisation during DWT computation is one of the design's main issues.

The choice of suitable wavelet filters for lossless image compression, along with a preprocessing block to establish the aspect ratio for the compression of medical images. The symmetric property of filter coefficients is exploited in the construction of the 2D DWT algorithm and architecture, while the multiplier-less DWT architecture is designed. A pipelined architecture has been proposed to boost the throughput of the encoding architecture while reducing the delay in the SPIHT encoding system. 2D DWT now uses the same multiplier-less calculation as 1D DWT.

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