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SHAVVY CHANNEL ENCODER FOR COGNITIVE RADIO- SURVEY AND DESIGN

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Abstract: People have recently been impacted by a number of unclear pandemic diseases. Under these circumstances, maintaining ties within society is necessary. In order to meet this constantly growing need, wireless communication is playing a significant role. Due to the enormous demand for wireless communication and the internet, it is important to consider how to make the best use of the available channels and frequencies, as they cannot be extended. A remedy for this issue is cognitive radio (CR). This article proposes the design of a Real Time Smart Channel Encoder to support CR technology and expanding Artificial Intelligence. This will support effective channel utilization and the realization of current CR technology.

The survey for comprehending cognitive radio, channel encoder, artificial intelligence, and the viability of real-time smart channel encoder is presented in this study.

Index Terms **- Cognitive radio(CR), channel encoder, VLSI, GNU radio, RTL, FPGA.**

I. INTRODUCTION

High-speed wireless mobile communications are becoming increasingly popular. Traffic is growing as a result of this, however bandwidth and accessible frequencies are constrained. Therefore, if we do not wisely handle the available frequencies, this additional traffic could result in a breakdown of the communication system. Additionally, because new communication systems need greater bandwidth and data rates, there may be a spectrum shortage. This happens because some customers have stagnant spectrum allocations and are not fully utilizing them. So, is there anything we can do to use this unutilized spectrum and improve traffic?

The technology as a solution that supports dynamic allocation of unused licensed spectrum to other users without disturbing the licensed users (primary users) effectively is called Cognitive Radio.

The main aim of CR is to increase utilization of spectrum by identifying unused as well as under-utilized spectrum in both normal and rapidly changing environmental conditions.

There are many definitions of cognitive radio: “Cognitive radio employs a dynamic time-frequency-power based radio measurement and analysis of the RF environment, to make an optimum choice of carrier frequency and channel bandwidth to guide the trans-receiver in its end-to-end communication with quality of service being an important design requirement.- Wireless World Research Forum(WWRF)”.[1]

II. SURVEY-COGNITIVE RADIO NETWORK

2.1 A systematic review of cognitive radio

The benefits and drawbacks of the wideband and narrowband spectrum sensing approaches, as well as implementation difficulties, have been covered in this paper. The author has provided explanations regarding the daily growth in demand for wireless gadgets and their internet access. According to the author, the issue is that the existing productivity of radio spectrum managers is insufficient to permit admission of this number of devices given the rise in demand for wireless channels. Because there is a paucity of radio spectrum, it is not practicable to share it among customers. With this in mind, research has indicated that Cognitive Radio technology, the subject of significant study by the scientific community, is one solution to these issues as well as many others. Cognitive radio technology is what makes it.[2] [3]

2.2 Decision making approaches in Cognitive radio

The author of this study has discussed a number of CR cycle steps, including spectrum sensing, spectrum decision-making, spectrum mobility, and spectrum sharing.

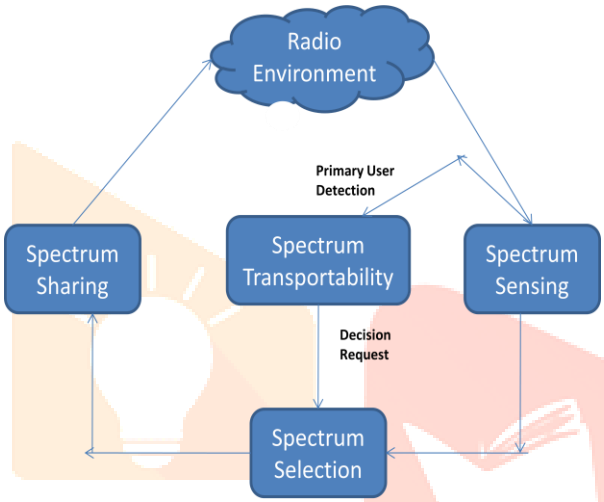

Figure 1: Cognitive Radio Cycle

The most crucial step is analysis and decision-making among these. It demonstrates cognitive radio, an artificial intelligence method.[4]

In Cognitive Radio Networks, users (or secondary users/unlicensed users) sense channels and use the available channels when they are not in use by primary licensed users, vacating the channel when the primary licensed users return to it. This prevents cognitive users from interfering with license users.[5] [6]

III. SAVVY CHANNEL ENCODER

The primary goals of near-future wireless communication systems are faster data rates, reliability, higher bandwidth, higher spectrum efficiency, energy efficiency, combined with reduced latency and fewer error, even if communication technology progress is a constant process.

Reliability of wireless communication systems can be increased by channel encoding as it adds extra bits in controlled manner and is considered to be most efficient element of communication system.

Many channel encoding techniques are used in encoding purpose such as, Convolutional code, Turbo Code, Repeat Accumulate Code, Reed Solomon Code, Low density parity check (LDPC) code, Polar code, Hamming Code etc. Among these it is user's intelligence to choose the particular coding technique as per the application. The main motive of channel encoder is to provide secured data transmission, reduced effect of noise and achieve less bit error rate.

Convolutional codes, Block codes, are the two fundamental forms of channel codes. Block codes are based on abstract algebra and finite field arithmetic. They are capable of detecting and correcting faults. This category includes LDPC and Reed Solomon codes. Convolution codes alternatively are created using a distinct strong mathematical framework and are generally utilized for real-time error correction. They combine all of the data into a single codeword. [7] [8]

3.1 *Convolutional code*

In convolutional codes, the message comprises of data streams of arbitrary length and a sequence of output bits are generated by exercising various Boolean functions to the data stream. [9]

In process of generating a convolutional code, the information is first passed sequentially through a linear finite-state shift register. The shift register comprises of (n-bit) stages and Boolean function generators.

A convolutional code can be represented as (n,k, K) where

- k is the number of bits shifted into the encoder at one time. Generally, k = 1.
- n is the number of encoder output bits corresponding to k information bits.
- The code-rate, Rc = k/n.
- The encoder memory, a shift register of size k, is the constraint length.
- n is a function of the present input bits and the contents of K.
- The state of the encoder is given by the value of (K - 1) bits. [10] [11]

3.2 Turbo code

Turbo codes are powerful error correction codes invented in the 1990s that are built by parallel concatenating two convolutional codes, connected via an interleaver, and decoded iteratively by using two soft-in-soft-out (SISO) decoders that exchange extrinsic information during each iteration.[10] [11]

3.3 LDPC

A low - density parity check (LDPC) code is specified by a parity-check matrix containing mostly 0's and a low density of 1's. The rows of the matrix represent the equations and the columns represent the bits in the codeword, i.e. code symbols. [12]

A LDPC code is represented by, where is the block length, is the number of 1's in each column and is the number of 1's in each row, holding the following properties –

- x is the small fixed number of 1's in each column, where x> 3
- y is the small fixed number of 1's in each row, where y> x.

3.4 Reed Solomon Code

The method of encoding in Reed Solomon code has the following steps – [13]

- The message is represented as a polynomial p(x), and then multiplied with the generator polynomial g(x).
- The message vector $[x_1,x_2,x_3.....x_k]$ is mapped to a polynomial of degree less than *k* such that $px(\alpha i)$ = xi for all i = 1,...k
- The polynomial is evaluated using interpolation methods like Lagrange Interpolation.
- Using this polynomial, the other points $\alpha_k + 1....\alpha_n$, are evaluated.
- The encoded message is calculated as s(x) = p(x) * g(x). The sender sends this encoded message along with the generator polynomial g(x).

3.5 A survey on channel coding techniques for next generation wireless networks

In this paper author has surveyed that Turbo code is more suitable for LTE network whereas LDPC is most suitable for next generation wireless communication network. Author on comparison of Polar Code and LDPC code also concluded how LDPC code is better than Polar code with respect to bit error rate performance, chip area required, complexity etc. [14]

3.6 Channel coding scheme for the control channel

On comparison of various channel coding schemes LDPC code be used for large code block. However, since the performance of LDPC has no advantage when the code block is small, the use of LDPC in the control channel has always been a marginalized solution. [15]

IV. DESIGNING METHODOLOGY

An electronic device called a field-programmable gate array (FPGA) has digital logic circuits that may be programmed to perform certain tasks. A general-purpose application processor cannot accomplish this capability as quickly or with as little power consumption as the logic in the FPGA, which has been configured especially to carry out our application. A system-on-chip FPGA, sometimes known as a SoC FPGA, is an FPGA that also has a CPU built into it. [16] [17] [18]

4.1 FPGA programming using RTL

The major steps in FPGA programming are Hardware architecture design, Design using RTL, Verification, Synthesis, Integration, Implementation Lab testing and debug.

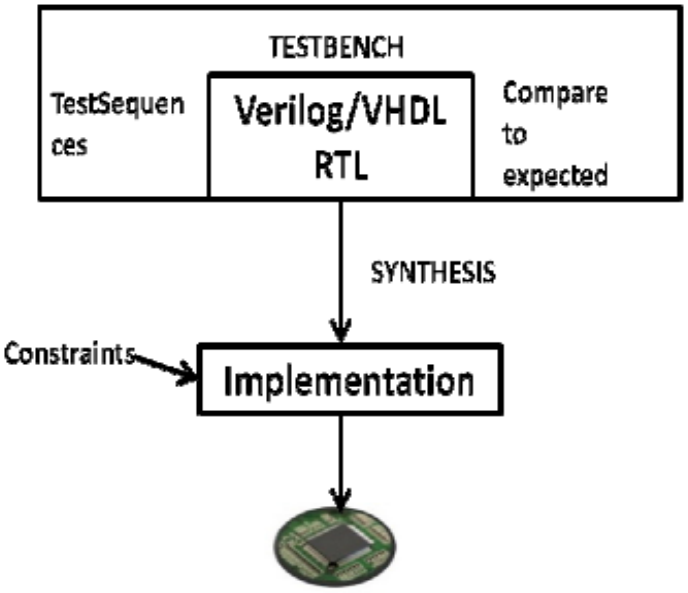

Fig.2. Workflow for FPGA using RTL/HDL

We can name this as VLSI design and implementation of circuit. VLSI i.e Very Large Scale Integration is the advanced technology used majorly in IC fabrication. Normally we can use hardware description languages such as VHDL/VERILOG for the designing of RTL i.e register transfer level. Once we code the RTL we can perform synthesis. Actually advantage of coding RTL is that we can do synthesis of our logic.

Questa Sim, Vivado, Cadence NCLaunch, Xilinx ISE are various tools used for FPGA implementation using RTL/HDL [19]. Among these Xilinx ISE is the most popular.

4.2 FPGA programming with MATLAB and Simulink

If algorithms are modeled in MATLAB and Simulink our focus remains on designing the algorithm and hardware architecture.[19]

The major steps in FPGA programming with MATLAB and Simulink are Adding hardware architecture, code generation, Integration, Synthesis and implementation.

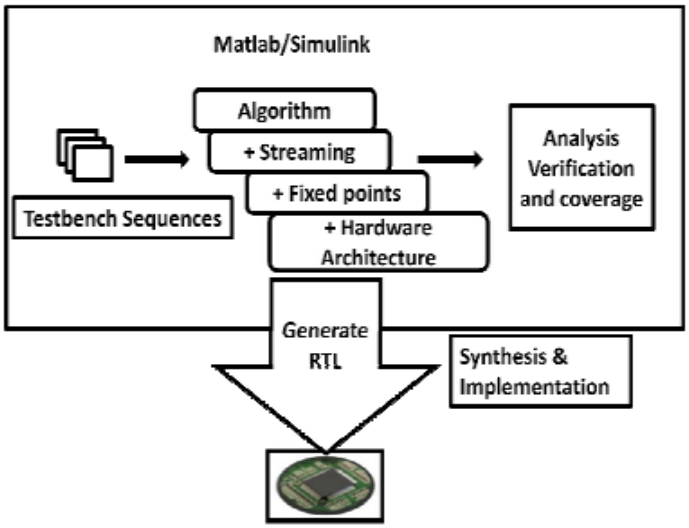

Fig.3. Workflow for FPGA using MATLAB and Simulink

Once the MATLAB-based hardware design is complete, the HDL coder creates target independent Verilog or VHDL RTL. For programming FPGAs, we still require a reference design for HDL coders to plug algorithms into.

4.3 GNU radio

Software defined radio (SDR) design can benefit from the novel reconfigurable hardware designs introduced by Field Programmable Gate Array (FPGA) technology. [20]

GNU Radio is a free & open-source software development toolkit that provides signal processing blocks to implement software radios. It can be used with readily-available low-cost external RF hardware to create software-defined radios, or without hardware in a simulation-like environment.

According to the study, in order to create and use FPGA accelerators in GNU Radio, the Zynq hardware must be configured, FPGA design software must be purchased, and an SD card containing the Linux kernel image, boot loader, root file system, and FPGA bitstream must be created. [21]

4.4 MATLAB and VLSI combination for FPGA

Circuit design is becoming increasingly difficult as wireless technology develops. Therefore, utilizing only RTL to achieve such a complex design will make code more complex. Therefore, we may test our module using MATLAB and use the resulting output vectors as the testbench inputs for RTL verification to reduce this and obtain a more reliable design.

With this approach we can reduce the efforts and complexity of RTL coding with tested and verified inputs. Also the synthesis is possible as we are dealing with RTL. So with the combination of both i.e. MATLAB and RTL/HDL we can work better for FPGA implementation. [19]

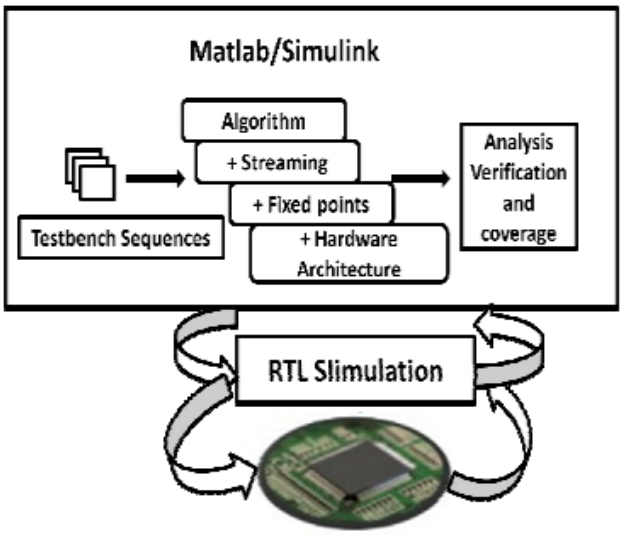

Fig. 4. Co-simulating MATLAB and Simulink together with your implemented design running

V. CONCLUSION

By adopting a dynamic spectrum allocation over the current static spectrum allocation, cognitive radio (CR) is the greatest approach in wireless communication systems for wiser spectrum utilization.

In order to obtain a low bit error rate with high dependability and real-time changes in the transmission environment, channel encoders for cognitive radio can be designed. The block code method is therefore more advantageous because it enables greater frequencies, such as next generation.

Xilinx ISE is most suitable platform for FPGA implementation over MATLAB also GNU Radio is an alternate option with SDR. Co-simulation of MATLAB and Xilinx can also be a solution for effective FPGA implementation.

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