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DESIGN OF 4 BIT FULL ADDER AND UNIVERSAL SHIFT REGISTER BASED ON QCA

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ABSTRACT

Semiconductor industry seems to approach a wall where physical geometry and power density issues could possibly render the device fabrication infeasible. Quantum-dot Cellular Automata (QCA) is a new nanotechnology that claims to offer the potential of manufacturing even denser integrated circuits, which can operate at high frequencies and low power consumption. In QCA technology, the signal propagation occurs as a result ofelectrostatic interaction among the electrons as opposed to flow to the electrons in a wire.The basic building block of QCA technology is a QCA cell which encodes binaryinformation with the relative position of electrons in it. A Quantum-dot cellular automaton (QCA) represents a modern technology for implementing small-sized circuits with high-performance, low-power consumption and various computations in digital circuits at the nanoscale level. These quantum dots made up at a nanoscale level which increases the performance of circuits. With the invention of QCA in electronics, the circuits can achieve their operations with very high efficiency and with low power dissipation. Meanwhile, a universal shift register (USR) is a particular circuit with the functions of storing and shifting bits to a specified direction and is observed as an essential component. This USR also has the process to load the data. Therefore, here we propose a USR circuit based on QCA, i.e., QUSR, which requires the essential components of a shift register and a multiplexer (Mux) combined and used to select the operation of the USR. In this project, we propose a 2-to-1 Mux, which then extended to a 4-to-1 Mux. Here, we suggest a new D flip-flop and design a shift register by connecting all of these. Finally, we propose a QUSR that consumes low power and computes high-performance by combining four 4-to-1 Muxes and a four-bit shift register. The proposed QUSR is highly efficient in time and space complexities and has a good energy dissipation performance. The proposed design performance metric of efficiency achieved by doing required simulations using the QCA Designer tool.

Keywords: QCA Technology, Cellular Automata, shift register and shifting bits.

1. INTRODUCTION

For last 40 years the advancements in the semiconductor industry have been able to keep up with the Moore‟s law. According to the International Technology Roadmap for Semiconductors (ITRS) projections, this trend is expected to continue until 2020 but beyond that the physical and power density limitations would prohibit the further scaling of the integrated circuits in contemporary manufacturing technology of complementary- metal-oxide-semiconductor (CMOS). For this very reason, researchers have been searching the avenues of nanotechnology for the rescue. They claim that nanotechnologyusing new fabrication materials could potentially replace CMOS for the most part because of the high device densities and low power consumption in nanotechnologies. One of the most promising nanotechnologies is Quantum-Dot Cellular Automata (QCA) which was first proposed by P.D. Tougaw and C.S Lent in early 90‟s. In this technology, the basic device for circuit implementation is a QCA-Cell which is very small thus enabling high densities. Both theoretical and experimental research in QCA claims that QCA circuits can operate at THz frequencies with low power consumption. A QCA cell contains electrons and the relative positions of the electrons in a cell are used to encode the binary information as opposed to voltage levels in CMOS. The counterpart of switching in CMOS is the Coulombic interaction between the electrons of QCA cells. This Coulombic interaction determines the position of electrons and thus the logic state of a cell. In CMOS or earlier technologies, the logic realization using regular structures, like Shannon lattice and Programmable-Logic-Arrays (PLA) have played an important role due to their ease of logic mapping and minimal routing requirements. In addition, it is easier to develop Electronic-Design-Automation (EDA) tools for logic synthesis using these regular structures compared to custom logic of unstructured logic networks. These properties of regular structures are highly desirable and beneficial for logic synthesis in QCA in particular.

The advantages are threefold; First, QCA circuits inherit the advantages of easier logic mapping and routing. Secondly, these propertiesare highly desirable since aforementioned processes are more complicated in QCA compared to previous circuit design technologies as the QCA is still developing. Thirdly, the use of regular structures results in simplified and uniform clocking structures,wh is one of the biggest challenges in the implementation of QCA circuits. A simple and uniform clocking structure would increasemanufacturability assuming that QCA technology would advance to that level in future. EDA tools play a vital role in the design and manufacturing of integrated circuits. EDA tools have enabled a faster and reduced effort design cycle as the complexity of chips increased considerably. It is evident that any new IC design technology would require a similar set of tools and QCA is no different. The QCA designs are not yet ready to scale to large sizes, however, the fundamental differences in circuit implementation between QCA and previous techniques require modeling and simulation EDA tools for correct understanding of QCA technology characteristics. So far, the work involving the
development of tools for QCA has been purely academic. The first tools developed for QCA simulations were MAQUINAS and QBert. The initial version, AQUINAS,which was able to perform quantum mechanical simulations of small circuits, was expanded to MAQUINAS which focused on molecular QCA. QBert tool was able to simulate larger designs but was limited to the digital logic simulations. One of the most popular recent tools is QCA Designer which allows users to create circuit layouts using graphical user interface and perform both quantum mechanical and digital simulations. Another layout tool called QCA-LG generates an automatic layout of simple combinational circuits by reading the net-list produced by synthesis tools. QCA- LG generates an equivalent QCA circuit representation of the input net-list and then computes the QCA-cell properties and their coordinates based on that representation. It then writes all the data to a file following the QCADesigner cell definition. This file can then be simulated using QCA Desginer simulator. Although the focus of the research presented in this thesis was essentially not to create a tool, the analysis needed for this work led to development of a simple but efficient logic synthesis and layout tool. It follows the same methodology, of generating QCA-cell data for whole QCA design and writing them to a file, as QCA-LG but uses QCA-cell data of input macro-cells as building blocks.

The main focus of this research is to study the trade-offs in logic implementation using regular structures in QCA domain. In particular, the goal is to compare the single output logic implementations using Shannon lattices with PLAs for area, latency and throughput using QCAs. The term regular structures or regularity in context to this thesis implies that no routing or specific placement process is needed at the layout level to connect modules used for logic implementation. In other words, regular structures should

enable the generation of complete QCA layout for a logic function simply by replicating and abutting a QCA structure in a tile-based fashion. This condition applies to both Shannon-Lattice and PLA layouts. The choice of regular structures, Shannon-Lattice and PLA, forthis thesis was based on the fact that these two structures are the most common and simple regular structures for logic realization. The simplicity of these structures is also favored by the number of QCA structures needed to be replicated to create each type of layout. The QCA-Shannon-Lattice requires only a QCA-multiplexer as a basic structure and QCA-PLA requires two basic structures: AND-plane and OR-plane structure. These structures and their use are discussed in detail in section 4.4 of this thesis. The reasoningbehind the consideration of only single output functions in this thesis owes to their simpler logic mapping to both Shannon-Lattice and PLA. The extension of PLA to multi-output is easier than Shannon-Lattice because generating multi-output Shannon- Lattice would require several optimizations. The implementation of such optimization algorithms for Shannon-Lattice in software tool, developed in this thesis, would becomplicated and is out of the scope of this research work. A study comparing single output functions when realized using CMOS Shannon-Lattice and PLA has already been presented. This goal involves generating QCA layout for different logic functions using both Shannon lattices and PLAs which can then be simulated with QCADesigner. Due to the fundamental differences in QCA and previous semiconductor-based technologies, wemay need to re-evaluate the designs and established studies for silicon based technologies such as one presented in differently. There are no similar previous studies related to this work that would compare any of: area, latency and throughput. The closest published research is the reliability comparison of PLA and custom logic implementation of a QCA adder. The authors of claim that smaller component requirements of custom logic make them more reliable than regular designs assuming that the componentsused to build each circuit are faulty.

2. LITERATURE REVIEW

NOVEL METHODOLOGY TO VALIDATE DUTS USING SINGLE ACCESS STRUCTURECHANDRA SHAKER PITTALA; J. SRAVANA; G. AJITHA; P. SARITHA; MOHAMMAD KHADIR; V. VIJAY; S. CHINA VENKATESWARLU; 2021 5TH INTERNATIONAL CONFERENCE ON ELECTRONICS, MATERIALS ENGINEERING & NANO-TECHNOLOGY (IEMENTECH)

Conventional shift-based scan chains have the drawback of peak power consumption which is reduced by the proposed single cycle access test structure for logic test. With the reduction of this power consumption the activity during shift and capture cycles have been achieved. In addition, more accurate circuit behavior can be achieved even at stuck-at and at-speed tests using the proposed methodology. Thereby it accomplishes close proximity to the functional mode during higher frequency operation tests. By using the proposed design minimum number of test cycles can be gained to the existed literature. It is observed that test cycles per net is below 1 for larger designs when tested for simple test pattern generator algorithm without test pattern compression. Has the advantage of autonomous of the plan estimate conjointly gives an extra on-chip investigating flag permeability for each enrols. It is in reverse congruous to the standard full check plans and with a minor improvement existing test design generators and test systems can be utilized conjointly talked about for the arrangement of including built-in self-test (BIST) and gigantic parallel check chains with the proposed plan. The design and implementation of single cycle access test structure for logic test is functionally verified using Vivado. The pre layout and post layout synthesis and its physical design are performed using cadence Genus and Innonus tools respectively, with the optimized area, power, and delay.

ENERGY EFFICIENT DECODER CIRCUIT USING SOURCE BIASING TECHNIQUE IN CNTFET TECHNOLOGY CHANDRA SHAKER PITTALA; M. LAVANYA; V. VIJAY; Y. V. J. C. REDDY; S. CHINA VENKATESWARLU; RAJEEV RATNA VALLABHUNI 2021 DEVICES FOR INTEGRATED CIRCUIT (DEVIC)

VLSI technology is essential for chip fabrication, and 3 to 8 decoder circuits are used in electronic gadgets; consistency of design, small, fast, in this proposed circuit, 3 to 8 decoder is implemented using 20nm CNTFET technology. 3 to 8 decoders are the key segments in some real-time applications. For the most recent couple of years, the minuscule size of MOSFET, which is under many nanometers, made some operational issues, for example, expanded entryway oxide leakage, intensified intersection leakage, high sub-limit conduction. The proposed model is recreated utilizing Cadence virtuoso with 20nm CNTFET nodes. This technique has some drawbacks as for further improvement introduced a top-gated structure CNFETs. The first is a metal contact, the nanotube on the top was minimal contact to the CNT, and the contact area is very small. A Schottky barrier forms at the metal-semiconductor interface is due to the semiconducting nature of the CNT increase the contact resistance. The second is due to back gate device geometry as the switching of the device on and off was made difficult at low voltage due to thickness, and the fabrication process led to poor contact between the gate dielectric and CNT To increase the device performance, CNFET has designed with a top-gated structure. The structure is made by using a carbon nanotube on the oxidized wafer. Each nanotube is located via atomic force microscopy. High-resolution beam lithography is used to isolate the source and drain contacts. At the top of the nanotube, a thin top-gate dielectric is deposited using atomic layer deposition or evaporation. Eventually, the top gate contact on gate dielectric.

BIASING TECHNIQUES: VALIDATION OF 3 TO 8 DECODER MODULES USING 18NM FINFET NODES MAY 2021 CHANDRA SHAKER PITTALA,M. LAVANYA,M. SARITHA,VALLABHUNI VIJAY,S. CHINA VENKATESWARLU,RAJEEV RATNA VALLABHUNI CONFERENCE: 2021 2ND INTERNATIONAL CONFERENCE FOR EMERGING TECHNOLOGY (INCET)

In this article, a low leakage power and high speed decoder for memory cluster application and proposed modern four strategies is proposed. But the decoder parameters of 3 to 8 decoders designed at 20 nm FinFET nodes using Cadence Virtuoso. In this research paper, we planned a low leakage power and high speed decoder for memory cluster application and proposed modern four strategies. In this paper, the collation of source predisposition decoder, source coupling decoder, body bias decoder and cluster decoder are planned and analyzed for memory cluster application. The plan is recreated utilizing Cadence virtuoso with 20nm innovation. The parameters of 3 to 8 decoders designed at 20 nm FinFET nodes using Cadence Virtuoso. The proposed decoder design is only analyzed for memory cluster applications and may not be suitable for other applications. - The design is simulated using Cadence Virtuoso with 20nm technology, and the results may vary for different technologies or tools. - The paper does not provide a comparison with other existing decoder designs, making it difficult to evaluate the effectiveness of the proposed design. - The paper does not discuss the cost or complexity of implementing the proposed design, which may be a limiting factor for practical applications. Proposing a low leakage power and high-speed decoder design for memory cluster applications. - Introducing four strategies for designing the decoder: source predisposition decoder, source coupling decoder, body bias decoder, and cluster decoder. - Analyzing the proposed design using Cadence Virtuoso with 20nm technology and evaluating its performance in terms of power consumption, delay, and area. - Demonstrating the effectiveness of the proposed design in reducing power consumption and improving speed compared to existing decoder designs. - Providing insights into the design considerations and trade-offs for decoder design in memory cluster applications.

REALIZATION OF 8 X 4 BARREL SHIFTER WITH 4-BIT BINARY TO GRAY CONVERTER USING FINFET FOR LOW POWER DIGITAL APPLICATIONS TO CITE THIS ARTICLE: P. ASHOK BABU ET AL 2021 J. PHYS.: CONF. SER. 1714 012028

Barrel shifter architecture is well known for bit manipulation in a single clock cycle. Due to its various operations and advantages, it is most likely used in the Arithmetic logic unit of every processor. Gray code is also known as reflective code which is widely used in digital communication for the purpose of error correction and error detection. In this project, an 8 x 4 barrel shifter is designed which is further connected to 4-bit binary to gray code converter. The barrel shifter is cascaded with binary to gray code converter so that this combination can be useful for the application of encryption of binary data in digital communications. It is designed in cadence virtuoso tool using FinFET technology at 18 nm node. The simulation results proves that the power consumed by the proposed design with FinFET technology is 11.92% less when compared with the conventional design with MOS transistors. Hence, this design can be used in application of low power digital communications. The functionality testing and verification is done using cadence virtuoso tool. An Arithmetic logic unit in a processor performs various arithmetic operations like addition, subtraction, multiplication and logical operations like AND, OR etc. Most of the operations require only operands, but few operations require sub-modules along with operands. For example, multiplication operation is done by multiplying of data using AND gate and addition of partial products using full adders or half adders. It also requires a shifter to shift partial products so that they can be added in correct format. Hence these modules play an important role in characterizing the performance of processors.

STATIC RAM MEMORY (SRAM) CIRCUITS AND ARCHITECTURES: A TUTORIAL AND SURVEY

In this system to design SRAM circuits and architectures, with an emphasis on high-capacity SRAM. First, to motivated discussion by showing how SRAMs can be applied to packet forwarding in network routers. At the circuit level, reviewed the two basic CMOS cells, namely the NOR cell and the NAND cell. Also shown how the cells are combined in a match line structure to form a SRAM word. explored the conventional precharge-high scheme for sensing the match line, as well as several variations that save match line power including low-swing sensing, the current-race scheme, selective precharge, pipelining, and current saving scheme. We have also reviewed the conventional approach for driving search lines, and the power-saving approaches which eliminate the search line precharge or employ hierarchical search lines. At the architectural level, we have reviewed three architectures for reducing SRAM power, namely bank-selection, pre-computation, and dense encoding. Finally, have presented our views of future development in the SRAM field.

3.EXISTING METHODOLOGY

QCA Cell
Cell-to-Cell Response
QCA Wire
QCA Wire Fan-out
QCA Gates
Majority, AND OR Gates
QCA Wire Crossing
QCA Clocking
QCA Clocking Architecture
Continuous clocking

4. PROPOSED METHODOLOGY

The CMOS technology has progressed to such smaller device geometries that the probabilities of variations in the manufacturing process are high. These factors result in the actual layout pattern that is different from the ones produced by the CAD tool. Regularity is a feature that can be employed to mitigate some effect of the variability. It can provide higher confidence in fabrication done by replicating layout pattern designed using CAD tool. Regularity improves the predictability of the physical implementation and allows for more accurate circuit analysis. Regularity is one of the design-for-manufacturability techniques exploited to some extent by the use of standard cells in CMOS. With small device size, exploiting regularity with regular designs is also significantly important in the QCA technology. As mentioned in the previous sections, the regular structures chosen for this study were the single output Shannon lattice and PLA. Any function minimized into a sum-of- products (SOP) form can be directly mapped to a PLA. PLAs do not require the placement and routing process as is the case with standard cell designs. Similarly, the Shannon lattice for a Boolean function is created by repeatedly applying the Shannon‟s expansion to the function. Each level can then be mapped on to an array of multiplexers or pass-transistors. The inputs of the multiplexer at a higher level are directly driven by the output of multiplexer at the immediate lower level. Thus, the whole Boolean function can be synthesized to a lattice of multiplexers abutted together without the need for placement and route processes.

5. PROPOSED IMPLEMENTATION

5.1 SIGNAL SYNCHRONIZATION

Even though, the signal synchronization is a challenge in circuit implementation in previous technologies as well, it is the granularity of the synchronization in QCA which leads to bigger complications. In traditional technologies, the signals values may notbe consistent with the expected values mainly due to the following two reasons (ignoring the second order effects like interconnect capacitance and cross-talk): (i) the timing requirements across the delay elements are not met at circuit implementation level or (ii) the signals go out of synchronization due to misplaced delay elements at the logic or architectural level. If these two conditions are satisfied, then the wire layout should not affect the information transmission. But in QCA technology, signal synchronization is required at the wire layout level due to the nature of signal flow in QCA. The signal flowin QCA is determined at the layout level by the clocking structure since a group of cells in a particular clocking zone acts as a delay element. This behavior can be observed by considering AND gates in both QCA and CMOS with signals routed to their inputs. AND gate in CMOS with buffered inputs and output. As long as the timing requirements of the delay elements E1and E2are met, the output Outwould produce the correct value of A& Birrespective of the layout of input and output wires. The incorrect clocking zone assignment for an equivalent circuit in QCA. The signals on which ANDoperation is to be performed should be in the same clocking zone when they reach the input of the gate. This also implies that a wire transmitting a signal should not violate the clocking zone phase-cycle-order, i.e., *Hold* -› *Latch* -› *Relax* -› *Release*. In other words, all the paths in the circuit should follow this order from input to output. In this particular case of the AND gate, the signal reaches input B quarter a cycle later than the signal reaching input A. Thus the output of the ANDgate is not reliable.

5.2 WIRE LATENCY

In traditional technologies, the latency of short wires is primarily governed by the material properties like resistance, capacitance etc. and likewise the latency of a short QCA wire is defined by the switching time of electrons between quantum dots in a cell. So, for short wires in both technologies, the latency depends on the underlying materials. However, the long QCA wires require them to be divided into multiple clocking zones for signal integrity. Then the latency of the wire becomes the function of the clocking structure i.e. total number of clocking zones that a long wire has been divided into, assuming that the frequency of clocking and electron switching is the same for both short and long wires. A long wire divided into clocking zones is equivalent to back-to-back D flip-flops and thus dividing a wire into more clocking zones than required for maintainingsignal integrity, is equivalent to adding more D flip-flops in back-to-back fashion. In such a case, it is not difficult to observe that a wire would require more clock cycles to transfer data from input to output. The presents examples of assigning the clocking zones to a wire, each cell is placed

in a different clocking zonewhich accounts for a total of ten clocking zone for the wire i.e. it would take ten quarter- clock-cycles or 2.5 clock-cycles from an input IN to transfer to Out. The provides a better solution where two cells are grouped in one clocking zone thus giving a total of four clocking zones for the wire which would take five quarter-clock-cycles for information transfer. The clocking zone assignment inefficient compared to assignment in is simply used as an example here and does not necessarily show the best clocking assignment, because more number of cells in wire can potentially be grouped together in one clocking zone giving a lower number of total clocking zones. In fact, in this particular example all the cells could possibly be assigned only one zone since the number of cells is small. In such a case, the information transfer from input to output would only take a quarter-cycle. However, as the number of cells in a wire increases, there is an upper bound on how many cells can be grouped in one clocking zone. This problem is discussed in a later section.

5.3 BASIC GATES AND LOGIC SYNTHESIS

In previous technologies, the logic circuits were generally defined in SOP or POS form and implemented using AND OR gates. In QCA, the logic primitives are majority gate and inverter. The authors in proposed a Boolean algebra based interpretation to convert the sum-of-product expressions into the reduced majority logic. Their results show that synthesizing logic into majority gates for QCA implementation results in smaller circuits than implementing QCA circuits based on their SOP or POS representations.

5.4 WIRE LENGTH

As in CMOS/silicon designs, the long wires present concerns in QCA technology as well. In semiconductor domain, the long wires are provided gain using repeaters/buffers to restore the signal strength and also to maintain rise-fall times. A long QCA wire also requires similar treatment in term of power gain. The power gain in QCA wire is provided by the clock. According to and, as the number of cells in a clocking zone increases, their successful switching becomes less reliable. It is, therefore, desirable that number of cells in a wire in a clocking zone is kept to minimum. Readers are encouraged to refer to for a detailed reasoning of the subject matter. Some clocking strategies have been proposed to deal with this issue.

5.5 WIRE LENGTH AND CLOCKING STRATEGIES

To alleviate the problem of wire length, other proposed clocking mechanisms are presented in this section. The PLA design used in this thesis also has long wires and thus it is important to gain the understanding of these schemes since similar scheme has been used for PLA clocking.

5.6 QCA CIRCUITS

Having built a foundation about the basics of QCA and the QCA circuit design considerations in previous sections, this section presents example QCA circuits. This section also shows the circuits which are used as standard library macro-cells to generate complete regular layout by the layout tool developed in this thesis. QCADesigner simulator was extensively used in this research work for designing and simulating the circuits. It is very important to note that the QCA circuits or their clocking assignments illustrated in this section may not necessarily represent the best implementation for a particular circuit. However, the designs presented below are chosen, from a pool of other designs considered and simulated using QCADesigner tool, based on following five design-constraints:

An acceptable switching behavior and signal level of important QCA-cell at key positions in the circuit.

A minimum size/area and number of required clocking zones when simulatingwith QCADesigner while satisfying constraint 1.

A minimum array of three QCA-cells in one clocking zone and maximum definedby constraint 1.

A minimum cell spacing of two cells between two wires satisfying constraint 1.

A minimum number of QCA-cell in the design while satisfying the aboveconstraints.

6. LAYOUT GENERATOR TOOL USING REGULAR CELLS

6.1 MOTIVATION FOR LAYOUT SOFTWARE

This research work presents an analysis on the performance/area trade-offs in logicrealization using Shannon lattice and Programmable-Logic-Array (PLA) in QCA for single output. As mentioned in the introduction of this thesis, only single output functions were considered due to their simplicity and ease of layout tool development for them. Performing the study needs creating and simulating QCA layout of different Boolean functions in both Shannon lattice and PLA. This process is simple when number of variables in the Boolean functions is small but as this number increases, it becomes a tedious task to perform a manual layout of whole design, define input-output cells and assign clock zones. An additional step of complexity is incurred when mapping the logic function to Shannon lattice which is the decomposition of the input Boolean function into its equivalent Shannon lattice representation. As a part of this thesis, a tool was developed in C programming language which accepts Boolean function in simple logic equation form or *blif* format and generates the desired Shannon lattice or PLA layout. It also performs the decomposition of Boolean function into Shannon lattice using simple algorithms. Even though the basic macro-cell can simply be replicated to generate the whole layout and bigger designs can be studied based on macro-cell properties, it is still worthwhile to develop such tools in order to analyze the consistency in the behavior of bigger circuits with macro-cells. This type of analysis is more important in a technology. where the state of a cell is affected largely with respect to the type and location of its neighbors. In addition, this tool provides the flexibility of using different designs of macro-cells to generate the layout which can be used to compare the behavior of varied layouts. In following section, the tool's structure and algorithm for generating the layout files are described. The tool's output layout file can be simulated in QCADesigner simulator.

6.2 LAYOUT FILE GENERATION FLOW

The objective of the tool is to produce a complete Shannon Lattice or PLA layout for the input Boolean function using the cells. The tool reads the configuration file that contains the Boolean function and other parameters (discussed later) to generate the layout. The Boolean function can either be directly specified in the configuration file as Boolean expression or converted from *blif* format into equivalent Boolean expression using the tool. The converted Boolean expression, however, needs to be manually added to the configuration file. If the input Boolean function is not in it minimized form, it is minimized using *ESPRESSO* minimize software. The following arethe inputs to the tool:

Boolean Function *blif* format: converts the function into Boolean expressionfor config-file.

Configuration File: contains the Boolean function and other parameters.

QCA Multiplexer Cell Layout File: used to generate the layout for ShannonLattice.

QCA AND- and OR-Plane Cells Layout File: used to generate the QCA PLAlayout.

The output of the tool is a. qca file containing the layout information which can then be simulated in QCADesigner. The overall high level view of layout generation flow

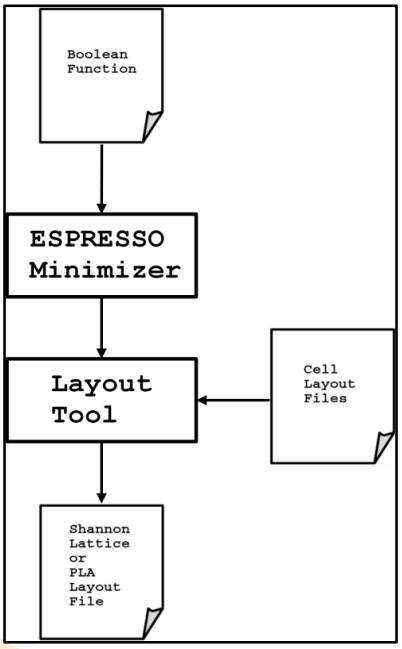


Figure: 1 Layout-generation flow

The detailed flow from defining Boolean function to QCADesigner simulation is shownbelow:

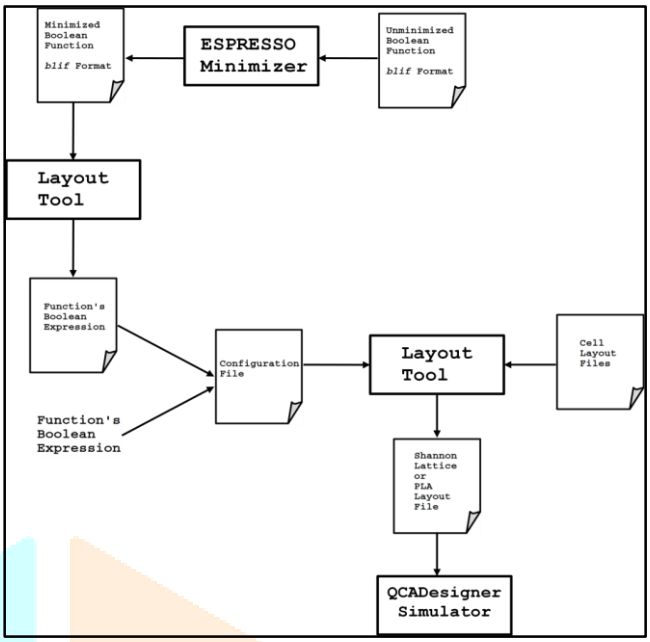


Figure: 2 Detailed layout-generation and simulation flow.

6.3 LAYOUT GENERATOR ALGORITHM

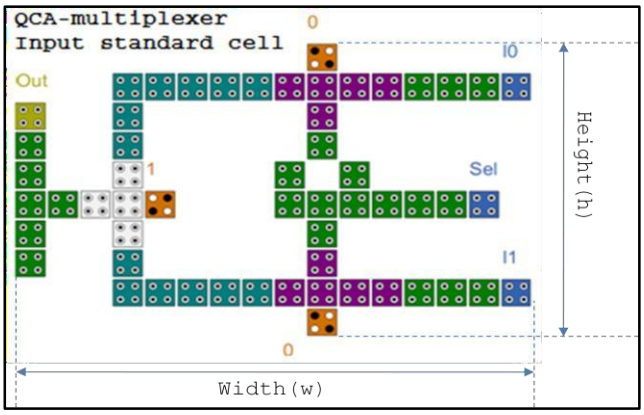
The basic algorithm for generating, either Shannon Lattice or PLA, layout is to read QCA-cell data from the input macro-cell files and, since the layout is regular and properties of all the QCA-cells in the final layout can be computed based on the characteristics of macro-cells, generate all QCA-cells for the final layout and write the QCA-cell data to a file to be simulated in QCADesigner. However, the series of steps that the layout-tool goes through is different between Shannon-Lattice and PLA layout. This is because of the fact that creating a Shannon-Lattice also involves the decomposition of the Boolean function and creating the lattice diagram. A Boolean function can be directly mapped to the PLA without any decomposition.

7. ANALYSIS AND RESULTS

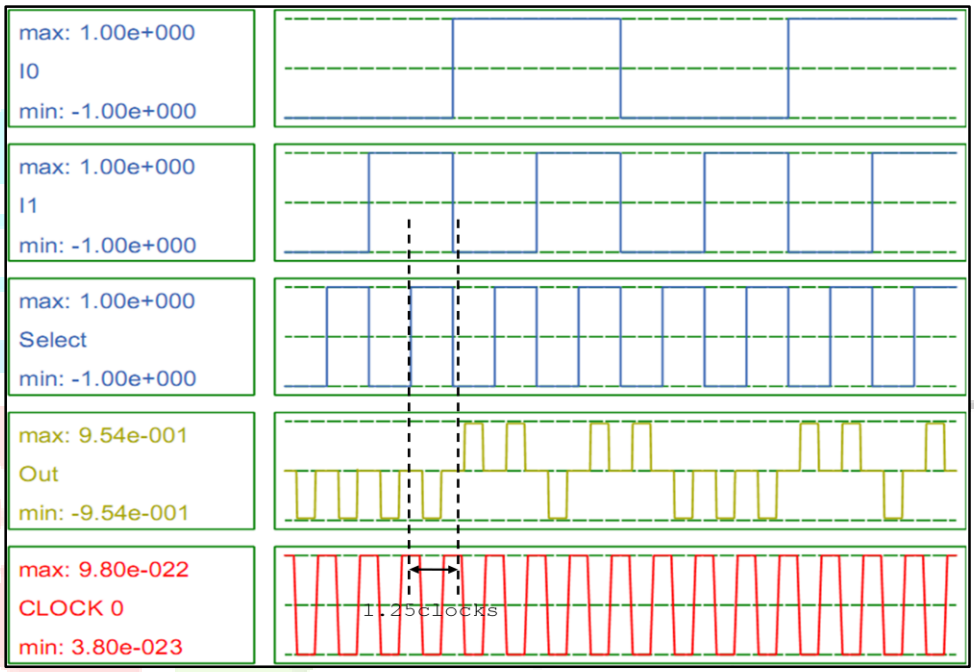
7.1 MACRO-CELL CHARACTERIZATION

Both QCA-PLA and QCA-Shannon-Lattice layout, presented in this thesis are generated using macro-cells as a basic element of the whole design. Thus, it is natural to characterize these macro-cells for area, cell-density and latency. As a reminder, these macro-cells were designed with design-constraints laid. All simulation was performed using QCADesigner with Bistable Approximation Simulation Engine for 12,800 – 600,000 number of samples with 100 – 500 iterations per sample on a computer system with Windows 7 OS running Intel Corei7 CPU and 8GB of RAM. The layout files were generated using a computer system with 64-bit Ubuntu OS, Intel Corei7 CPU and 8GB of RAM. It advised to use the layout tool on a 64-bit OS system with large memory as this one because some issues were observed on systemswith smaller memory.

7.1.1 QCA-MULTIPLEXER MACRO-CELL



(a) QCA-multiplexer macro-cell.



(b) Simulation waveforms: Selto Outlatency.

Figure :3 Latency computation for QCA-Multiplexer.

Latency: In the QCA-Multiplexer macro-cell, the select signal Sel or its complement are connected to the same majority gates as the inputs I0 or I1. Thus the latency from Sel or any of the two inputs to the output is same. The latency for thiscircuit is 1.25 clock cycles. The latency of this circuit can also be computed by counting the number of clocking zone, from any input to the output, which is five. Since QCA-clock consists of four phases, it would take a quarter of a cycleto move data from one clocking zone to next. Thus, five clocking zones would take five quarters of a cycle i.e. 1.25 clocks. The latency for the whole design is computed differently when latencies from inputs to output are different. In such a case, the latency of whole design would be the worst-case latency i.e. the latency of the input-output path that takes most clock cycles.

Area: As reported by QCADesigner, the area of QCA-Multiplexer (h x w) shown in Figure 6- 1(a) is 63192.98 nm^2or 0.06μm^2. Total number of QCA-cells in this design is 56, which gives a cell-density of 890 cells/μm^2. The throughput is defined as number of clock cycles between successive output appearances or outputs per clock cycle.

QCA-Multiplexer Macro-Cell	
Number of QCA-cells	56
Worst-case-latency (clocks)	1.25
Throughput (output/clock cycle)	1
Area (nm^2)	62964.00
Cell-density (cells/μm^2)	890

Figure: 4 QCA-Multiplexer macro-cell characteristics.

8. CONCLUSION

The USR designed using QCA technology on the QCA Designer tool to store and shift data in both directions (left and right) using a D flip-flop and 4 to 1 Mux. That helps to minimize power consumption and increase its performance compared with the existing model, VLSI technology. This kind of USR implemented with the help of nanotechnology, and then it evacuates the VLSI in creating chips with transistors and other electronic devices in the design of USR. That can be done when nanotechnology comes into the electronic field; then, many inventions may be made and improve this project and be applied to get product-type results. From the obtained results obtained, we can conclude that by using the QCA Designer tool, we can design USR by using QCA technology and can operate in parallel-in-parallel-out mode and make efficient and has fast response when compared to the VLSI model of USR.Although this works adds to the knowledge base of scientific community, the study has some limitations. One major limitation of this comparison is that non-symmetric function were not included due to which QCA-Shannon-Lattice came out to be a clear winner in each field. This is because the current lattice diagram generation algorithms implemented in the software can only efficiently handle symmetric functions. For future work, the algorithms in the tool for logic synthesis of Boolean function to Shannon- Lattice should be replaced with some advanced algorithms as presented. Thetool currently has limitations on the size of Boolean function that can be handled by it to generate layout. It can be improved by refining the code to use the memory efficiently. In future, the tool can be extended to work with the function net-list and generate layouts for sequential circuits using PLA and memory.

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