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LOW PASS CONTINUOUS TIME DELTA SIGMA MODULATOR

P. Shivani, Student, M E, Osmania university

Md . Misbahuddin, Assistant professor, Electronics and communication engineering, Osmania university

ABSTRACT : High speed and high resolution analog-to-digital converters (ADCs) are in greater demand due to the quick development of fast digital signal processors constructed utilizing very-large-scale integration (VLSI) technology. These ADCs can be used in fabrication processes and are designed for digital circuits and systems. The ADCs are the main bottleneck in the majority of mixed-signal designs since the scaling of VLSI technology significantly restricts the dynamic range that is available for the interface of analogue and digital signals. One of the ADC architectures, delta-sigma oversampling ADCs, provide an ideal balance between circuit complexity, cost, and power consumption. Analogue components with poor precision can nonetheless deliver high accuracy. The Sigma-Delta (SD) ADC is one of the best ADC topologies for lowvoltage and low-power applications because its loop-filter is its main design bottleneck. The construction of a low pass continuous time delta sigma modulator is the main goal of this effort. We'll create a method for analyzing and synthesizing lowpass continuous time sigma-delta$\Delta\sum$ modulators. Using continuous-time filters and this technique, it is possible to create $\Delta\sum$ modulators from discrete-time topologies. Utilizing a discrete simulator and discretizing a continuous-time model are the foundations of the analysis technique.

Keywords :Continous time $\Delta\sum$, loop filter .

Introduction

Pulse-density modulation (PDM), also known as delta-sigma modulation, is the conversion of an analogue voltage signal into a pulse frequency or pulse density. Given that the timing and sign of the pulses can be determined, it is quite simple to create, transmit, and accurately renew a series of positive and negative pulses that represent bits at a known constant rate at the receiver. Such a series of pulses from a delta-sigma modulator can be used to accurately reproduce the original waveform. Contrarily, if the analogue signal were to be transmitted directly without being converted into a pulse stream, all background noise in the system would be added to it, degrading the signal's quality. An alternative to pulse-code modulation (PCM), which samples and quantizes to a multi-bit code at the Nyquist rate, is the use of PDM as a signal representation.

A pulse stream is produced by a delta-sigma or other pulse-density or pulse-frequency modulator in which the frequency of the pulses, f, in the stream is proportional to the analogue voltage input, v, such that f = k . v, where k is a constant for the specific implementation. The integral of v is monitored by a feedback loop, which subtracts from it when the integral waveform crosses a threshold, T, signalling that the integral has increased by the specified amount Δ . As a result, the combined waveform saw tooths between T and T - Δ . A pulse is added to the pulse stream at each step.

It is not unexpected that analogue to digital converters (ADCs) today use a variety of approaches to achieve faster processing times and higher resolutions than their simpler predecessors. Here's where the Delta-Sigma $\sum\Delta$ ADC comes in, which combines a few methods like oversampling, noise shaping, and digital filtering. That's not to say that you need multiple chips to do this; nowadays, single chip Delta-Sigma ADCs are tiny and reasonably priced. Sometimes they are referred to as Sigma-Delta $\sum\Delta$ merely for the purpose of confusion, a move I support as there aren't currently enough sources of misunderstanding in the engineering community.

To accomplish analog-to-digital conversion, the delta-sigma modulation approach combines filtering and oversampling. The noise from a low resolution quantizer is first bent away from the signal band before being removed by filtering. We are interested in the use of a continuous time filter inside the delta-sigma loop for high-speed conversion since it can be used to radio receivers and other high frequency circuits. Another benefit of continuous time modulators is that they have less switching noise and built-in antialiasing.

The spectrum of a series of output bits produced by a time-domain simulation of the modulator is used to determine an $\Delta\sum$ M's performance. It is then characterised using some common ADC performance metrics, like DR and SNR, while leaving out others, like DNL and INL, which have no relevance to $\Delta\sum$ Ms. Oversampled converters typically require many more output samples than a Nyquist rate ADC before performance can be assessed, so how to actually carry out the time-domain simulation is a subject of major importance in oversampled converters.

THE ΔΣ MODULATOR :

The ΔΣ modulator is the ΔΣ ADC's brain. It is in charge of digitising the analogue input signal and lowering low-frequency noise. At this point, noise shaping is implemented by the design, which causes low-frequency noise to be pushed up to higher frequencies where it is outside the band of interest. One of the reasons ΔΣ converters are suitable for low-frequency, high accuracy measurements is noise shaping.

An analogue voltage with time variations serves as the input signal to ΔΣ the modulator. This input-voltage signal was largely used by the early ΔΣ ADCs for audio applications where AC signals were crucial. Conversion rates now include DC signals as focus shifts to precision applications. A sine wave's single cycle will be used as an example in this lecture.

Figure 1. Block diagram of ΔΣ ADC

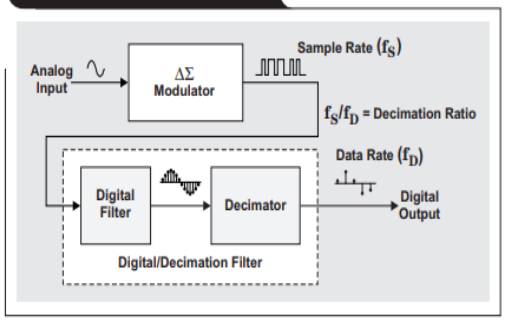
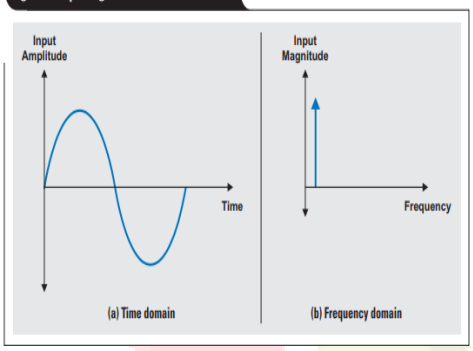


Figure 2. Input signal to the ΔΣ modulator

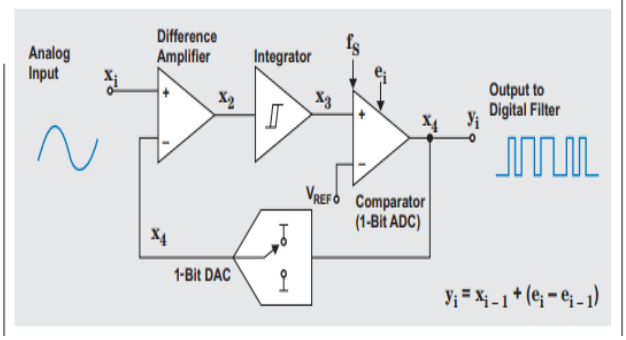


He aforementioned figure displays a single sine wave cycle as the input to a DS modulator. Voltage amplitude in this single cycle varies throughout time. The time-domain signal in Figure 2a is depicted in frequency-domain form in Figure 2b. The curve in Figure 2b, which looks as a spur or a straight line, is a representation of the continuous sine wave in Figure 2a.

The ΔΣ modulator can be viewed in two different ways: in the time domain (Figure 3), or in the frequency domain (Figure 4). The first-order ΔΣ modulator's workings are depicted in the time-domain block diagram of Figure 3. A fast, single-bit, modulated pulse wave is created from the analogue input signal by the modulator. More significantly, the frequency analysis in Figure 4 demonstrates how the modulator influences the system's noise and makes it possible to produce a higher-resolution result.

The ΔΣ modulator depicted in Figure 3 samples the input signal numerous times to create a stream of 1-bit codes. Together with the modulator's 1-bit comparator, the system clock implements the sampling rate, f_s.

Figure 3. First-order ΔΣ modulator in the time domain



In this way, the ΔΣ modulator's quantizing action is generated at a high sample rate that is sync'd with the system clock. Like all quantizers, the ΔΣ modulator generates a stream of digital values, in this case a 1-bit stream, that correspond to the voltage of the input. The input analogue voltage is therefore represented by the ratio of ones to zeros. The ΔΣ modulator has an integrator, which is uncommon in quantizers and has the effect of sculpting the quantization noise to higher frequencies.

As a result, the noise spectrum at the modulator's output is not flat.

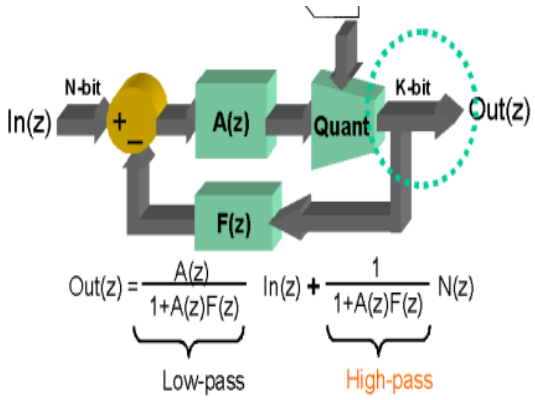
The 1-bit digital-to-analog converter (DAC) output and analogue input voltage are distinguished in the time domain, producing an analogue voltage at x_2. The integrator receives this voltage and outputs a change in direction, either positive or negative. The amplitude and sign of the voltage at x_2 determine the slope and direction of the signal at x_3. Depending on its initial state, the comparator's output changes from negative to positive or from positive to negative when the voltage at x_3 equals the comparator reference voltage. The 1-bit DAC and the digital filter stage, y_i, both receive the comparator's output value, x_4, at the same time. The 1-bit DAC reacts by altering the analogue output voltage of the difference amplifier whenever the comparator's output changes from high to low or vice versa. This results in a different output voltage at x_2, which causes the integrator to move anticlockwise. This time-domain output signal represents the input signal as pulse waves at the sampling rate (f_s). The averaged output pulse train has the same value as the input signal.

The time-domain transfer function is also shown in the discrete-time block diagram in Figure 3. The converter's quantization noise is created by the 1-bit ADC's coarse, 1-bit output code, which digitises the signal in the temporal domain. The modulator's output, e_i - e_i - 1, is equal to the input plus the quantization noise. The quantization noise, as shown by this formula, is the difference between the most recent quantization error (e_i) and the prior one (e_i -1).

THE LOW PASS CT DELTA-SIGMA MODULATOR IS BRIEFLY INTRODUCED IN THE SECTIONS THAT FOLLOW.

LOW PASS

Building H(z) from integrators will shape noise away from dc since integrators have poles at dc. Low pass loop filters are used to build **ΔΣ**Ms when the quantization noise has a high pass shape, and these **ΔΣ** Ms are referred to as low pass (LP) converters.



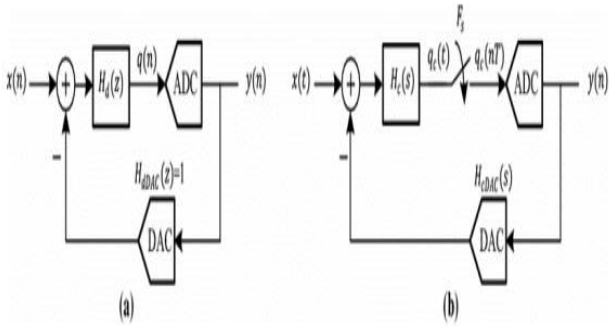
CONTINUOUS-TIME

In the discrete-time (DT) domain, we have been writing the loop transfer function H(z). Discrete-time circuits like switched-capacitor (SC) [Bai96] or switched-current (SI) [Ned95] circuits are how the majority of Ms in the literature are implemented. The loop filter can be constructed as a continuous-time (CT) circuit (s), for instance using transconductors and integrators [Jen95].

DT-to-CT Conversion of Delta-Sigma Modulators

Most delta-sigma designs concentrate on DT implementations before exploring the continuous-time realm. As a result, during the past 20 years, numerous software tools and cutting-edge architectures have been researched to aid in the construction of DT delta-sigma modulators. Therefore, a DT system level build, which is more quicker and simpler, is typically where the design of a CT delta-sigma modulator begins . To meet the performance requirements, including the peak SNR and the ENOB, the DT modulator is synthesised. Then, in order to obtain the equivalent CT modulator, the DT domain to CT domain conversion is carried out.

The impulse-invariant transformation and the Z-transformation are two often employed techniques for the DT-to-CT transformation. This translation can also be carried out using some built-in MATLAB tools. The MATLAB transformation function is employed in this project. To provide a better understanding of the transformation processes, a brief description of the impulse-invariant transformation approach is still provided. The DT and CT modulators' condensed block diagrams are illustrated in Figures 4(a) and 4(b), respectively, for illustration purposes.



The CT modulator's clocked quantizer serves as the link to the DT domain because when the inputs to both quantizers are similar at the sampling moment, both designs' output digital codes and noise performance should be identical. This situation is shown by Equation (1).

$$\mathbf{q(n) \equiv } \left. \boldsymbol{q(t)} \right|_{t=nT_s} \quad \mathbf{(1)}$$

The feedback signals dictate the inputs to the quantizers for the identical analogue input signal. The feedback signal routes for both modulators are depicted in Figures 5(a) and 5(b), respectively, to make analysis easier.

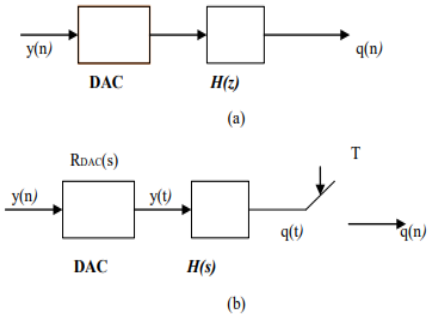


Fig no 5 : Feedback signal path of the (a) DT delta-sigma modulator (b) CT delta-sigma modulator

The y(n) to q(n) transfer functions for both systems must be the same at the sample instants in order to satisfy equation (2). Equation (3) depicts it in the frequency domain.

$$\mathbf{z^{-1}\{H(z)\} = L^{-1}\{R_{DAC}(s)H(s)\}|_{t=nT_s}} \quad \mathbf{(2)}$$

Equation (2) results in the following in the time domain:

$$\mathbf{h(n) = [r_{DAC}(t) * h(t)]|_{t=nT_s} = \int_{-\infty}^{\infty} r_{DAC}(\tau)h(t-\tau)d\tau\,|_{t=nT_s}} \quad \mathbf{(3)}$$

where is the representation in the frequency domain, and $\mathbf{r_{DAC}}$ is the feedback waveform in the time domain.

The above techniques make both modulators' open-loop impulse responses equal at the sampling times, which is why this technique is known as the impulse-invariant transformation. This technique enables the DT loop filter's noise-shaping function to be precisely replicated in the CT loop filter. As a result, both modulators' performances are identical, and the transition is accomplished.

Implementation in MATLAB

The CT ΔΣ M NTFs used in this thesis are created as high pass Chebyshev Type 2 filters. A STF is created as a low pass filter using the numerator of a lowpass Chebyshev Type 2 filter and the denominator of the NTF after an NTF has been
established. All CT ΔΣ used in this thesis have a signal bandwidth of 20 MHz and a sampling rate of 1GHz. The block diagrams for all first order, second order, third order, fourth order, and fifth order CT ΔΣ Ms are described here.

First-Order lowpass CT ∑ΔM

The block diagram of a first-order lowpass CT ∑ΔM built utilising CIFB architecture is shown in Fig. 6. The first order lowpass CT ∑ΔM has a single integrator, as seen in Fig. 6.

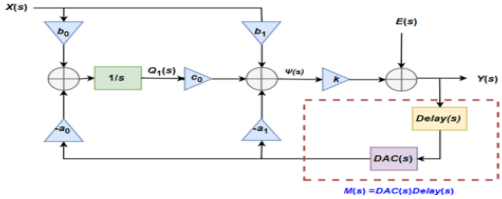


Fig 6 First-order lowpass CT ∑ΔM block diagram

The STF and NTF of the first order lowpass CT ΔΣM illustrated in Fig. 6 can be expressed as by substituting (6.2) into (6.3) and inserting the resulting equation into (6.1).

$$Y(s) = kT(s) + E(s) \quad (6.1)$$

$$NTF(s) = \frac{Y(s)}{E(s)} = \frac{k}{1+a_1KM(s)+a_0c_0KM(s)\frac{1}{s}} = \frac{s}{a_0c_0M(s)+(\frac{1}{k}+a_1M(s))s} \quad (6.2)$$

$$STF(s) = \frac{Y(s)}{E(s)} = \frac{b_1k+b_0c_0k^{1}/_{s}}{1+a_1KM(s)+a_0c_0KM(s)\frac{1}{s}} = \frac{b_1s+b_0c_0}{a_0c_0M(s)+(\frac{1}{k}+a_1M(s))s} \quad (6.3)$$

A high pass Chebyshev Type 2 filter with a cut-off frequency close to the CT M's 20 MHz bandwidth is created to determine the appropriate NTF. The STF is then created as a lowpass filter utilizing the denominator of the NTF and the numerator of a lowpass Chebyshev Type 2 filter. The sampling rate and signal bandwidth for this thesis are 1GHz and 20MHz, respectively.From the MATLAB code we will get this

$$NTF(s) = \frac{s}{s+8.66e08} \quad (6.4)$$

$$STF(s) = \frac{8.66e08}{s+8.66e08} \quad (6.5)$$

The coefficients a_0,a_1 , b_0, b_1, and c in Fig. 5.1 are calculated by comparing equations (6.2) and (6.3) with (6.4) and (6.5), respectively. K is set to 1 in this thesis. The magnitude response of the NTF in (6.4) and the STF in (6.5) is shown in Fig.7

The amplitude response of the NTF for frequencies below 20 MHz is practically significantly less than one, as shown in Fig. 7 , and as a result, the quantization noise will be dampened for these frequencies. Additionally, Fig.7 demonstrates that the STF's magnitude response is roughly one for frequencies below 20 MHz, suggesting that signal frequencies are passed within the bandwidth of the transmission without considerable attenuation .

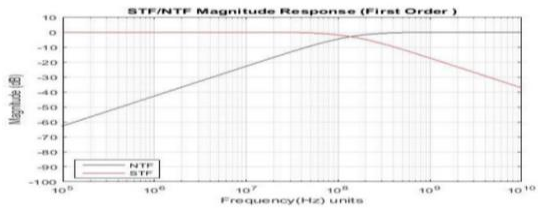


Fig 7 The magnitude response of the NTF and the STF .

For the Higher orders we can find STF and NTF in MATLAB by using this method .

The STF and NTF of Higher orders is as follows

Order		Implementation
1st	STF	$\frac{8.66e08}{s+8.66e08}$
	NTF	$\frac{s}{s+8.66e08}$
2nd	STF	$\frac{0.01523s^2+6.764e17}{s^2+1.155e09s+6.764e17}$
	NTF	$\frac{s^2-2.384e-07s+9.554e15}{s^2+1.155e09s+6.764e17}$
3rd	STF	$\frac{1.736e07s^2+6.603e26}{s^3+1.731e09s^2+1.512e18s+6.603e26}$
	NTF	$\frac{s^3+2.126e-07s^2+1.433e16s+1.147e11}{s^3+1.731e09s^2+1.512e18s+6.603e26}$
4th	STF	$\frac{7.991e-05s^4-5.035e-11s^3+2.278e16s^2-9.782e09s+8.116e35}{s^4+2.467e09s^3+3.062e18s^2+2.229e27s+8.116e35}$
	NTF	$\frac{s^4-4.091e-07s^3+1.911e16s^2-4.727e11s+4.564e31}{s^4+2.467e09s^3+3.062e18s^2+2.229e27s+8.116e35}$
5th	STF	$\frac{1.738e05s^4+2.477e25s^2+7.061e44}{s^5+3.002e09s^4+4.53e18s^3+4.232e27s^2+2.445e36s+7.061e44}$
	NTF	$\frac{s^5+7.332e-07s^4+2.388e16s^3+1.444e12s^2+1.141e32s+2.088e29}{s^5+3.002e09s^4+4.53e18s^3+4.232e27s^2+2.445e36s+7.061e44}$

Table:1 (First , Second , Third , Fourth , Fifth) order Simulated STF and NTF

MODULATOR IMPLEMENTATION AT THE SUBSYSTEM LEVEL

The first order modulator prototype model is provided in this chapter since the sub-blocks employed in this modulator are also used in higher order modulators. The implementation and simulation of sub-blocks at the circuit level that are employed in the construction of modulators of any order are the topics of this chapter. Spectra Simulator is used for simulations while the CADENCE schematic design tool is used for the circuit level execution of the sub-blocks.

CMOS Op-Amp with Two Stage

According to the block diagram, it contains two stages: stage 1 is the differential amplifier, and stage 2 is the common source amplifier.

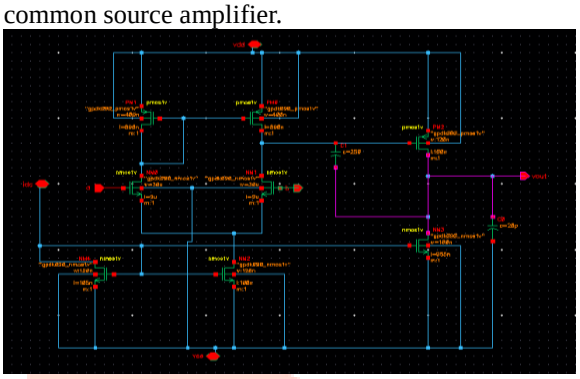


Fig 7 Schematic of Op Amp

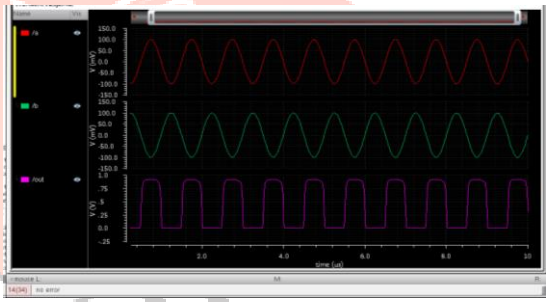


Fig 8 Op Amp Results

When Vdd = 1.25v is given and Input signals as 100 mv with phase of 90 and 0 degrees and opposite magnitude with 1MHz frequency is applied we can observe those results. By using this Op Amp circuit we need to create a Integrator circuit which is as follows as shown in below fig 9 ,

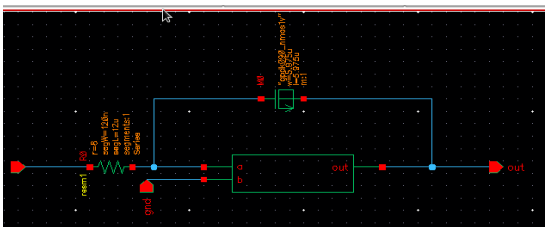


Fig 9 Integrator Schematic

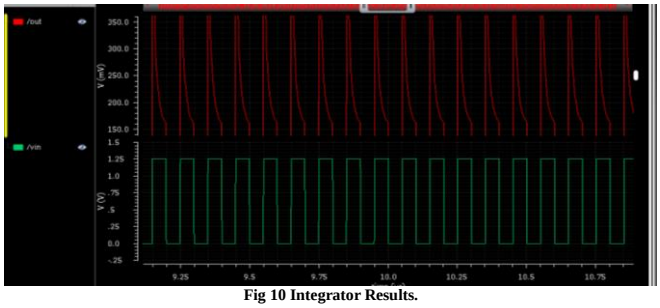


Fig 10 Integrator Results.

Because the integrator produces a pulsed output at half and fourth of the $Vref$ from a square wave input. The simulation ran for 60 ns with a 1.25 Vpp input signal .

Comparator

When two voltages or currents are compared, a comparator switches its output to show which is greater. A circuit with a binary output is called a comparator.

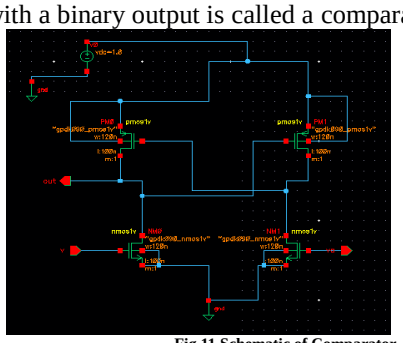


Fig 11 Schematic of Comparator

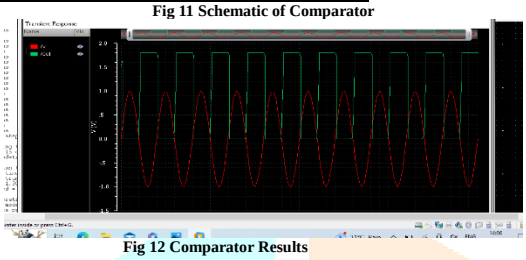
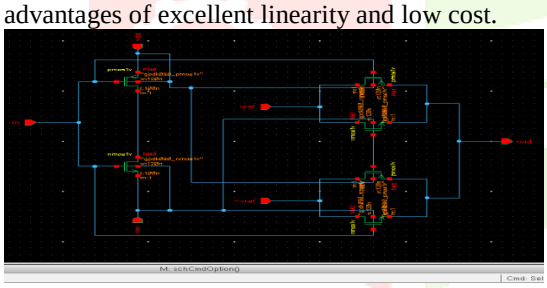


Fig 12 Comparator Results

Digital to Analog Convertor: An oversampling digital-to-analog converter (DAC) with a real 1-bit DAC (i.e., a straightforward "on/off" switch) in a delta-sigma loop running at multiples of the sampling frequency is referred to as a bit-stream or 1-bit DAC. The 1-bit designation is rather misleading because the combination is equivalent to a DAC with more bits (often 16–20). Due to the fact that the majority of processing occurs in the digital domain and 49 requirements for the analogue anti-aliasing filter after the output can be reduced, this type of converter has the advantages of excellent linearity and low cost.



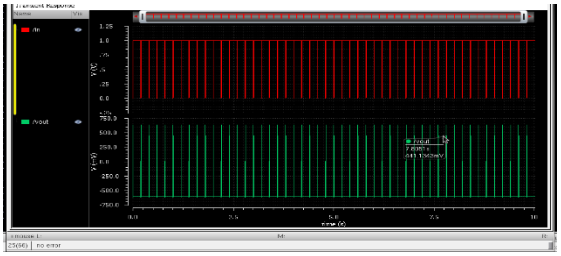


Fig 13 DAC Results

D Latch :A D Latch is inserted after the comparator to produce delayed output and for sampling purposes. The output values of the comparator are changed from (-1.788 V, 1.8 V) to (0, 1.8 V).

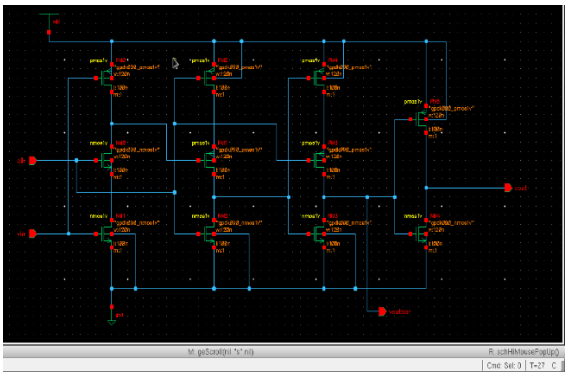


Fig 14 D Latch Schematic

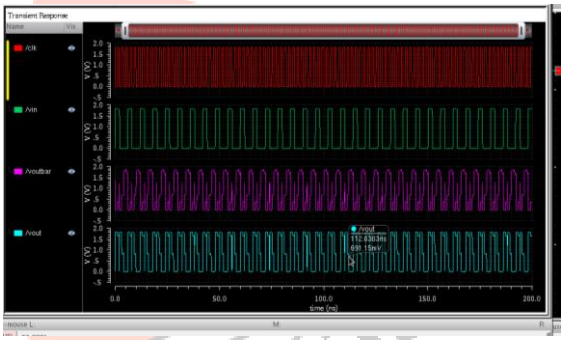


Fig 15 D Latch Results

The input on terminal D is followed onto the output terminal ' $Vout$' and its complement is present on the '$Vout\_bar$' terminal if the clock input transitions to the negative. Up until the clock makes another negative transition, the output is retained. This is visible in Fig. 15 . When the input clock is applied to terminal D, DFF produces a delay equal to ($Tclk$/2). A signal on terminal $Vout$ is in phase with a signal on terminal D, take note.

Summer Circuit : The signal coming from the 1-bit DAC is added to the input signal at the summing amplifier of the sigma delta modulator. The output signal from the DAC and the real input sinusoidal signal are input to a differential pair MOS transistor NM0- NM1 that serves as the summing amplifier. With the aidof this differential pair, the signal from the DAC is added to the input signal.

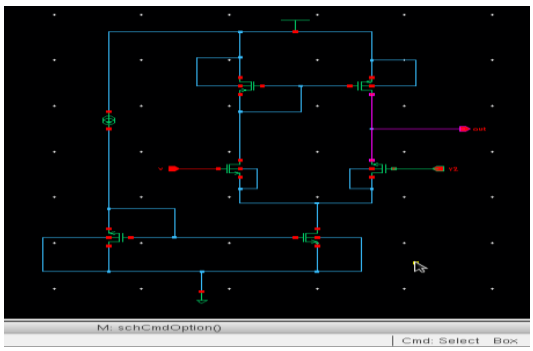


Fig 16 Summer Schematic

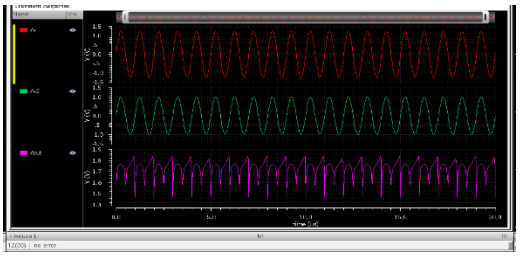
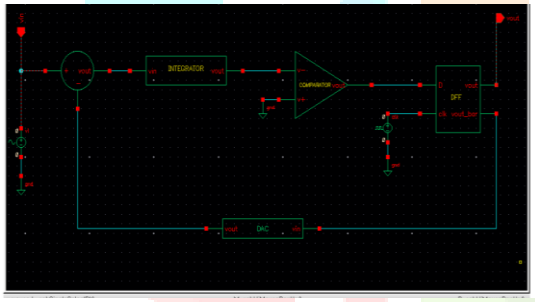
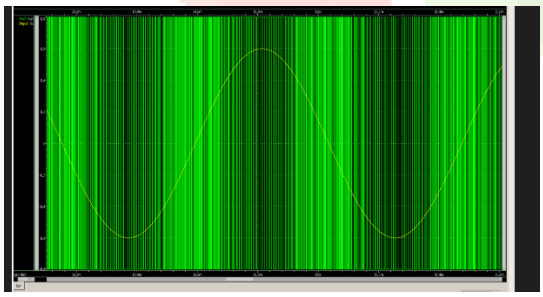


Fig 17 Summer Schematic results

Summary First order sigma delta modulator is created using gpdk 90nm technology in a cadence virtuoso environment to achieve small implementation area. having a peak-topeak input voltage of 0.6 V. The single-ended nature of this design makes it suitable for straightforward applications with acceptable noise performance. The schematic of First order Low Pass Continous time Sigma delta Modulator and its results are presented below.





Conclusion and Future scope .

This Paper provides the STFs and NTFs of CIFB implementations of first, second, third, fourth and fifth order CT ∑ΔMs and also summarizes the desired STF and NTF transfer functions of first, second, third, fourth and fifth order CT ∑ΔMs used in this paper .

A low pass continuous time first order sigma-delta modulator with a bandwidth of 20 KHz was demonstrated in this thesis work. The several design factors that are available at the system level were highlighted, and MATLAB simulations were run in order to derive the loop filter coefficients. The modulator's individual building blocks were each meticulously designed. The modulator and individual blocks were simulated with CADENCE tools.

Future Works :The important areas we may focus on are the different numerical integration techniques and the simulation of one-bit, two-bit, and three-bit first, second, third, fourth, and fifth-order CT Δ∑ Ms using Simulink. Modelling many non-idealities that are connected to the CTΔ∑ Ms would be interesting, including operational amplifier noise, clock jitter, integrator non-idealities, finite DC gain, slew rate, finite bandwidth, amplifier saturation, and trans conductor nonlinearities. The stability of the CT Δ∑ Ms is another important area that needs improvement. Determining the stability criteria and performing a stability analysis of the CTΔ∑ Ms using techniques like analytical root locus would be fascinating. It would be fascinating to study on even higher orders of CT Δ∑Ms since this thesis is only concerned with fifth-order CT Δ∑Ms .

We can also design higher orders of Low pass continuous time delta sigma modulator in Cadence , and also we can design the circuit in Verilog – A and Verilog AMS in Cadence .

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