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IMPLEMENTATION OF 17-LEVEL SYMMETRIC MULTILEVEL INVERTERS

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Abstract: This paper implements a symmetric hybridized cascaded multilevel inverter for 17 level. The symmetric hybridized multilevel inverter topology consists of a modified H-bridge inverter, which results in an increase in the output voltage to five level from the three level by using a bi-directional switch at the midpoint of a dual-input dc source. The proposed topology with the staircase modulation technique has been verified using MATLAB–SIMULINK. The results of the proposed topologies are experimentally obtained for steady state, and the performance of the same is tested under different resistive and inductive load disturbance conditions. The results substantiate that these multilevel inverter topologies are better stabilized during load disturbance conditions with low total harmonic distortion, a lesser number of switches, and increased output voltage levels, and these topologies well suit for renewable energy applications.

Index Terms **- Multilevel inverter; Cascade h-bridge, Hybridized cascade h-bridge, SPWM.**

I. INTRODUCTION

The multilevel inverters have been developed and utilized for higher voltage levels. In achieving higher voltage levels and power levels, hybridized cascaded multilevel inverters (MLI) are proven to be more flexible than conventional topologies[1-5]. Its property can be used to increase the power output of the inverter. Cascaded MLIs are constructed by linking in series output terminals of several H-bridge inverters. It is hence evident that this configuration supports high power levels with the use of low voltage rating components in inverters. In case of a fault in any one of the inverter cells, it can be easily and quickly replaced because of its modularity property Based on converter topology and its domain of application, each modulation technique has its own advantages and disadvantages[6-10]. High power applications utilize a frequency up to 1 kHz. PWM methods based on the carrier are classified into level shifted and phase shifted modulation schemes. Level shift modulation techniques are mostly employed in various applications to generate high-quality output waveforms. The cascaded MLI can be operated in both symmetric and asymmetric configuration[11-15]. In the symmetric configuration, the magnitude of input DC sources is equal, due to which a number of output levels are less in addition to utilizing more number of switches with increased total harmonic distortion (THD). Asymmetric MLI input DC sources are unequal due to which different voltage levels can be generated. By combining such voltage levels more levels can be generated with a lesser number of switches with a consequent reduction in THD.

II. HYBRIDIZED CASCADE H-BRIDGE MLI

This inverter uses several hybridized H-bridge inverters connected in series to provide a sinusoidal output voltage. Each cell contains one hybridized H-bridge and the output voltage generated by this multilevel inverter is actually the sum of all the voltages generated by each cell i.e. if there are k cells in an hybridized H-bridge multilevel inverter then a number of output voltage levels will be 4k+1where as for cascade H-bridge it requires 2k+1 by this we can say how many switches are reduced and how much weight is reduced. This type of inverter has an advantage over the H-bridge and all other types of inverter as it requires fewer components as compared to the H-bridge inverters and all other types of inverter so its overall weight and price are also less.

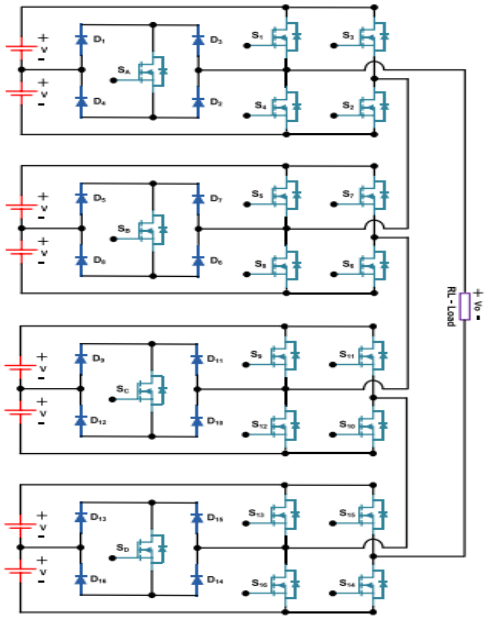

Figure.1: 17 level hybridized cascade h-bridge MIL

The hybridized Cascaded H-bridge multilevel inverter uses switches. It requires less number of components in each level as compared to previous described types. This topology consists of series of power conversion cells and power can be easily scaled. The combination of 5 switches pair in each cell is called hybridized H-bridge. It consists of hybridized H-bride cells and each cell can provide 5 different voltages like zero, positive DC (+1V and +2V) and negative DC (-1V and -2V) voltages. In a single-phase inverter, each phase is connected to a single dc source. Each level generates three voltages which are positive, negative and zero. This can be obtained by connecting the AC source with the DC output and then using different combinations of the four switches. The inverter will remain ON when two switches with opposite positions will remain ON. It will turn OFF when all the inverters switch ON or OFF. To minimize the total harmonic distortion, switching angles are defined and implemented. The calculations for the measurement of switching angle will remain the same.

III. SWITCHING TECHNIQUE OF HYBRIDIZED CASCADE H-BRIDGE

The operation of H-bridge topology can be interpreted in terms of two-stages. In the first stage, the output levels +V1, 0, −V1 is delivered by the association of bidirectional switch to the second leg on H-bridge while in the second stage, the output levels +2V1, 0, −2V1 are generated. The generated 5-level output voltage using symmetric basic hybridized cascaded MLI topology is depicted in Figure.3.2 . The switching states representing the status of the basic MLI are given in Table 1.

Table 1: Switching states of hybridized cascade h-bridge

Output voltage levels	Switching states				
switches	S_1	S_2	S_3	S_4	S_A
+2 V	1	1	0	0	0
+1 V	0	1	0	0	1
0 V	0	1	0	1	0
0 V	1	0	1	0	0
-1 V	0	0	1	0	1
-2 V	0	0	1	1	0

The following section discusses the choice of the number of sources, switches, and output voltage levels. In the symmetric hybrid and asymmetric multilevel inverters, the values of the dc sources are unequal so that number of output levels can be generated using a number of switches. It is assumed that the k_{th} cell is same DC sources.

In the proposed symmetric hybrid multilevel inverter the input DC sources are equal and the inverter equations can be written as follows.

$$V_{d1} = V_{d1} = \cdots\cdots = V_{dk} = V_d \quad (1)$$

The number of levels that can be determined is as follows where m is the no cell and n is the number of dc sources in each cell,

$$N\ Levels = 2mn + 1 \quad (2)$$

The switches can be estimated as .N switch,

$k = 2P_k + 1$ (3)

The maximum output voltage can be estimated as,

$V_o = mnV_d$ (4)

For the proposed asymmetric multilevel inverter the input DC sources are unequal and the equation can be written as,

$V_{d1} = V_1 = V_d$ (5)

Then, the k^{th} cell dc voltage source magnitude is given by

$V_{dk} = (2P_1 + 1).(2P_2 + 1) \cdot \cdot \cdot \cdot (2P_{k-1} + 1).V_d$ (6)

Where k^{th} is the number of cells and P_k is the number dc voltage sources in the kth cell..The number of output voltage levels can be estimated as

. N Levels $= (2P_1 + 1).(2P_2 + 1) \cdot \cdot \cdot \cdot (2P_m + 1)$ (7)

The maximum output voltage estimated is as follows,

$V_o = [(2P_1 + 1).(2P_2 + 1) \cdot \cdot \cdot \cdot (2P_m + 1)] - 1 \ V_d/2$ (8)

The number of switches estimated is .N switch,

$k = 2(P_k + 1)$ (9)

By using the aforesaid equations the no. of switches, the no. of voltage levels and the o/p voltage of H-bridge topologies can be determined.

The 17-level symmetric cascaded H-bridge MLI. In this topology, the operation of every H-bridge is similar to the basic H-bridge topology. In this symmetric inverter, pulses are generated using PWM modulation scheme for obtaining different output voltage levels. The pulses are generated individually and fed to the first, second, third and fourth stage respectively and finally, all

Table 2: Switching state of hybridized cascade h-bridge for 17 levels

V_O	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**0**	**-1**	**-2**	**-3**	**-4**	**-5**	**-6**	**-7**	**-8**
S_1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
S_2	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
S_3	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
S_4	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1
S_5	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
S_6	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0	0	0
S_7	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
S_8	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	1	1
S_9	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0
S_{11}	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1
S_{12}	0	0	0	0	1	1	1	1	0	1	1	1	1	1	0	1	1	1
S_{13}	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
S_{14}	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0
S_{15}	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1
S_{16}	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
S_A	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
S_B	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
S_C	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0
S_D	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

The outputs of the individual stages are combined to obtain the required output voltage. The control states of the power switches. In this topology, all the input voltage sources are fixed as v = 100 v for acquiring the maximum peak to peak voltage of 1200 v at the load ends. The load used for testing is 100ohm resistor. The voltages at various stages, output voltage and current. The proposed topology consists of diode, supply voltage and switches. The switched capacitor doubles the input voltage at the load ends. The proposed topology produces +v and +2v voltage levels at the load ends with a lesser number of switches. The switching patterns for the switches s1&s2, voltage ac during on & off period of the switch and the output voltage across the load, the load voltage is equal to the input voltage i.e. 100 v. The results show that the output voltage is becoming 4times. Using this topology more output voltage can be obtained for multi-levels with the minimum input voltage. From figure 1, we can analysis the operation by taking help of the table 2. When the switches s2, s4,s6, s8, s10, s12, s14, s16 or s1, s3, s5,s7, s9,s11, s13,s15 are on state and remaining are off state there will be no path for current hence the output voltage will be 0 level. When s2, s4,s6, s8, s10, s12, s14, s16,sa are on and remaining are off the output voltage at resistor is +1 level. Similarly, when s3, s4, s6, s8,s10, s12, s14, s16, sa are on and remaining are off the output voltage at resistor is -1 level. When s1, s2, s4,s6, s8, s10, s12, s14, s16 are on and remaining are off the output voltage at resistor is +2 level. Similarly, when s3, s4, s6,s8,s10, s12, s14, s16 are on and remaining are off the output voltage at resistor is -2 level. When s1, s2, s6, s8,s10, s12, s14, s16 ,sb are on and remaining are off the output voltage at resistor is +3 level. Similarly, when s3, s4, s7,s10, s12, s14, s16,sb are on and remaining are off the output voltage at resistor is -3level. When s1, s2, s6, s8,s10, s12, s14, s16 are on and remaining are off the output voltage at resistor is +4level. Similarly, when s3, s4, s7,s8, s10, s12, s14, s16 are on and remaining are off the output voltage at resistor is -4 level. When s1, s2, s5,s6, s14, s16, sc are on and remaining are off the output voltage at resistor is +5level. Similarly, when s3, s4, s7,s8, s11, s14, s16, sc are on and remaining are off the output voltage at resistor is -5level. When s1, s2, s5,s6, s9, s10, s14, s16 are on and remaining are off the output voltage at resistor is +6level. Similarly, when s3, s4, s7,s8, s11, s12, s14, s16are on and remaining are off the output voltage at resistor is -6level. When s1, s2, s5,s6, s9, s10, s14, sd are on and remaining are off the output voltage at resistor is +7level. Similarly, when S_3, S_6, S_4,S_8, S_8,S_{10}, S_{12}, S_{14}, S_{16}, S_D are on and remaining are off the output voltage at resistor is -7level. When S_1, S_2, S_5,S_6, S_9, S_{10}, S_{13}, S_{14} are on and remaining are off the output voltage at resistor is +8level. Similarly,

When S_3,S_4,S_7,S_8, S_{11}, S_{12}, S_{15}, S_{16} are on and remaining are of the output voltage at resistor is -8level. In this way total 17levels of symmetric multilevel inverter are obtained.

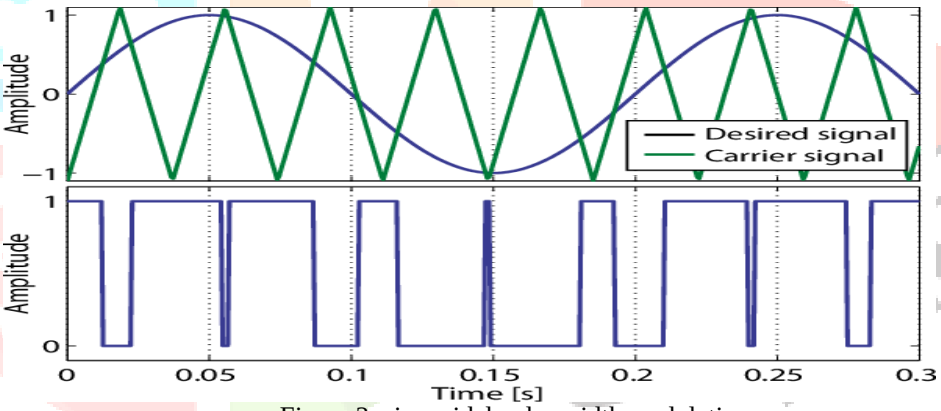

Figure.2: sinusoidal pulse width modulation

The term SPWM stands for “Sinusoidal pulse width modulation” is a technique of pulse width modulation used in inverters. An inverter generates an output of AC voltage from an input of DC with the help of switching circuits to reproduce a sine wave by generating one or more square pulses of voltage per half cycle. If the size of the pulses is adjusted, the output is said to be pulse width modulated. With this modulation, some pulses are produced per half cycle. The pulses close to the ends of the half cycle are constantly narrower than the the pulses close to the center of the half cycle such that the pulse widths are comparative to the equivalent amplitude of a sine wave at that part of the cycle.

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IV. SIMULATION RESULT

In Figure 3 17-level symmetrical Multi level inverter topology consist of 4 units, in each unit there are 4 diodes, two supply voltage sources and 5 switches. The pulses are generated individually and fed to switches.

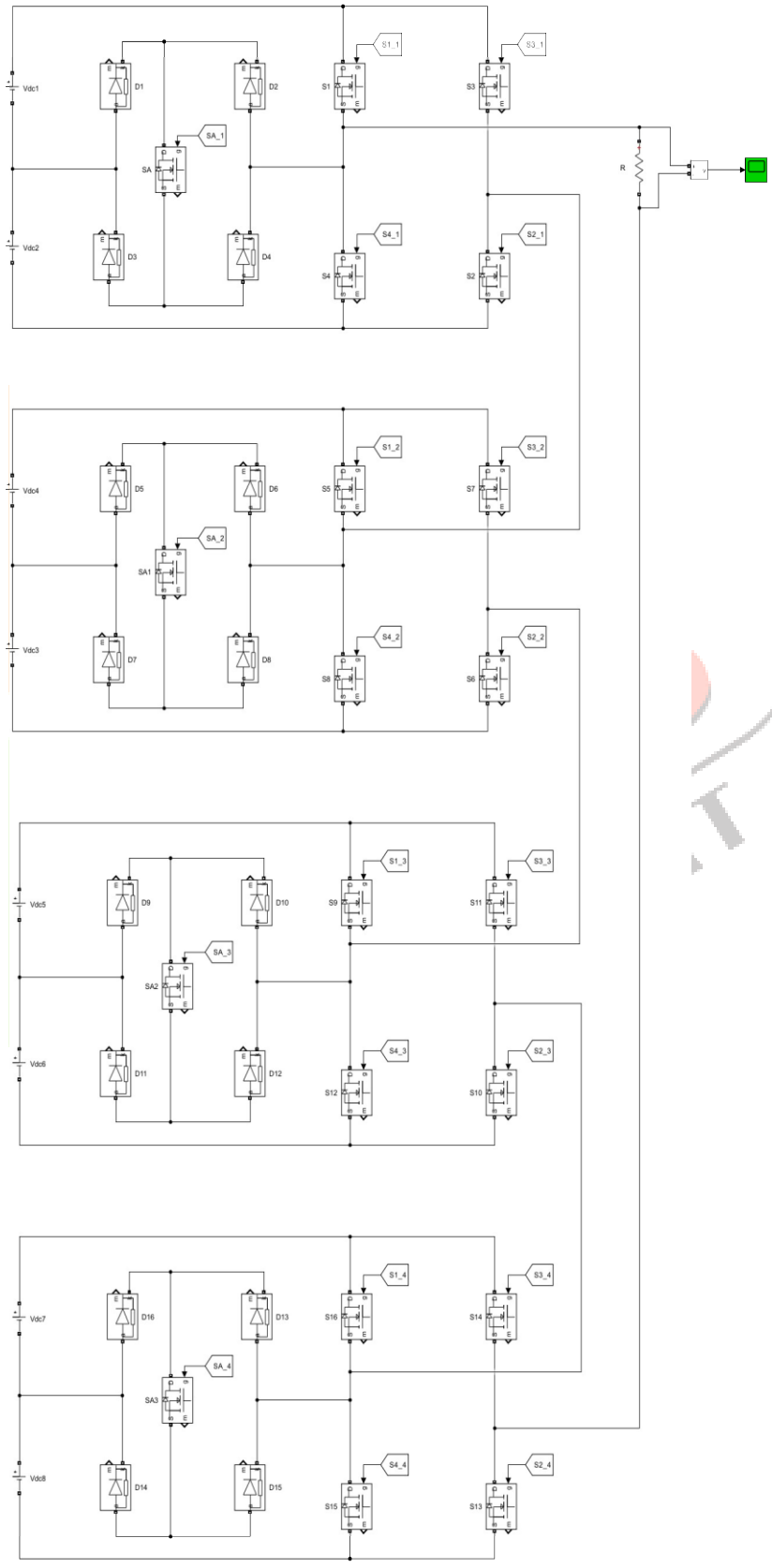

Figure 3: **17 level hybridized cascade h-bridge MIL Simulation diagram**

The fallowing are current waveform, voltage waveform and FFT analysis simulation results of hybridized cascade h-bridge and cascade h-bridge respectively.

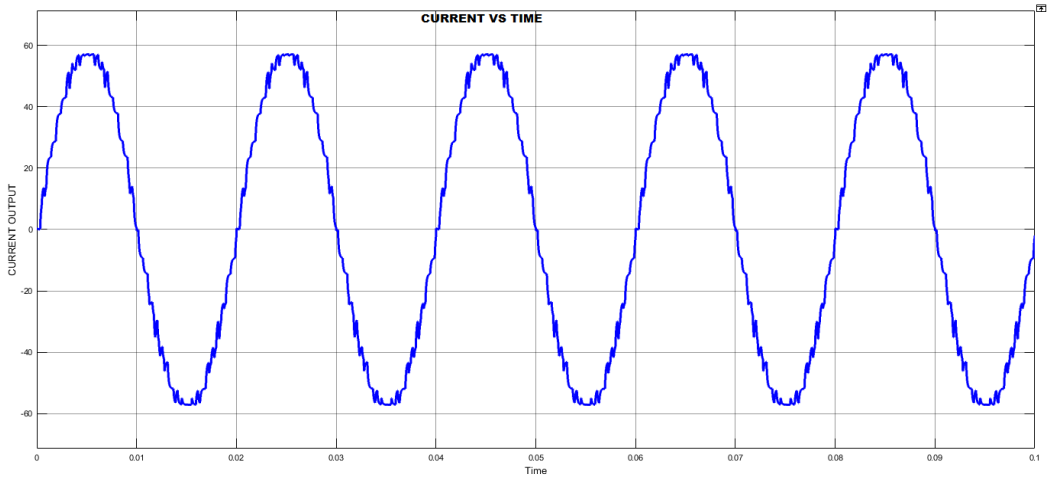

Figure.3: Output load current wave form of 17-level hybridized MLI for RL- load

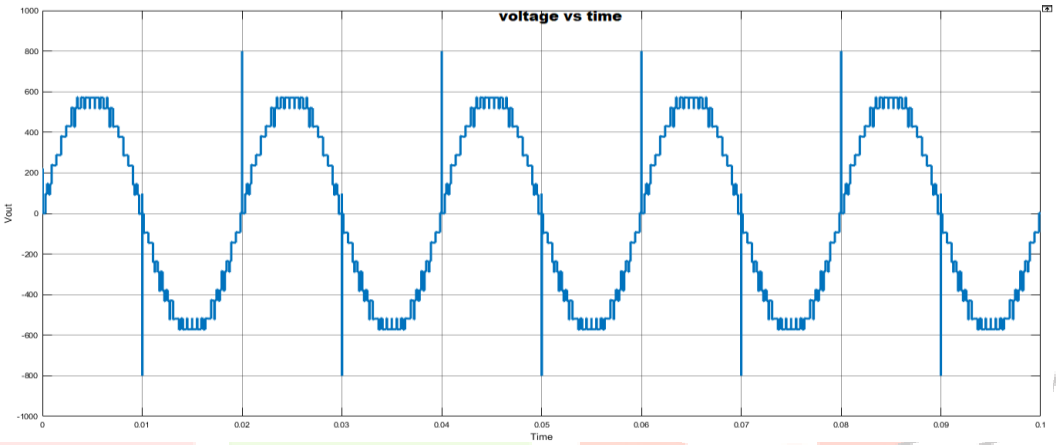

Figure.4: Output load voltage wave form of 17-level hybridized MLI for RL- load

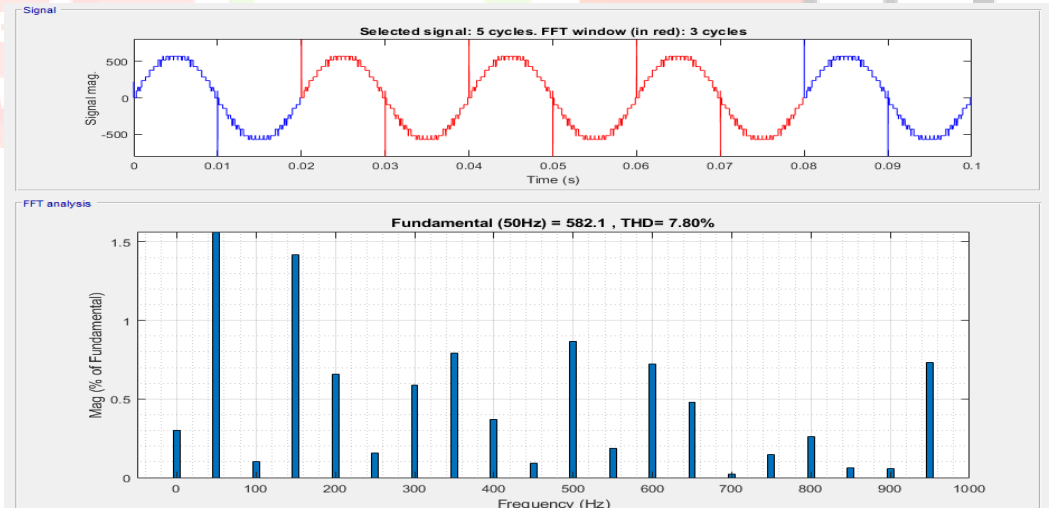

Figure.5: Voltage wave form THD hybridized cascade hybrid for RL load

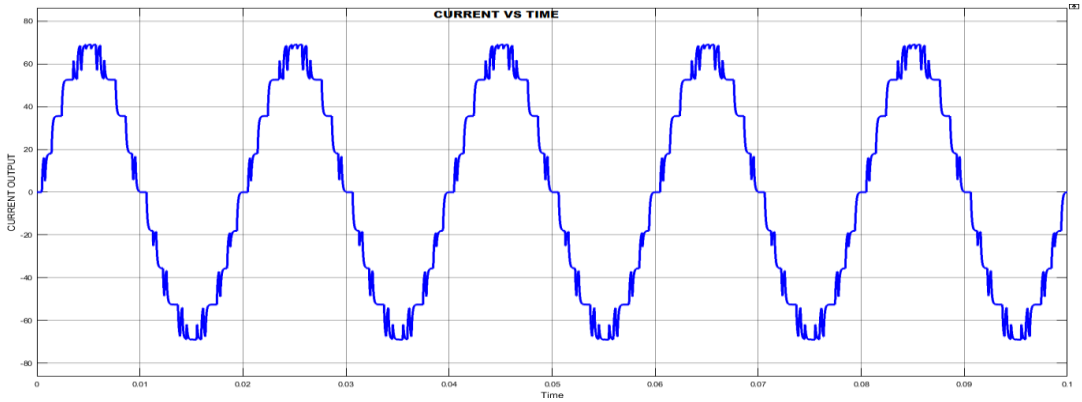

Figure.6: Output load current wave form of 17-level cascade MLI for RL- load

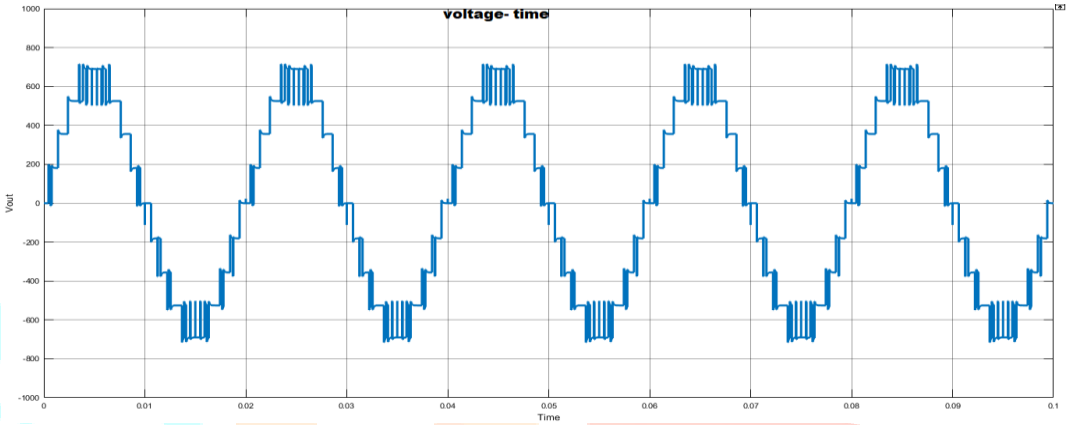

Figure.7: Output load voltage wave form of 17-level cascade h bridge MLI for RL- load

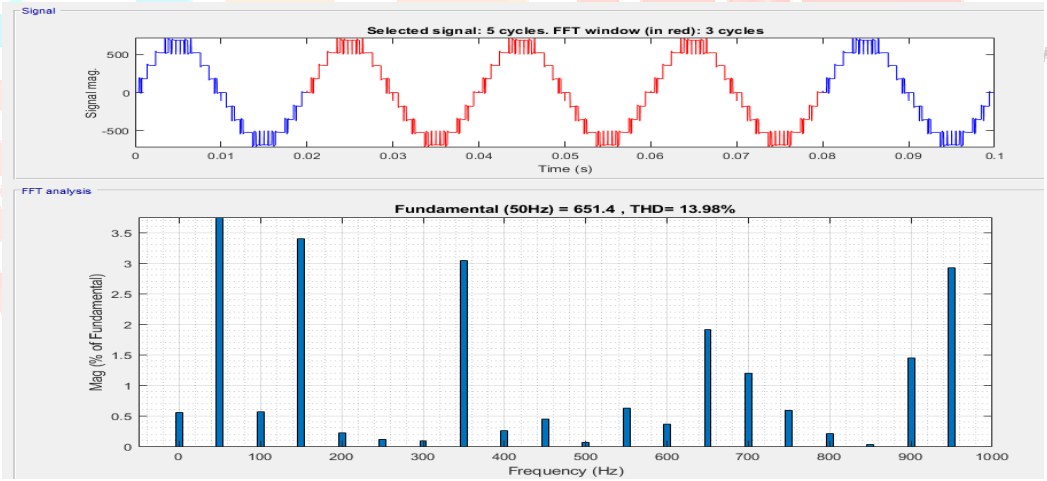

Figure.8: Voltage wave form THD with cascade h bridge MLI for RL load

The above results of 17 level hybridized cascade h-bridge and 17 level cascade h-bridge are illustrated in the below table 3and table 4.

Table 3: Outputs values of 17-level MLI

RL Load	Peak to peak Voltage	RMS Voltage	Peak to peak Current	RMS Current	THD
Hybrid	1210.9V	428.2V	120.19A	42.521A	7.80%
Cascade	1369.3V	484.2V	136.59A	48.3A	13.9%

Table 4: Comparison between cascade h-bridge and hybridized cascade h-bridge MLI

	Cascade H-bridge	**Hybridized Cascade H-bridge**
Levels	17-level	17-level
Total no. of legs	8	4
Levels per leg	3 (+1, 0, -1) for 1st leg; 2(+1, -1) for other legs	5(+2, +1, 0, -1, -2) for 1st leg; 4(+2, +1, -1, -2) for other legs
Total levels	1×3+7×2=17	1×5+3×4= 17
No. of switches per leg	4 MOSFETS	5 MOSFETS
Total no. of switches	32	20
Load type	RL load	RL load
THD	13.9%	7.80%

Therefore, It can be concluded in reference with the table 3 and table 4, about the better performance of hybridized cascade 17-level multilevel inverter in comparison with cascaded H-bridge multilevel inverter in terms of No. of legs, Switches and cost factor. With Improved THD% from 13.98% to 7.80% for RL load.

V. CONCLUSION

The analysis of a 17-level hybridized cascade H-bridge and cascade h-bridge symmetric multilevel inverters is simulated for RL-load. It is shown from results that the system is readily adaptive and maintains a stable output voltage with 7.80% and 13.89% THD for 17-level multilevel inverter for hybridized cascade h bridge RL load, and cascade h bridge RL load respectively. The hybridized cascade H-bridge topology is best suitable compared to cascade h bridge. Due to low THD, these topologies inherently utilize a lesser number of switches and a minimum number of dc input voltage sources. For less no. of switches more levels of output is obtained.

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