MITIGATION OF CUSTOMER VOLTAGE MAGNIFICATION DUE TO BACK TO BACK CAPACITOR SWITCHING

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Abstract: In the early days of development of the power system, electrical engineers were mainly concerned about 'keeping the lights on'. They designed the power system to withstand outages. The main concern was to prevent the frequency of power system from deviating from 50Hz after outages. With the development in technology, use of gadgets like computers, arc furnaces, xerox machine etc. increased. Due to the use of these devices the load on the power system increases especially during the day time because of which many a times voltage level decreases and is needed to be increased. This task of increasing the voltage profile is done by switching on of a capacitor bank in the power system. But this switching action gives rise to capacitor switching transients. These transients are very hazardous to the power system as they cause severe problem to it and components present in it. For instance, at any moment it can crash the computer or data loss and other such problems. So, it becomes necessary to know the cause of these transients so that they can be suppressed.

In this a back to back capacitor bank energization model is simulated in MATLAB Simulink environment. The voltage signals are captured at the source bus and load bus. The FFT analysis is carried out and mitigation of voltage magnification is done using pre-insertion resistors.

Keywords:- Capacitor switching, maximum transient overvoltage's, power quality (PQ), voltage magnification etc.

I. INTRODUCTION

Nowadays a various industries are implementing an automatic power factor correction panel using capacitor banks for the improvement of power factor, but these capacitor banks are making an issue of switching transients during its energization. To improve the power factor capacitor banks may be switched several times during a day. An uncertain loads and fluctuations in voltage are responsible for the switching of capacitor banks. As a result, an unwanted voltage and current spikes having magnitude several times that of voltage and current in steady state will appears in the system, which tends to reduce the life of capacitor banks and electromagnetic switches. Therefore, to suppress this transient from the system certain techniques are implemented. One of the techniques is based on the zero-voltage closing control, this technique requires a lot of electronic equipment's, which tends to go for extra control system as a result cost and complexity of the system increases. Insertion of reactor is one of the methods for mitigation of surges but there is a problem of series resonance in the system. This research work presents a simple structure of resistive capacitor switching technique for mitigation of transients in the system. This technique contains a limiting resistor which works hand in hand to remove the switching transients occurred during the energization of capacitor bank. A limiting resistor is connected in such a way that when transient occurs in the system it should be suppressed by limiting resistor. Benefit of this system is that it has fast response.

II. PROBLEM STATEMENTS

Voltage magnification occurring due to utility capacitor switching is now becomes a common phenomenon. This voltage magnification phenomenon leads to nuisance tripping of adjustable-speed drives (ASDs) and malfunctioning of other end user equipment's. As the utility and customers are now concern about power quality, there is a need to reduce or eliminate the effects of voltage magnification on customer electrical equipment. The devices that are commercially available to reduce or eliminate the effects of voltage magnification include high-resistance or low-resistance pre-insertion inductors used with circuit switchers, controlled closing circuit breakers or vacuum interrupters, and circuit breakers with pre-insertion resistors. This work mainly focuses the problem of occurrence of voltage magnification issue due to capacitor switching and its mitigation using the pre-insertion resistors.

III. CONDITION OF VOLTAGE MAGNIFICATION

Voltage magnification occurs when the transient oscillation initiated by the energization of the distribution capacitor bank excites a series resonance formed by the low voltage system. The result is a higher overvoltage at the low voltage bus.

The highest transient voltages occur at the lower voltage capacitors when the following conditions are met:

- The natural frequencies f1 and f2 are nearly equal.
- The capacitive MVAr of the switched capacitor bank is significantly greater (>10) than the lower voltage capacitor.
- There is little damping on the low voltage system (mostly motor load).

The magnified transient at the lower voltage bus can reach 4 per-unit.

Synchronous closing control

Method for controlling overvoltage by switching when the voltage across the switch at the closing instant is equal to zero (zero voltage on capacitor - zero voltage on bus).

Pre-insertion device:

Method for controlling overvoltage by inserting an impedance (usually inductance or resistance) in series with the component to be energized voltage.

Arresters:

Method for controlling overvoltage by "clipping" at a specified protective level.

Capacitor Bank Calculations

The current flowing through the capacitor at normal power frequency is

$$I = \frac{Q}{\sqrt{3}V} = \frac{40*10^3}{\sqrt{3}*400} = 57.7350A$$

The capacitance for each leg can be determined via the following method:

$$X_c = \frac{V^2}{Q}$$

$$C = \frac{Q}{V^2\omega} = \frac{40*10^3}{400^2*2\pi*50} = 795.7747\mu F$$

The minimum source inductance required to limit the transient to an acceptable level is determined as follows. Assume that the rated (short-circuit) breaker current is 10 kA. Use a tolerance factor of 5 % for the voltage (V = 400V x 1.05=420V)

$$X_L = \frac{V}{\sqrt{3}*10*10^3} = \frac{420}{\sqrt{3}*10*10^3} = 0.0242487\Omega$$

$$L = \frac{X_L}{\omega} = 77.18604\mu H$$

The instantaneous voltage V_0 is the peak phase voltage across the capacitor when breaker B1 is closed. If the capacitor is initially charged, then this value must be added or subtracted from V_0:

$$V_0 = \frac{\sqrt{2}}{\sqrt{3}}(V_{rated}) = \frac{\sqrt{2}}{\sqrt{3}}(400) = 326.5986V$$

The switching surge impedance is determined by the combination of source inductance and the capacitance in a single leg of a bank:

$$Z_{surge} = \sqrt{\frac{L}{C}} = 0.3114399\Omega$$

The following equations can be used to determine the magnitude and frequency of the inrush currents when breaker is closed at a voltage peak. Since the transient frequency of the inrush current is much higher than the 50 Hz power frequency, we can assume the instantaneous voltage (V_0) will remain constant over the transient period.

$$I_{peak} = \frac{V_0}{Z_{surge}} = 1048.7062A$$

$$f = \frac{1}{2\pi\sqrt{L*C}} = 642.1785Hz$$

The inrush current magnitude is approximately 20 times higher than the peak current at the power frequency.

The pre-insertion resistance will damp out the transients. Its value can be determined using the following equation:

$$R_{optimum} = \sqrt{\frac{L}{C}} = 0.3114\Omega$$

IV.   SYSTEM STUDIED

The capacitor bank energizing model developed in Simulink is shown in figure 1. It is used to simulate customer voltage magnification caused by capacitor bank energization for power factor correction in the power system. The model consists of 11 kV, 30 MVA, 50 Hz three-phase source feeding through 11 kV/0.4 kV, 1 MAV delta/wye transformers to 100 kW resistive and 100 kvar inductive load. The voltage measurement is carried at 11 kV and 0.4 kV buses. Each feeder bus consists of a capacitor bank connecting through a three-phase circuit breaker. The capacitor bank at 0.4 kV bus has a capacity of 40 kvar, which can compensate power factor up to 0.857 for a 100 kvar inductive load. The capacitor bank at 11 kV bus usually has a higher capacity, in this model 100 kvar is used. The capacitor bank energizing model is capable of simulating customer voltage magnification caused by energization of capacitor bank at 11 kV bus or at 0.4 kV bus. A 0.2 second simulation time is set to run the simulation.
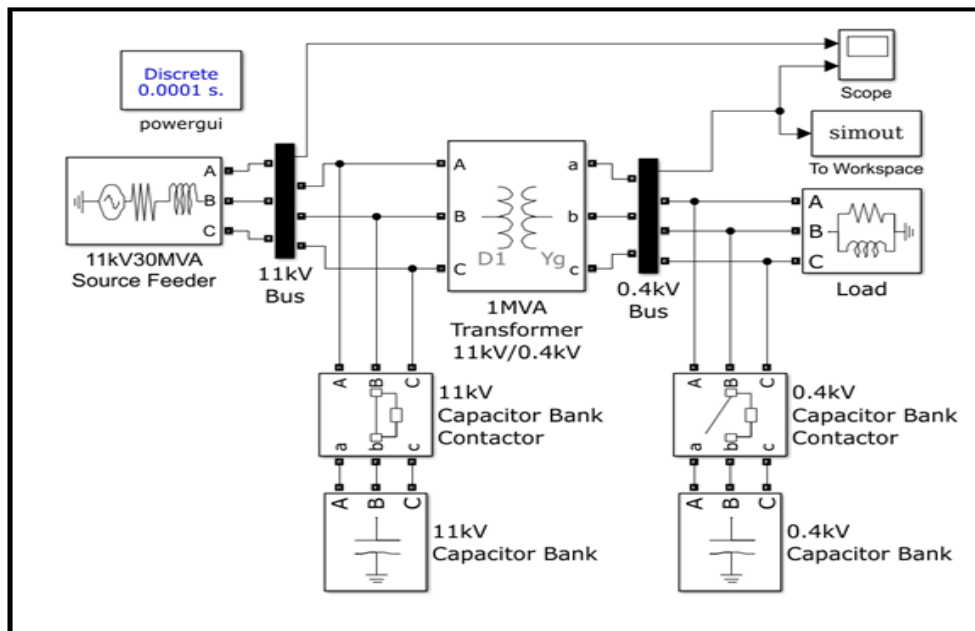
Figure 1:- Capacitor Bank Energizing Model Developed in Simulink

Simulation Cases

The capacitor bank energization model is simulated using MATLAB Simulink Environment. Here star connected capacitor banks configurations are used. In general, there are two capacitor switching configurations. Configuration1 is when a signal capacitor bank is connected to the A.C bus. This is typically referred to as isolated capacitor switching. Another configuration is when there are multiple capacitor banks A.C bus. When a bank is switched on to the bus with other banks all ready connected, this is referred to as back-to-back capacitor.

In this report back-to-back capacitor switching configurations with star connected capacitor banks are considered.

In Simulink circuit there are total 2 capacitor banks. They are connected to the A.C bus with the help of circuit breakers. In this project work 3 cases are considered.

Case 1: Without Pre-insertion resistor
1) Back-to-Back switching of 0.4kV capacitor bank

Case 2: With Pre-insertion resistor of 0.3Ω
1) Back-to-Back switching of 0.4kV capacitor bank

Case 3: With Pre-insertion resistor of 3Ω
1) Back-to-Back switching of 0.4kV capacitor bank

In each case the capacitors are switched at instants $0°, 45°$ and $90°$ of R phase(which is a reference phase).

Methodology

The Capacitor Bank Energization Model Shown In Figure 1 Is Simulated Using MATLAB Simulink Environment. Total 3 Cases Of Capacitor Switching Are Simulated At 00, 450 And 900 Switching Instants. The Voltage Waveform Is Captured At The Source And Load. The Duration Of Simulation Run Is Kept 0.2 Seconds. The Waveform Is Sampled At 10 Khz Sampling Frequency.

The voltage magnification phenomenon occurs due to the switching of capacitor bank at the source and load buses. The evaluation of this phenomenon is done by measuring the voltage peak during the transient period in the captured voltage waveform. Further the FFT analysis of the captured voltage waveform is done with the help of MATLAB toolbox. The percentage of THD is estimated in each case corresponding to 11kV and 0.4kV voltage waveforms.

In case back-to-back switching of capacitor bank is done to simulate voltage magnification phenomenon. In case 2 the mitigation of voltage magnification is done by using the pre-insertion resistor (0.3Ω) technique of mitigation. In case 3 the mitigation of voltage magnification is done by using the pre-insertion resistor (3Ω) technique of mitigation. In each case FFT analysis is done and the THD percentage are calculated. Finally, the comparison of the THD percentage in each case is done to evaluate the performance of mitigation technique.

V.   SIMULATION WAVEFORMS AND FFT ANALYSIS

The simulation waveforms of voltages for each case at $0°$, $45°$ and $90°$ instants are represented along with its FFT analysis.

1) **Back-to-back capacitor switching of 0.4kV & 11kV capacitor at $0°$ instant of R-phase**

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at $0°$ instant of R-phase. Figure 2 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at $0°$ instant of R-phase.
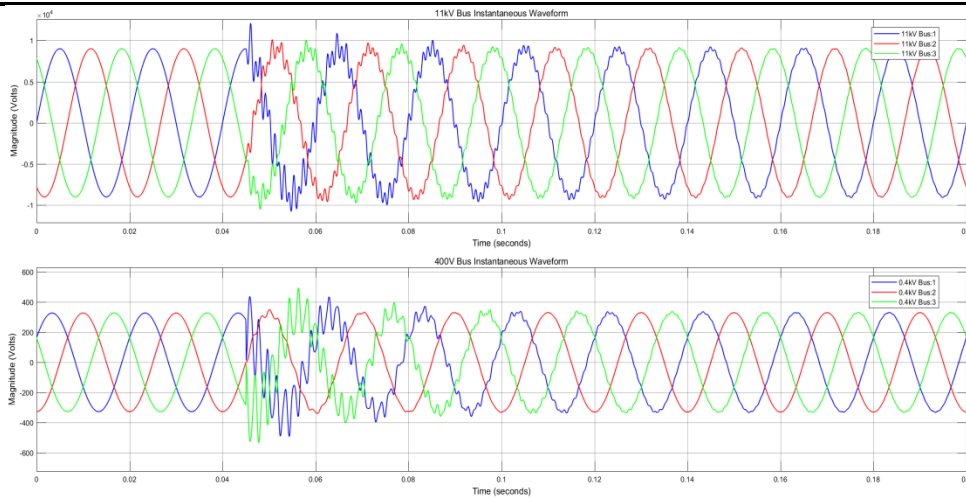
Figure 2:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 3 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 2.85%.
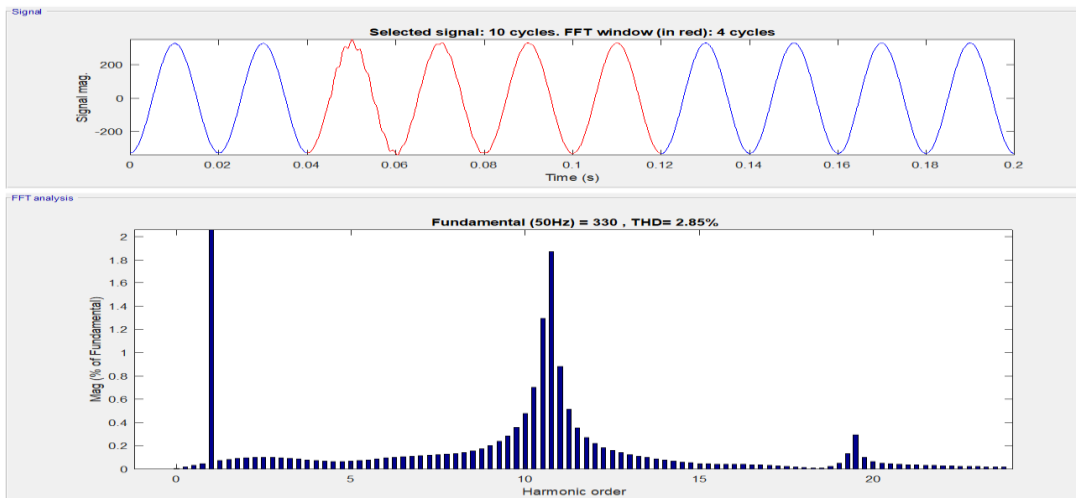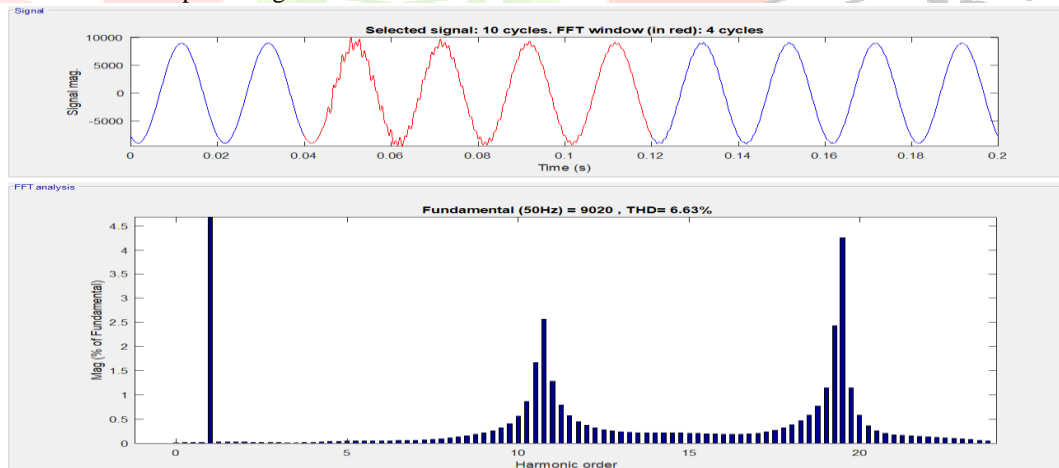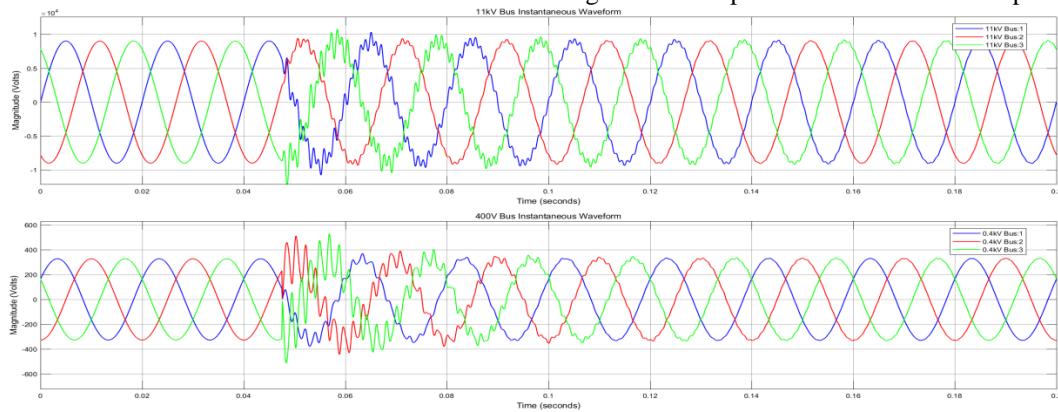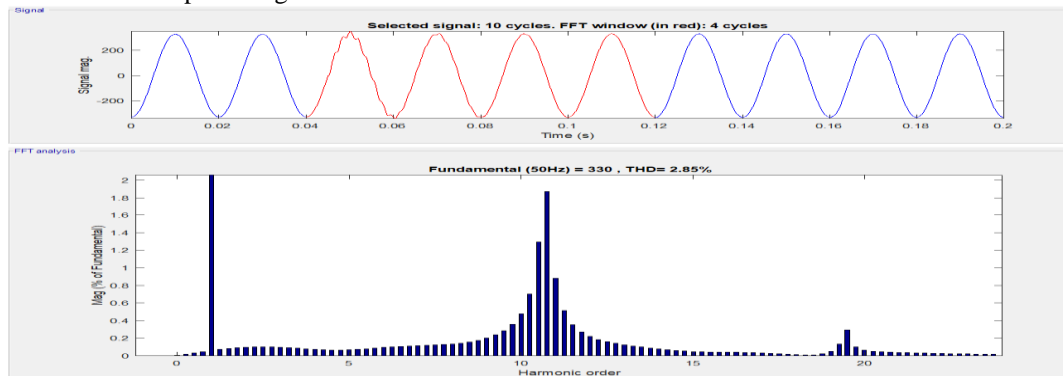

Figure 3:- FFT analysis of voltage waveform at 0.4kV bus

Figure 4 shows the FFT analysis of voltage waveform at 11kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 6.63%.

Figure 4:- FFT analysis of voltage waveform at 11kV bus

2) **Back-to-back capacitor switching of 0.4kV & 11kV capacitor at 45^0instant of R-phase**:

    In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 45^0 instant of R-phase. Figure 5 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 45^0 instant of R-phase.

Figure 5:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

    Figure 6 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 2.85%.
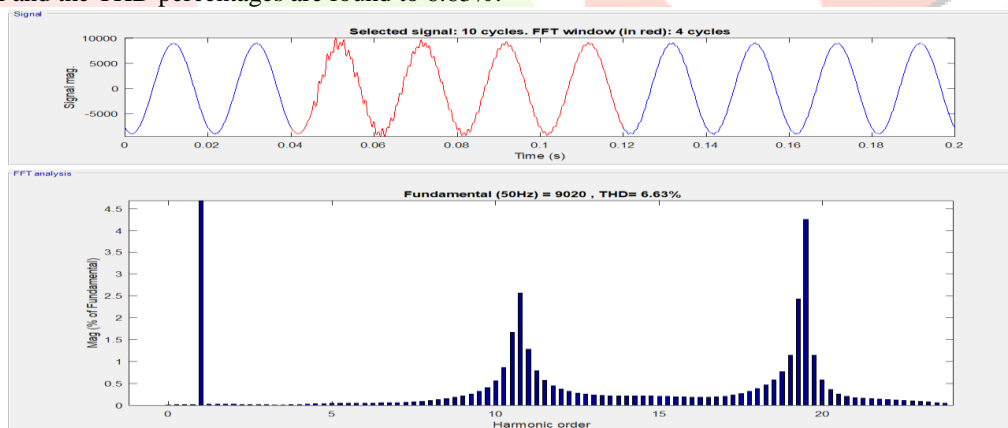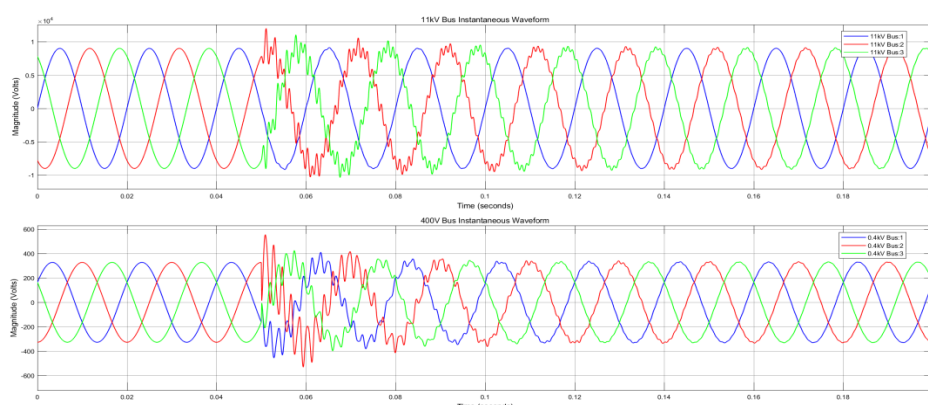

Figure 6 :- FFT analysis of voltage waveform at 0.4kV bus

    Figure 7 shows the FFT analysis of voltage waveform at 11kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 6.63%.

Figure 7:- FFT analysis of voltage waveform at11kV bus

3) **Back-to-back capacitor switching of 0.4kV& 11kV capacitor at 90^0instant of R-phase:**

    In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 90^0 instant of R-phase. Figure 8 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 90^0 instant of R-phase

Figure 8:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 9 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 30.98%.
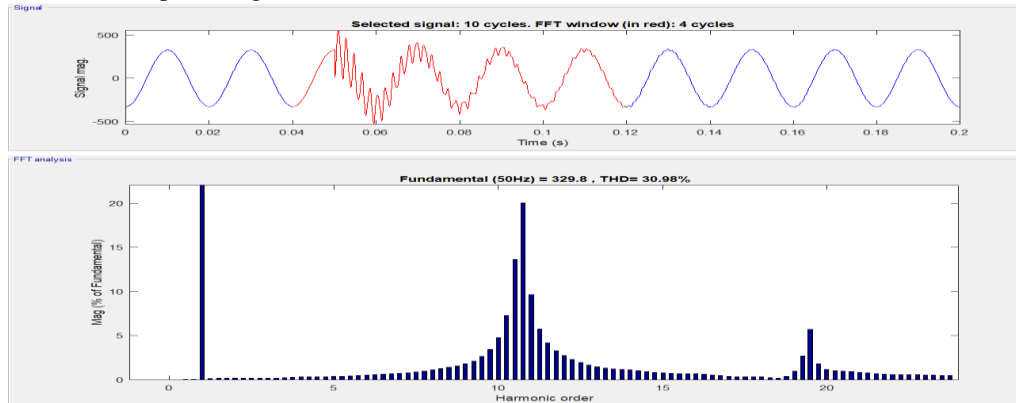

Figure 9 :- FFT analysis of voltage waveform at 0.4kV bus

Figure10 shows the FFT analysis of voltage waveform at 11kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 11.72%.
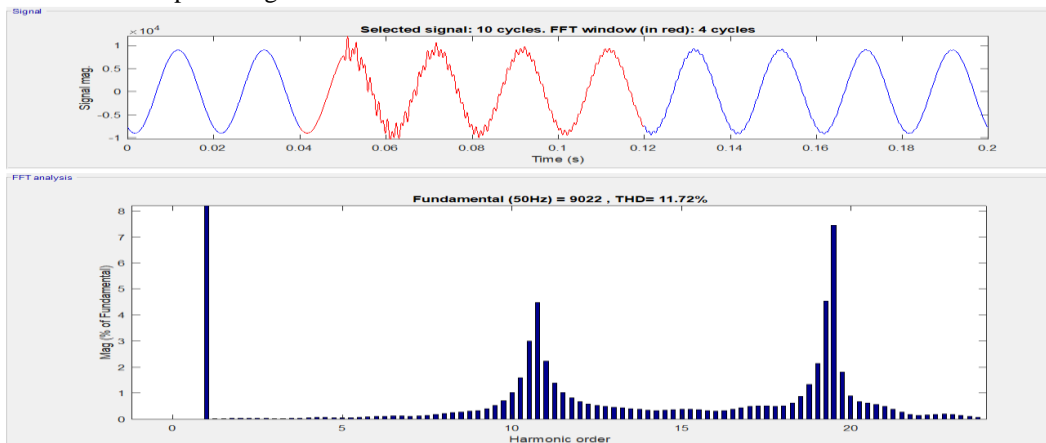

Figure 10 :- FFT analysis of voltage waveform at11kV bus

VI.   MITIGATION OF VOLTAGE MAGNIFICATION

At the switching instant, the voltage in the capacitor cannot change instantaneously. The bus voltage is pulled down, and then rises as the capacitor begins to charge. During the process, the capacitor voltage may overshoot. This phenomenon of voltage magnification is mitigated by various techniques. In this report pre-insertion resistors are used to mitigate the voltage magnification effect. As per the calculation the pre-insertion resistor of 0.3 Ω is required to mitigate the voltage mitigation. Here we have considered 0.3 ohm and 3 Ω pre-insertion resistors for mitigation of voltage magnification caused by capacitor switching. Figure below shows the results of pre-insertion resistor method of mitigation of voltage magnification.

With Pre-insertion Resistor of 0.3 Ω

1) **Back-to-back capacitor switching of 0.4kV & 11kV capacitor at 0^0 instant of R-phase:**

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 0.3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 11 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 0^0 instant of R-phase with the pre-insertion resistor of 0.3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.
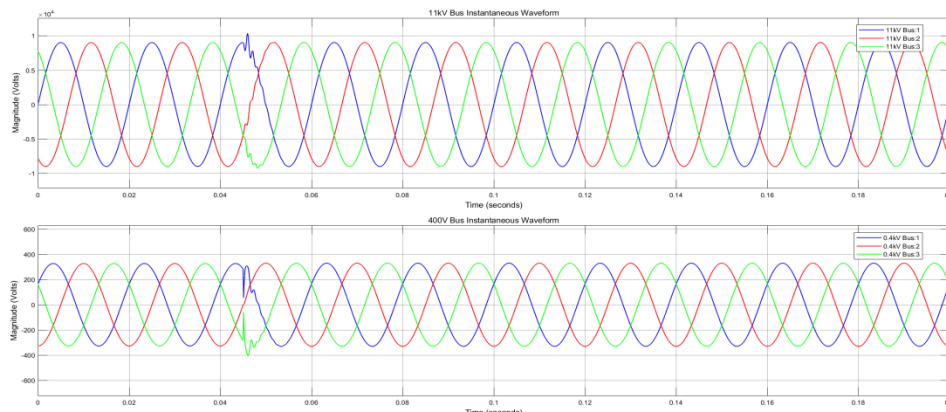

Figure 11 :- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 12 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.60%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching
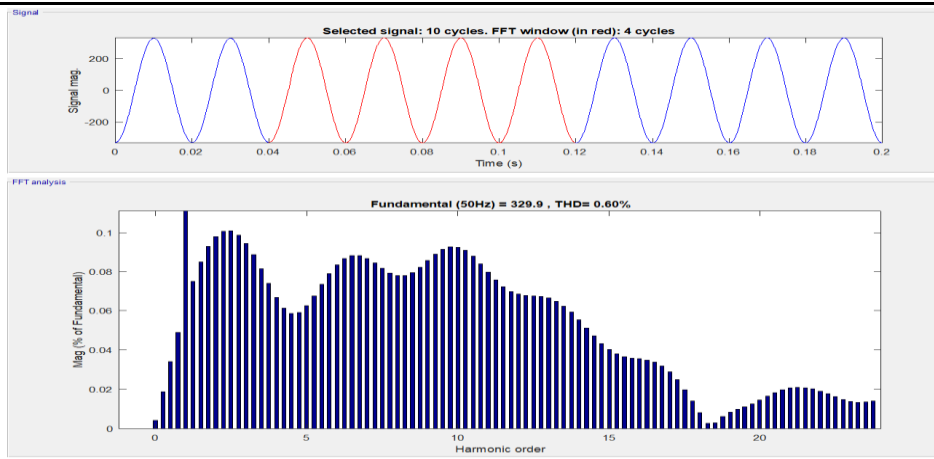
Figure 12 :- FFT analysis of voltage waveform at 0.4kV bus

Figure 13 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 1.24%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
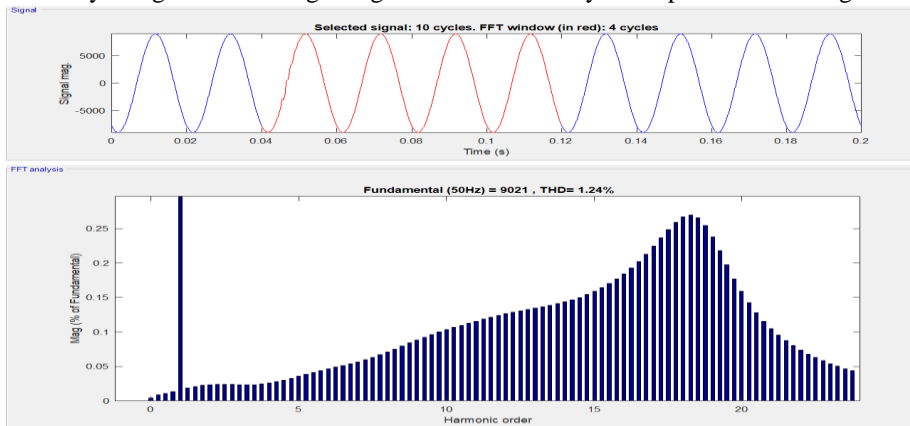

Figure 13:- FFT analysis of voltage waveform at11kV bus

2) **Back-to-back capacitor switching of 0.4kV & 11kV capacitor at 45^0instant of R-phase:**

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 45^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 0.3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 14 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 45^0 instant of R-phase with the pre-insertion resistor of 0.3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.
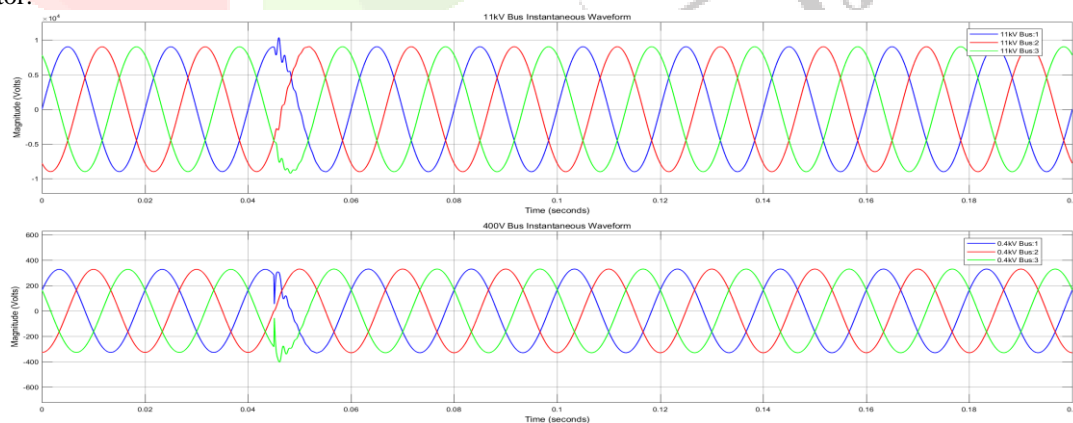

Figure 14:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 15 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.60%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
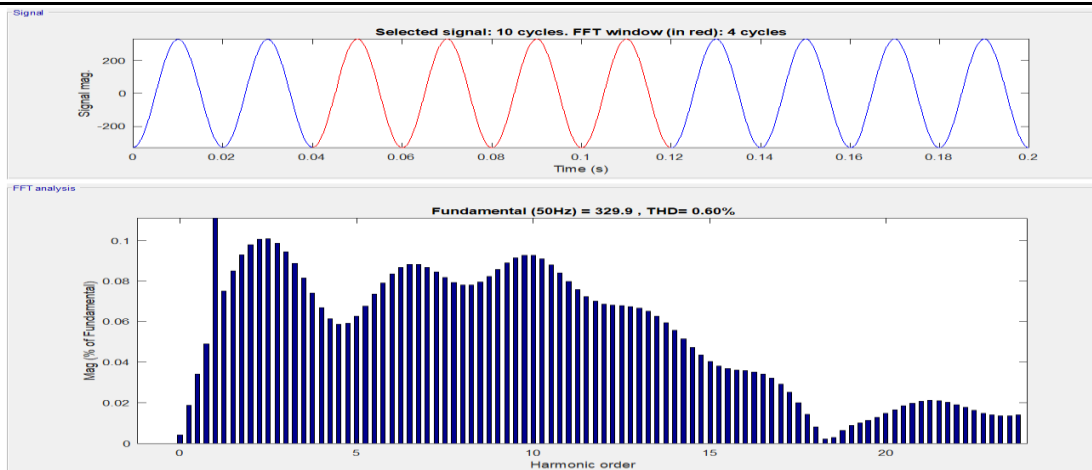
Figure 15:- FFT analysis of voltage waveform at 0.4kV bus

Figure 16 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 1.26%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
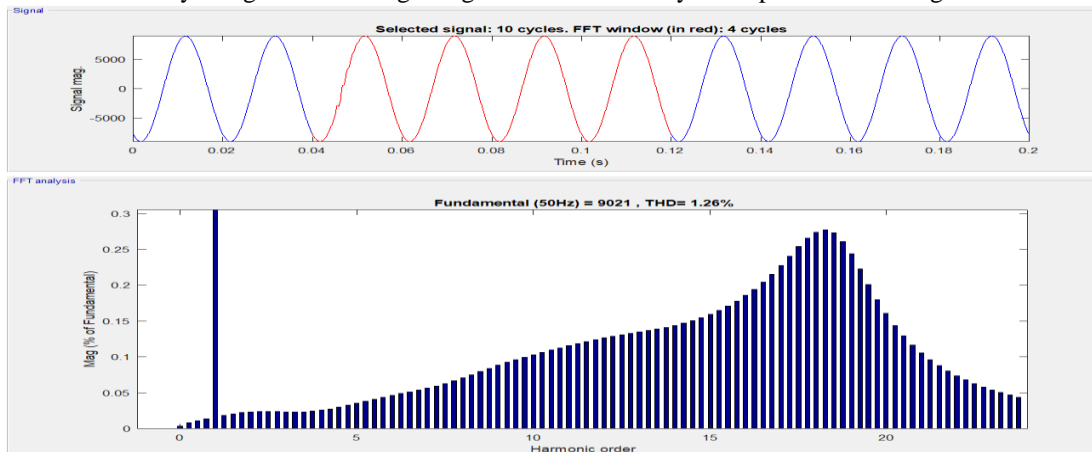

Figure 16:- FFT analysis of voltage waveform at11kV bus

3) **Back-to-back capacitor switching of 0.4kV & 11kV capacitor at 90^0 instant of R-phase:**

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 90^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 0.3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 17 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 90^0 instant of R-phase with the pre-insertion resistor of 0.3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.
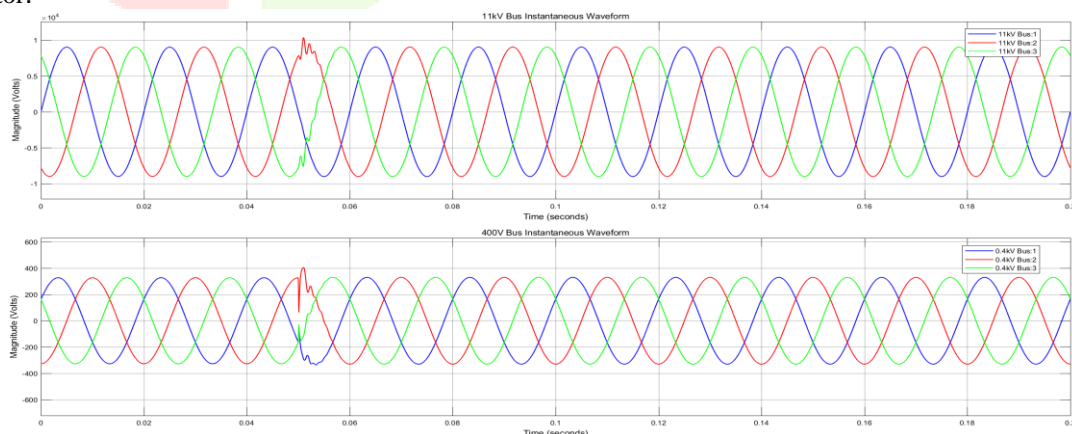

Figure 17:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 18 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 6.22%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
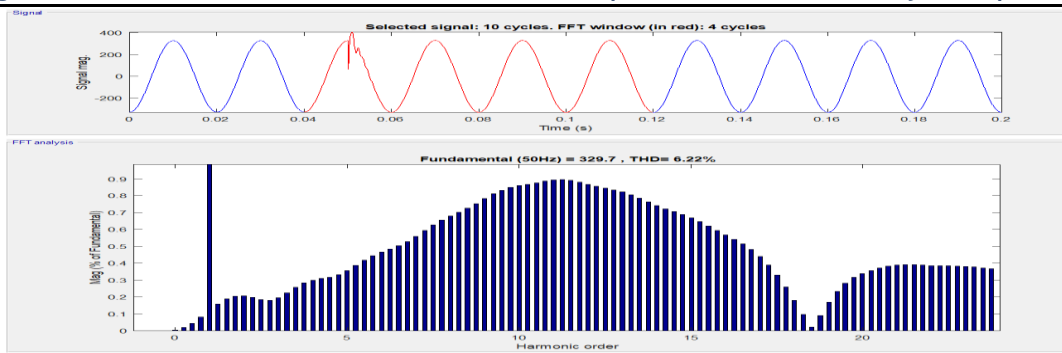
Figure 18:- FFT analysis of voltage waveform at 0.4kV bus

Figure 19 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 2.24%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
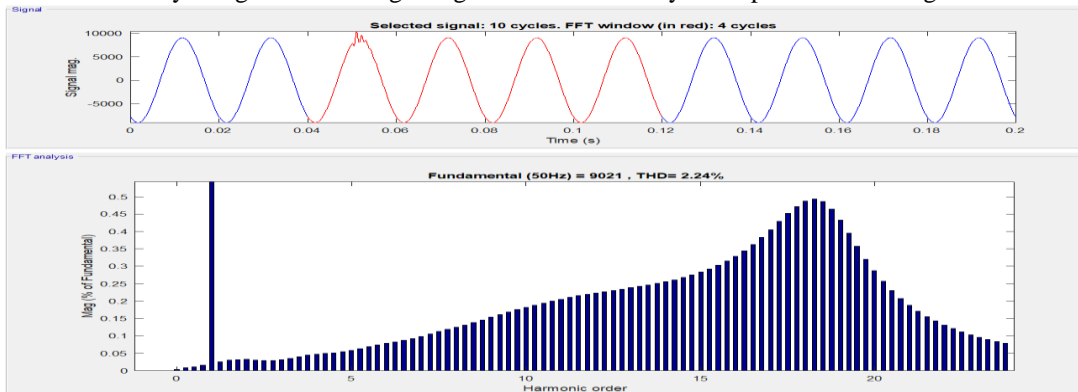

Figure 19:- FFT analysis of voltage waveform at11kV bus

With Pre-insertion Resistor of 3 Ω

1) **Back-to-back capacitor switching of 0.4kV & 11kV capacitor at 0^0 instant of R-phase:**

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 20 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 0^0 instant of R-phase with the pre-insertion resistor of 3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.
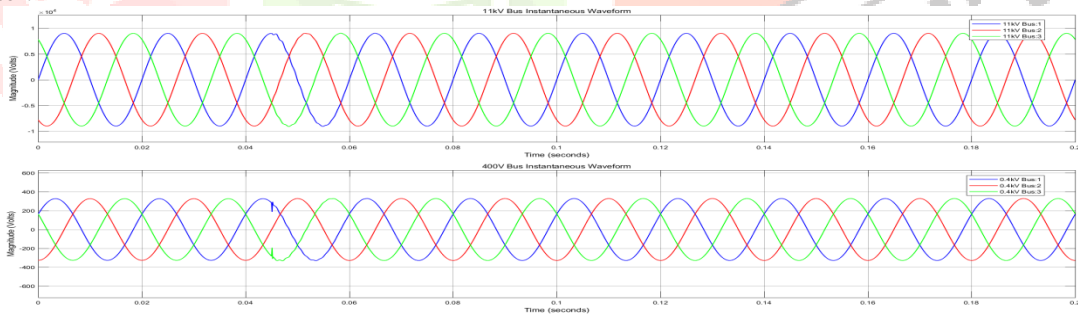

Figure 20:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 21 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.20%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
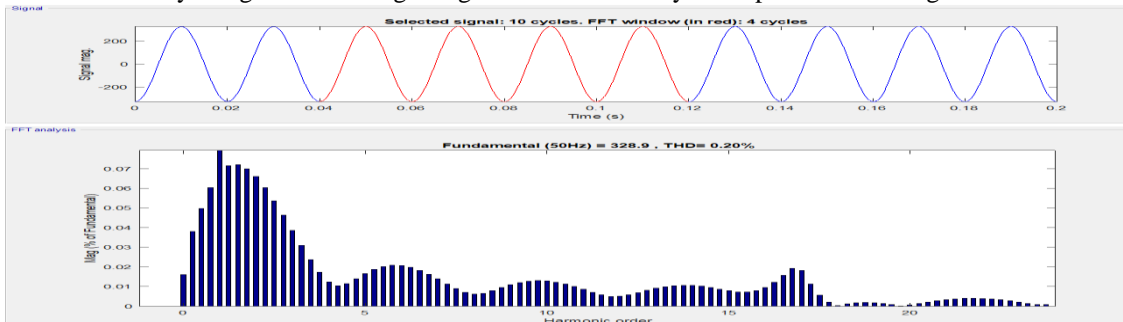

Figure 21:- FFT analysis of voltage waveform at 0.4kV bus

Figure 22 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.33%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
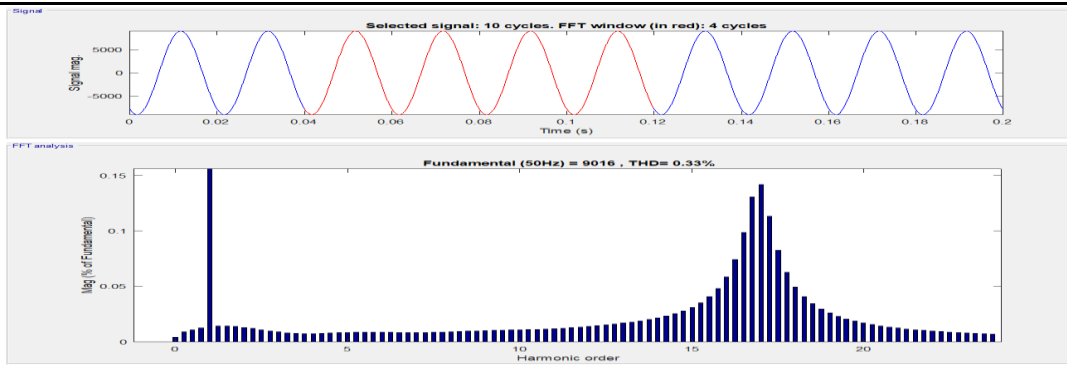
Figure 22:- FFT analysis of voltage waveform at11kV bus

2) Back-to-back capacitor switching of 0.4kV & 11kV capacitor at 45⁰instant of R-phase:

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 45^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 23 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 45^0 instant of R-phase with the pre-insertion resistor of 3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.
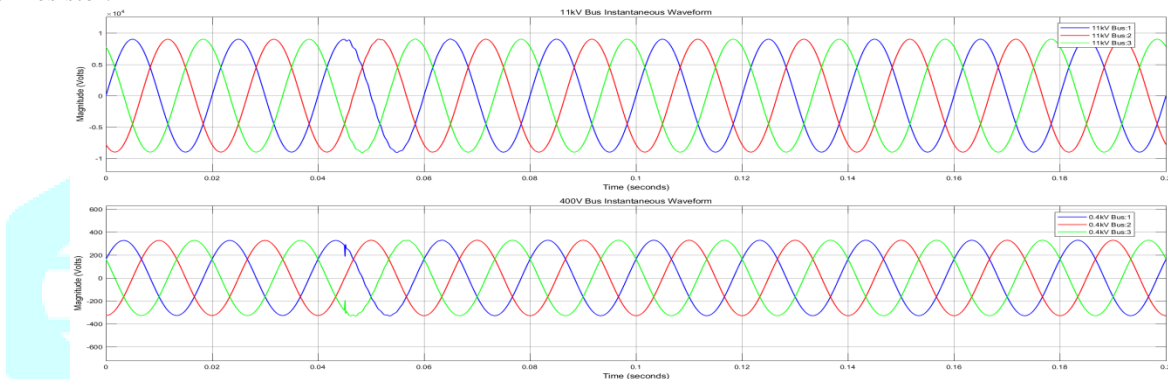

Figure 23 :- FFT analysis of voltage waveform at11kV bus due to back-to-back capacitor switching

Figure 24 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.20%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
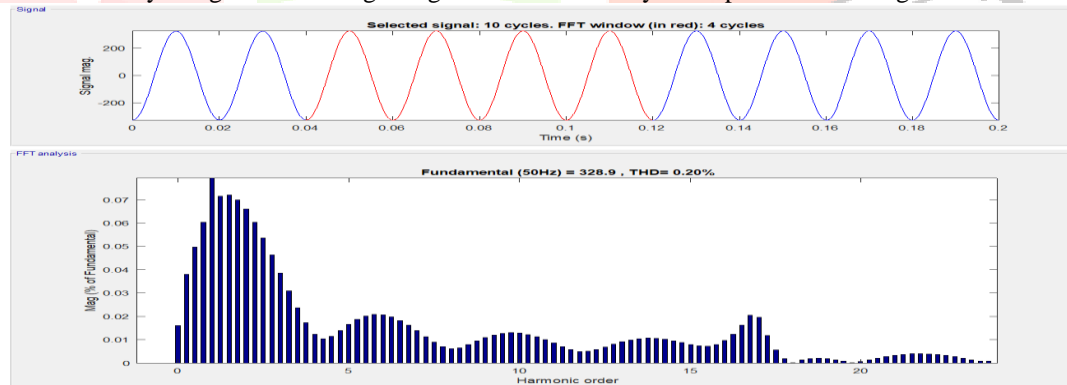

Figure 24:- FFT analysis of voltage waveform at 0.4kV bus

Figure 25 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.34%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
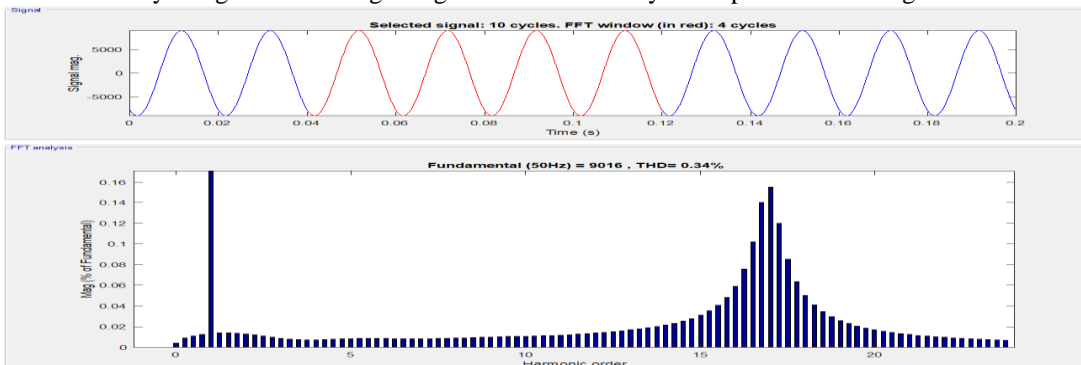

Figure 25:- FFT analysis of voltage waveform at11kV bus

3) Back-to-back capacitor switching of 0.4kV & 11kV capacitor at 90^0 instant of R-phase:

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 90^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 26 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 90^0 instant of R-phase with the pre-insertion resistor of 3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.
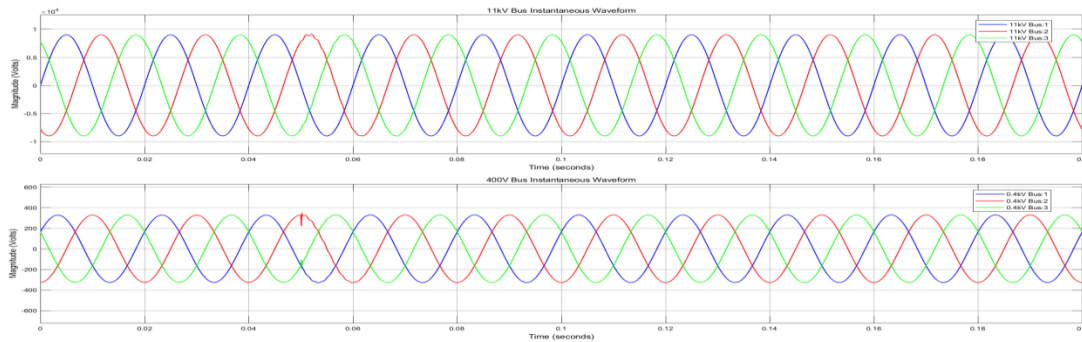

Figure 26:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 27 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 1.83%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

Figure 27:- FFT analysis of voltage waveform at 0.4kV bus

Figure 28 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.60%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.
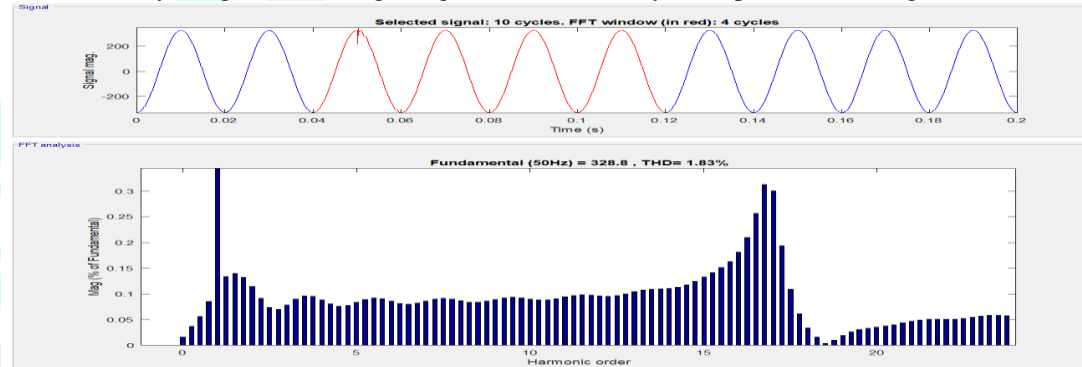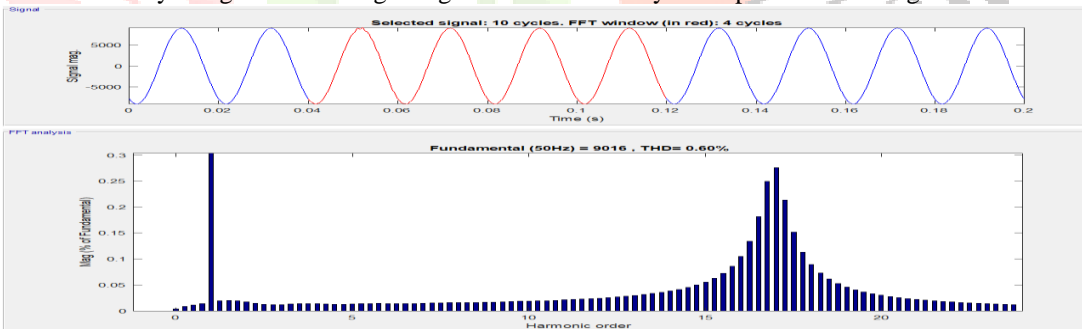

Figure 28:- FFT analysis of voltage waveform at 11kV bus

VII.   COMPARATIVE ANALYSIS

At the switching instant, the voltage in the capacitor cannot change instantaneously. The bus voltage is pulled down, and then rises as the capacitor begins to charge. During the process, the capacitor voltage may overshoot. The comparative analysis of the THD percentage in each case is done and tabulated as below.

Table 1:- Back-to-back capacitor switching of 0.4kV capacitor at 0^0, 45^0 and 90^0 instants of R-phase

Capacitor Switching Instant	THD % Without Pre-Insertion Resistor	THD % With 0.3Ω Pre-Insertion Resistor	THD % With 3Ω Pre-Insertion Resistor
Zero Degree	2.85	0.60	0.20
Fourty Five Degree	2.85	0.60	0.20
Ninty Degree	30.98	6.22	1.83

Table 2:- Back-to-back capacitor switching of 11kV capacitor at 0^0, 45^0 and 90^0 instants of R-phase

Capacitor Switching Instant	THD % Without Pre-Insertion Resistor	THD % With 0.3ΩPre-Insertion Resistor	THD % With 3Ω Pre-Insertion Resistor
Zero Degree	6.63	1.24	0.33
Fourty Five Degree	6.63	1.26	0.34
Ninty Degree	11.72	2.24	0.60

VIII.   CONCLUSION

In this report the voltage magnification phenomenon which originated from utility capacitor bank switching is simulated and studied. The characteristics of the switching transients coming from the utility system of the capacitor bank are analyzed. For customers having the power quality problems, these can be controlled by the different mitigation techniques as we have seen in the MATLAB simulation results. The information obtained from the simulations and results depicts that transients are produced in the current and voltage when capacitor banks are switched. Both Isolated switching and Back-to-back switching of capacitor bank is done. Magnified transients up to 2 p.u. are possible. It is observed that the transients are more at ninty degree switching instant and less at zero degree switching instant. Transients occurred during the energisation of capacitor bank under both isolated switching and back-to-back switching are successfully eliminated by using the pre-insertion resistor. The pre-insertion resistor technique of mitigation of voltage magnification caused by capacitor switching is most simple and less expensive technique applied in the real-world power utility. It can be concluded from the simulation results that the pre-insertion resistor techniques can remove the transients successfully.

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