



IMPLEMENTATION OF CMOS INVERTER-BASED OTA'S

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Abstract:

The development of wearable devices, particularly in the biomedical and healthcare field of applications, has grown much especially during the last two decades. The sensors used in this field have special design and development restraints: the portability, the size and weight, longevity, ergonomics and the power consumption in parallel with the energy-efficiency are among the most important aspects to take in consideration. The devices must have small form factor and active area with low power consumption, enabling comfortable, unobtrusive and long-time monitoring, hence, suitable for daily use. Sensing amplifiers usually dominate the power and the noise of the recording frontend, therefore significant research activity has been focused on designing this block, taking into consideration the need for high improvement in power consumption, with proposals of new strategies to overcome the challenges of modern CMOS technologies.

A new family of innovative operational trans-conductance amplifier (OTA) topologies based on CMOS inverter structures, with improved power consumption. This new family of OTA designs is suitable for biomedical and healthcare circuits and systems, due to the high improvement in power consumption, when compared to the state-of-the-art in this field. Two fully-different implementations are presented, a first one with a double CMOS branch biased by two pairs of voltage-combiners structures in both NMOS and PMOS configurations, and a second one with folded voltage-combiners specifically targeting low voltage applications, e.g., supplies below 1 V. The usage of voltage-combiners to bias the OTAs improves power consumption. The folded voltage-combiners biased OTA is able to operate correctly under a voltage supply down to 0.7 V with proper DC biasing. The simulation is performed in HSPICE Synopsys Tool and compared with existing designs.

KEYWORDS -OTA's, CMOS, AC AND DC ANALYSIS

I. INTRODUCTION

The electronics industry has achieved phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, and large-scale systems design - in short, due to the advent of VLSI. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field. Gives an overview of the prominent trends in information technologies over the next few decades. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end users with a certain amount of processing power and portability. This trend is expected to continue, with very important implications for VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example). The other important characteristic is that the information services tend to become more and more personalized (as opposed to collective

services such as broadcasting), which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility.

II. LITERATURE SURVEY

2.1 Introduction

Distinguished by the raising level of integration and complexity. It aims to decrease exponentially the minimum feature sizes used to design integrated circuits. The cost of design is a great problem to the continuation of this evolution. Senior designer's knowledge and skills are required to ensure a good analogue integrated circuit design. To fulfill the given requirements, the designer must choose the suitable circuit architecture, although different tools partially automating the topology synthesis that appeared in the past. The optimization becomes an important method; a heuristic process was developed in. Nominal circuit design was considered in, sizing problems were discussed in, and worst-case optimization in. Several optimization tools were developed, such as equation-based GPCAD, AMG using a symbolic simulator and the simulation-based ASTRX/OBLX. Recently, the sizing problem from different aspects are addressed in numerous papers. Designing high-performance baseband analog circuits is still a hard task toward reduced supply voltages and increased frequency. Current tendency focuses on some radiosoftware receivers which suppose an RF signal conversion just after the antenna. Thus, a very higher sampling frequency and resolution analog-to-digital converter design is required. Our target was to design a inverter-based OTAs biased by folded VCs, circuit in sight of Sigma Delta analog-to-digital converter design using for wideband radio applications.

The keeper transistor M2 has been incorporated to replenish the dynamic node against leakage-current and charge sharing. Depending on footer transistor inclusion, the domino logic circuit variants are classified as footed domino logic and footerless domino logic circuits.

Domino logic circuit operation occurs in two phases as defined by the clock CLK signal. The pre-charge phase occurs when clock signal CLK is LOW and evaluation phase occurs when clock CLK is HIGH. Scaling up of keeper transistor size increases the robustness of the circuit. However, this increases the contention between keeper and PDN. This is due to the keeper circuit, which tries to retain the logic HIGH during HIGH input conditions to the pull-down network (PDN). This leads to decreased speed performance.

To alleviate this issue, various domino logic structures are proposed in the literature. Although, dynamic logic circuit offers reduction of area and increased speed, significant dynamic power consumption is high due to the output signal transitions at the output node during pre-charge phase even for consecutive HIGH inputs. The necessity to reduce the dynamic power consumption paved to various static switching mechanism design structures of domino logic such as Pseudodynamic buffer (PDB), Limited Switch Dynamic logic (LSDL).

In PDB mechanism, during the second pre-charge phase, the discharge of the output node is prevented. This facilitates in retaining the previous evaluation output. Thereby, the switching at the output node is reduced. A clock delayed dual keeper with static switching (CDDK-SS) is proposed, a control mechanism for the keeper to reduce contention current and also provides a static output. It is based on the delayed enabling of the dual keeper transistor arrangement using, delayed inverted clock signal. The static inverter configuration at the output node prevents the discharge of the output node during the pre-charge phase.

2.2 Existing System

The development of wearable devices, particularly in the biomedical and healthcare field applications, has grown much during the last two decades.

The sensors used in these fields have special design and development restraints: portability, size and weight, longevity, ergonomics and power consumption in parallel with the energy-efficiency are among the most important aspects for consideration.

2.3 Disadvantages of the Existing System

- Implementation cost is more
- High power consumption
- Delay is more

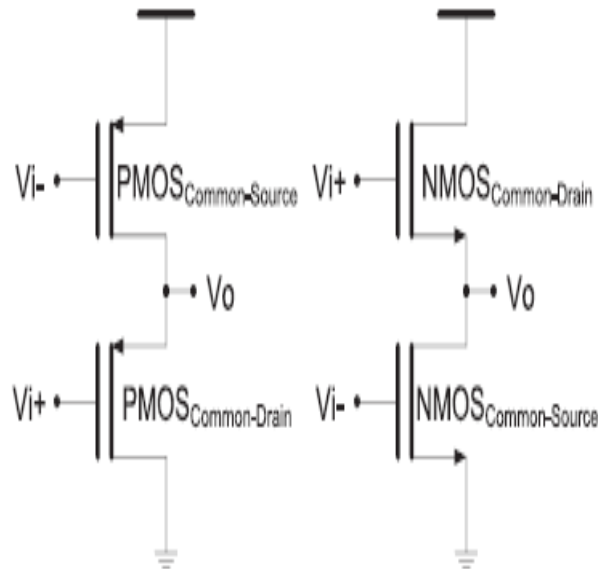


Fig. 1. Standard VCs: a) PMOS based; b) NMOS based

i) Inverter-based OTA biased by standard VCs

This paper presents a new family of inverter-based OTAs biased by voltage-combiners for gain and energy-efficiency improvement. This family encompasses a standard and a folded configuration. In the first case, i.e., the standard configuration, the biasing of the proposed inverter-based OTA is carried out by two pairs of cross-coupled PMOS and NMOS voltage-combiners. In the second case, i.e., in the folded configuration, the biasing is carried out also by two pairs of voltage combiners, yet in a folded configuration biased in current, for proper DC point in lower voltages, e.g., supplies below 1 V.

The schematic of a voltage combiner in its standard configuration is shown in Fig.1, for both PMOS and NMOS flavors. A mixture of two common-drain (CD) devices and two common sources (CS) devices have a frequency response similar to that of a first-order low-pass filter [9].

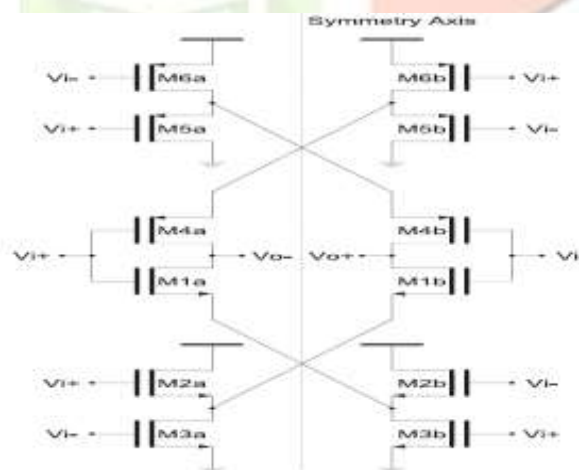


Fig. 4.2. Inverter-based OTA biased by standard VCs.

ii) Inverter-based OTA biased by Folded VCs

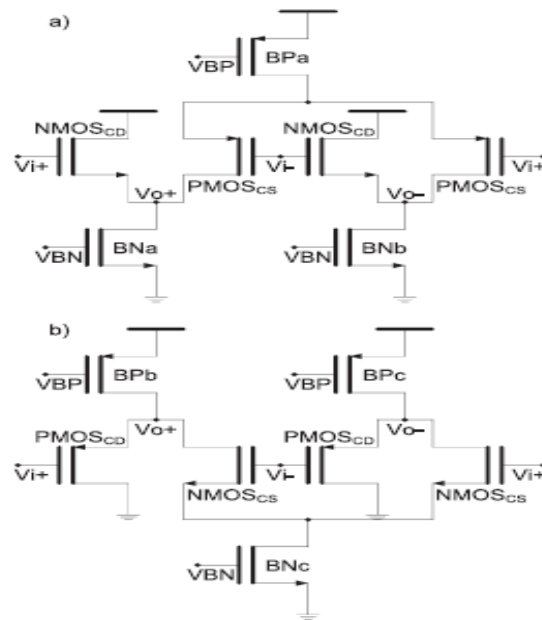


Fig.3. Folded VCs: a) PMOS based; b) NMOS based.

The appropriate response to voltage supplies below 1 V relies on a topology in which the CD and CS devices are folded and are, furthermore, biased by current sources in a fully-differential configuration. The corresponding circuit schematic is shown in Fig. 3, where a doublet of folded voltage-combiners are designed to operate with a nominal supply spanning from 1.2 V down to 0.7 V without stacking issues, i.e., maintaining proper DC biasing. Furthermore, an implementation using low-voltage devices and the intrinsic biasing strategy of the circuit allow for a low current draining with operating point establishment, which otherwise would not be possible for lower supply voltages, e.g., below 1.8 V, using the standard VC approach. The circuit in Fig. 4 employs two PMOS devices in a CS configuration and two folded NMOS devices in a CD configuration, combined with differential input and output. This structure is biased in current by the top and bottom current sources [9]. The gain of the fully-differential folded VC circuit is given by (6), neglecting the body-effect.

The circuit schematic of the proposed folded VC biased CMOS inverter-based OTA is shown in Fig. 4.4. This circuit is compounded by two folded voltage-combiners structures which bias two inverter branches for further gain, as given in (11), and GBW enhancement. Manual design procedure follows the standard approach: establishment of a proper DC operating point (definition of the overdrive voltages and saturation margins); DC current budget in all branches is calculated.

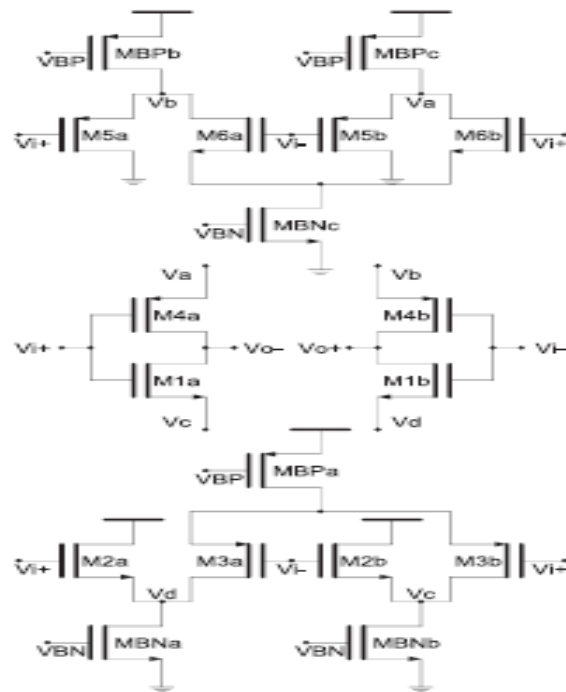


Fig. 4 Inverter-based OTA biased by folded VCs.

III PROPOSED SYSTEM

- This presentation addresses a new family of innovative OTA topologies based on CMOS inverter structures with improved gain and energy-efficiency.
- In particular, two configurations are proposed addressing the both high and low voltage supplies, i.e., supplies above 1.8 V and below 1 V.
- In the first case, a voltage-combiners biased inverter-based OTA proposed with complete freedom from static current sources by properly biasing the devices in voltage through two pairs of cross-coupled voltage-combiners, improving the gain and energy-efficiency of the basic structure
- In the second case, folded voltage combiners biased inverter based OTAs proposed to improve the gain and works with a supplies below 1V.

Folded Cascode OTA

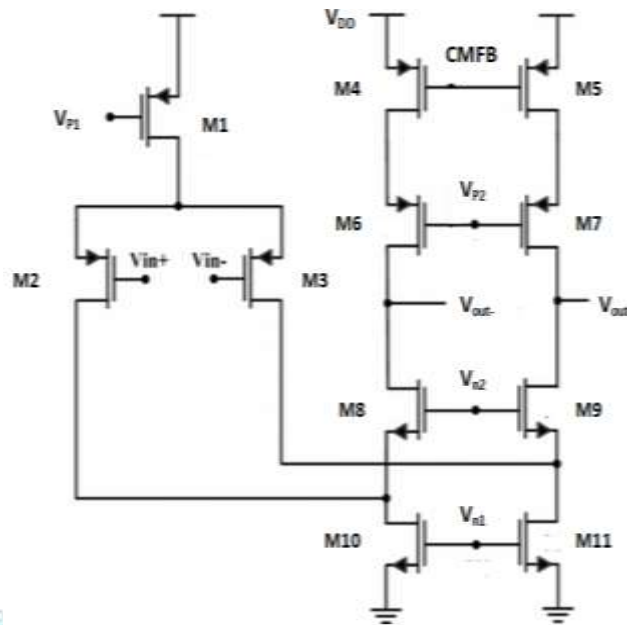


Fig.5. Folded Cascode OTA

The folded cascode OTA shown in fig.5 is folded first stage in PMOS based pull up network for better frequency response and good gain capable of operating at lower potentials of 1.2V, 1V and 0.7V. The second stage is similar to Wilson current mirror which the maximum output voltage is set lower than $V_{DD} + V_T + 2V_{ds,sat}$, so that the output voltage is restored to a minimum fall to $+2V_{ds,sat}$. The current that flows through M_1 , M_{10} and M_{11} is $2I_{SS}$ whereas the current through the transistors M_4 and M_5 is I_{SS} . With a proper bias supply for V_{n1} , V_{n2} , V_{p1} , V_{p2} and V_{CMFB} we get the required improvement in output potential and frequency response.

Advantages over existing system

- Low Power Consumption
- Delay is less
- Speed is high
- Its able to operate at 0.7V,1V,&1.2V

COMPARISON OF RESULTS

After discussing the different parameters of OTA design we can evaluate our study toward other works. The performance of the folded cascode OTA from this work has been compared to Existing methods like folded cascode OTA. This comparison is given in Table I in terms of Power in watts and in Table II in terms of delay in ns. It is clearly seen that with folded cascode OTA architecture, we reach low power low delay in the biasing voltage 0.7V.

The designs are modeled using SPICE Language and the simulated HSPICE tool. The results developed are tabulated in Table I.

Table I: Comparison Table (Power in W)

Methods	OTA	0.7V	1.0V	1.2V
Existing Methods	Standard VCs (PMOS)	0.39 x 10^{-6}	1.2 x 10^{-6}	2.1×10^{-6}
	Standard VCs (NMOS)	9.18x 10^{-15}	1.9x 10^{-14}	2.7×10^{-6}
	Inverted-based OTA biased by standard VCs	1.81 x 10^{-6}	5.66 x 10^{-6}	10.02×10^{-6}
	Folded VCs (PMOS)	5.14 x 10^{-6}	14.2 x 10^{-6}	23.6×10^{-6}
	Folded VCs (PMOS)	4.7 x 10^{-6}	11.05 x 10^{-6}	17.43×10^{-6}
Proposed Method	Inverted-based OTA biased by Folded VCs	9.81 x 10^{-6}	27.7 x 10^{-6}	44.8×10^{-6}

From table I, the proposed method shows an improvement as the supply voltage reduces from 1.2V to 1V and to 0.7V with an improvement of 40.19% and 65.26% respectively.

IV. CONCLUSION

Consequently, the synthesis of high-performance analog integrated circuits constitutes a complex activity requiring the command of many concepts. As a result, the analog designer remains a rare and highly-valued engineer worldwide.

This contribution presents the strategy design of inverter-based OTA biased by folded VCs in the biasing voltages such as 0.7V, 1V and 1.2V. We estimate power consumption in different methodologies. This work has been implemented in HSPICE TOOL.

V.FUTURE SCOPE

Future work would involve the exploitation of these results on folded cascode OTA for low consumption and wide-band applications to use in wide band analog-to-digital converters.

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