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ADC COMPARATOR PERFORMANCE

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***Abstract*:** In the modern world of electronic goods, analogue to digital converters serve as the lock devices. Scientists' interest in the ADC structure grows as the digital signal processing business develops. Today, an ADC is an instance of the system on an IC board rather than a separate signal converter circuit. The demands on the ADC structure in terms of sample speed, power, area, resolution, disturbance, etc. grow as a result. As each day goes by, more innovative theories and techniques are being developed to produce high-performance ADCs. The comparators are therefore regarded to be the fundamental analogue building mode of any flash ADC and have a significant impact on performance. The best ADC performance requires a high level of comparator precision. The performance of the analogue to digital converter (ADC) is observed using a comparator in this paper as well as recent observations on comparator usage in ADC.

Index Terms: **Comparator, low power, high speed, low area**

I. INTRODUCTION

Light, music, and other real-world signals are analogue in nature. Any analogue signal that has to be handled digitally first needs to be transformed from analogue to digital using a circuit defined as an analog-to-digital converter. Depending on whether the input signal's amplitude is higher or lower than a connected signal, a comparator will generate output voltage which is either high or low. It generates a binary output whose value is determined by the matching of the two given analogue inputs. Common comparators fall within the open-loop and dynamic comparators categories and have a variety kind of construction. Functional operational amplifiers are the open-loop comparators [1].

Dynamic comparators match the amplitude of the input and the externally connected signal via positive feedback, which is a flip-flop characteristic. These many forms of comparator, however, are fundamentally common in structure and use a lot of power. Instead of employing a whole analogue block of comparators, a single ended comparator structure can be added as an analogue comparator.

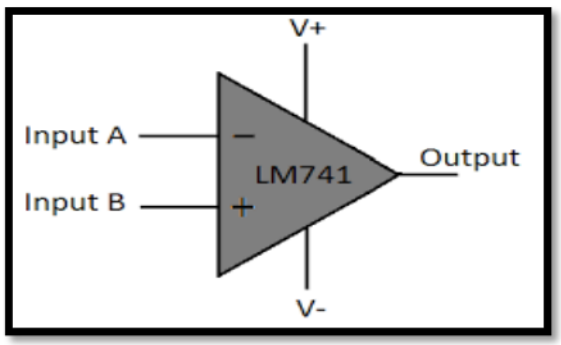

Fig.1: Comparator

II. ADC DEVICE

An ADC is a device that convert an analog signal—which solely takes into account analogue values like voltage and current—into a digital form that can be processed by a computer. The output is a continuous stream of digital values that transformed a constant time and constant amplitude analog signals into a

discrete time and discrete amplitude digital signal. The flash ADC operates with a lower resolution and at a high speed. Due to its parallel execution, it is also referred to as a parallel ADC.

III. LITRETURE SURVEY

Scientists typically focus on the improvement of the comparator circuit as a technique to reduce power consumption and improve the performance matrices of ADC. The research project under consideration under this area takes into account ADC structure employing comparator threshold voltage scaling.

According to **Veera Boopathy et al. 2015 [7]**, double gate MOSFETs have lower leakage current and delay than single gate MOSFETs. The total power utilisation of the inverter, static, dynamic circuit, and latch is higher when compared to a bulk Si single gate device exhibits a factor of over lOX reduction in leakage current and latency when employing a double gate device. In the DG circuit, they analyze and estimate the leakage current dependence of input patterns for static circuits. In terms of input pattern, the Ioff differs from the SG devices by a little margin.

Venkata Ramakrishna et al. 2016 [8] have analyzed that although CMOS technol- ogy scaling increased speed, leakage currents remained as a negative side effect. Stacking is another method for reducing subthreshold leakage currents by connecting transistors in series. By adjusting the voltage at the MOSFET's source terminal, we propose a circuit approach for minimizing MOSFET leakage currents. We offer a circuit approach that uses two extra transistors to reduce leakage currents in sub 100-nm CMOS VLSI circuits.

Sagar Nandrajog et al. 2015 [3] States that the necessity to reduce power dis- sipation for high-end equipment such as Analog to Digital Converters and operational amplifiers is critical in today's scientific environment. Leakage current is a significant contributor to power dissipation. In compared to a charge sharing dynamic latch com- parator, this circuit reduces 68.83 % of total power frequencyat a frequency of 100MHz and reduces latency by 89.6 %. A variety of power reduction approaches, such as MTCMOS, power gating, GALEOR, LECTOR, and others, are available to optimise the power of CMOS devices. To efficiently reduce power dissipation, In our research, we utilised the comparator circuitry using the LECTOR technique.

The technique of using PMOS transistors at the inputs of the first and second stages of the comparator in this circuit was proposed by **Ata khorami et al. 2016 [2]**. The second stage is engaged after the first stage with a predetermined delay during the assessment phase to achieve a regulated pre-amplifier gain. In addition, the first stage is turned off after the delay to reduce overall power consumption. Furthermore, the comparator's offset voltage and power usage are linked to the speed, which is simply regulated by the second stage's delay. As a result, a low-power comparator can be effi- ciently developed for a given offset and speed requirement. Unfortunately, lesser power usage comes at the expense of a significant drop in speed. Another example is the use of NMOS input transistors in a comparator to achieve high-speed behaviour, despite the fact that it increases power consumption by a factor of four.

Preeti Verma et al. 2011 [4] have given the brief idea about the scaling of the threshold voltage in CMOS circuits produces a rise in leakage current below the thresholdLeakage is expected to increase exponentially over the next decade, according to the In- ternational Roadmap of Semiconductors (ITRS). LECTOR is a design method for CMOS gates that reduces leakage current while preserving dynamic power dissipation. The leak- age current and propagation delay of the fundamental CMOS NOT gate were studied in this article.

Dinesh Kumar et al. 2016 [9] described a new 0.18m CMOS architecture for a two-bit magnitude comparator using adiabatic logic that consumes less power. A magnitude comparator is a combination of logic components with a low power requirement. used in low-power applications such as communication and computing processing, as well as analogue to digital converters. The average switching capacitance per cycle, node voltage swing, and supply voltage all affect power dissipation in MOS devices. The power consumption due to transitions is proportional to the square of the supply voltage since the voltage swing is usually equal to the supply voltage.

Monika Gautam et al. 2016 [10] discussed the rising clock frequency and complex- ity of high-performance VLSI devices has resulted in a significant increase in power con- sumption, which has proven to be a key impediment to the realisation of high-performance designs. Although these energy dissipation benefits come at the expense of reduced dy- namic performance, when speed isn't as important as low power, the sequential circuits achieved by ICAL logic are a good choice.

Sagar Kumar Vinodiya et al. 2017 [11]. Due to the growing demand for low-power, high-speed analog to digital converters (ADCs), various comparator types were examined and their simulated results were compared. This motivates the development of CMOS comparators that can run at maximum speed at low supply voltage while maintaining excellent power efficiency. In most high-speed ADCs, the comparator is a critical component. Comparators are critical components in modern communication and biological systems because they connect the analogue and digital worlds.

Srinivasa Rao Vemu et al. 2018 [12] discussed about how dynamic comparator is the vital building block of analog to digital converter. In order to increase power efficiency and speed, dynamic renewable comparators require energy-efficient and high-speed ADC. By changing the comparator design, power leakage is reduced, which reduces the circuit's power and delay even further.

Harshita Kushwaha et al. 2021 [13] The design of a low-power, high-speed comparator was described. The design is aimed for SAR ADC implementation. The term "clocked comparator" refers to a dynamic comparator that utilizes latch. The purpose of latching is to provide positive feedback and to facilitate application.

IV. Parameter Check

The comparison of the current comparator on the basis of their effectiveness is presented in the following table.

Table I: Comparison Summary

Parameter	Resolution	Architecture	Technology	DNL (LSB)	INL (LSB)	Voltage Supply	Power Dissipation	Samples/sec.	Ladder Network
Year 2017	6-bit	Flash	65nm	0.3	0.6	1.2 V	2.1 mW	1G	NO
Year 2018	6-bit	Flash	90nm	0.5	0.96	0.9 V	98 mW	3.5G	YES
Year 2021	6-bit	Flash	130nm	0.4	0.6	1.2 V	90 mW	600M	YES
Year 2014	6-bit	Flash	65nm	0.5	0.5	1.2 V	12mW	800M	YES
Year 2015	6-bit	Flash	250nm	-	-	2.5 V	66.8mW	1G	NO

V. CONCLUSION AND FUTURE SCOPE

We eliminated certain comparisons when studying high speed comparator. The coupling capacitance of the comparator is the sole factor that can be used to choose a virtually resistance value because the the worst Nyquist frequency is equal input signal frequency. The capacitance at the comparator mode's input increases as the number of bits does as well. The associated value will vary owing to noise and disturbance if the

sampling speed is rapid enough, and the comparator will match the wrong entries if the obstruction value is fixed to increase the amount of bits. This will lower the overall output of the design.

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