



Study and Analysis of New Three-Phase Modular Multi-Level Inverter

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Abstract—this paper proposes a new three-phase modular multi-level inverter (MMLI). The proposed inverter consists of repeated modular primary cells that are connected in series configuration. Therefore, the proposed topology can be extended to get more output voltage levels by adding additional cells without increasing voltage stresses across power switches. Both sinusoidal pulse width modulation (SPWM) and staircase modulation are successfully applied to the proposed inverter. The proposed inverter features many advantages such as reduced number of semiconductor power switches, driver circuits, dc-voltage sources, simplified control algorithm, and reduced voltage stresses across the switches independent of output voltage level. Furthermore, the performance of the proposed inverter is studied under both open-loop and closed-loop operations for highly inductive load. Beside the obtained simulation results, a laboratory prototype has been carried out and tested to verify the control techniques and performances of the topology. Simulation and experimental results are compared together to highlight the similarity and consistence of them.

Index Terms—Modular multi-level inverter, reduced dc-voltage sources count, sinusoidal pulse-width modulation.

I. INTRODUCTION

CURRENTLY, renewable energies sources (RESs) have gained great interest in worldwide to find vital solutions for world energy crisis and pollution reduction. RES can solve the problems of the increased electrical loads on the utility grid and providing electricity for remote areas as well. The increasing number of RESs and distributed generations (DGs) require new technologies for the operation and management of the electrical power transferred between RESs and customers, in order to maintain and improve the power-supply reliability and quality that match the international standard requirements. [1], [2].

One of the main developments in the RES systems is the im-

provement in the power converters, which have the pivotal role to convert the raw generated energy to the loads/utility grid. Consequently, the classical inverters like DC-AC converters, and DC-DC converters are substituted by more stimulated topologies that aim to increase system reliability, efficiency, life time, and to decrease system size

and cost [3], [4].

Among the promoted converters topologies, multi-level inverters (MLIs) have characterized by many features such as generating output voltage with extremely low THD, reduced output filter size, low dv/dt , low electromagnetic interference (EMI), and increased system efficiency due to its operation with fundamental switching frequencies. Moreover, using MLIs lead to eliminate the boosting stage on the input side of the inverter and remove the power transformer at the output AC side [2], [5]–[13].

The various topologies of MLIs can be categorized into two main groups named as single dc-voltage source MLIs and multi dc-voltage sources MLIs. Single dc-voltage source have only one dc-voltage source, and many capacitors and diodes. It has not the capability of voltage boosting since the output peak AC voltage has to be the same as the input dc-voltage source value [14]. Furthermore, the control algorithm of single dc-voltage source encounters many difficulties than multi-sources category as it needs capacitors voltage balancing techniques. On contrary, multi-dc voltage sources MLIs have many dc-voltage sources and reduced number of capacitors and clamped diodes. It features several merits such as high modularity degree, simple cell structure, and reduced manufacturing costs. In addition, when a fault is occurred in one of these cells, the faulty cell can be replaced easily without affecting the healthy ones.

In the literature, there are many different topologies of MLIs are addressed. In [15], the authors presented multilevel dc link topology (MLDCL). It was constructed by connecting half H-bridge cells in series configuration, and a main cascaded H-bridge stage connected across them to change the produced voltage polarity. However, this MLI topology needs an increased components count compared to the conventional topologies, besides there is a high voltage stresses across switches. While, in [16], the authors presented three phases asymmetrical multilevel cascaded inverter, where the output voltage different levels were generated by connected cells in series. It used the phase-shift between the inverter three legs to produce the line voltage in place of using H-bridge to get the AC-voltage different polarities as in [15]. Nonetheless, this topology suffering from increased number of dc-voltage sources and power switches to generate extra voltage levels.

In [17] and [18], many improved cells were formed by merging well-known cells such as full bridge or half bridge connected in series, parallel, or in cross configurations. The formed cells such as clamp-double cell, T-connected NPC, and alternative active 3-LNPC were aiming to overcome the basic cells demerits. However, they are also suffering from electrolytic capacitors limitations such as increased inverter size, reduced inverter life time, and complicated control techniques for voltage balancing over capacitors. To overcome some of these limitations, the authors in [19] introduced the double sub-module cell, that aiming to improve voltage balancing across capacitors at low-switching frequency. But it needs more components count when it is compared to half bridge module.

On another side, many topologies as in [20] were introduced to utility scale applications. It principally uses a DC-AC converter equipped with a medium frequency transformer that has the function to transform the DC input voltage into three AC isolated voltages. However, this configuration suffers from increased components counts, increased EMI noise, reduced efficiency, and decreased power density. In [21], a MLI consisting of high-voltage primary stage linked with low-voltage secondary stages was introduced. Practically, this topology is effectively suitable in medium-voltage applications. It has low utilized components count as dc-voltage sources and power switches. However, it appears to have high conduction losses as the zero-voltage state in the pole waveform requires $(n-1)$ switch to be in ON-state.

In [22], the authors introduced three-phase MMLI. Basically, it used a reduced components count to produce the necessary voltage levels across the output terminals. However, it has some limitations for applying this topology on high voltage applications since the voltage stresses on the utilized power switches are increased as cells number increased. On another side, in [23], a new MLI topology is proposed, it required six dc-voltage sources, nine power switches, and three power diodes to produce three voltage levels across the pole terminals. It needs high components count. Additionally, it is not applicable for inductive loads as the location of the power diodes are preventing the freewheeling currents. Moreover, this topology is expected to have increased power losses due to diodes existing.

It is apparent from the above mentioned topologies that an extra developments and improvements on the MLIs power and/or control stages need to be done, as almost all of them need large number of the components count, dc-voltage sources, and electrolytic capacitors. This paper proposes a new MLI topology that exhibits reduction in the components count compared to the addressed topologies, without changing the output voltage levels number. In addition, the proposed topology has the feature of its switches has reduced stresses irrespective to output voltage levels.

This paper is structured as follows: the configuration and the operation of the proposed inverter is introduced in section II. The switching schemes are demonstrated based on three levels per pole case-study in section III. While both simulation

and experimental results are provided in section IV. A comparison between the proposed topology and the addressed MLIs is offered in section V. Finally, summary is provided in section VI.

II. PROPOSED MLI TOPOLOGY CONFIGURATION

A. Generalized Power Circuit

The generalized three- phase configuration of the proposed MMLI for n levels across the pole voltage is demonstrated in Fig. 1(a). The proposed topology consists of $(n-1)/2$ basic modular cells, $(n-1)$ isolated dc-voltage sources, and $(6n-6)$ switching devices, and no electrolytic capacitors or power diodes are required. The basic cell is constructed by combining Two conventional three- phase voltage source inverters (VSIs) in distinct manner to build a new cell that able to generate three voltage levels across the output terminals (T_1 and T_2 , T_3 and T_4 , T_5 and T_6) as shown in Fig. 1(b).

The basic cell utilizes two dc-voltage sources along with twelve switching devices. Through repeating this cell in cascading configuration, the output levels number can be increased to n levels as shown in Fig. 1(c). It is worth mentioning that increasing the number of cells is not affecting the voltage stresses over the power switches. Therefore, the proposed topology is much appropriate for low, medium, and high voltage applications as well.

B. Case-study Circuit

So as to investigate the operation and performance of the proposed MLI, a basic cell has been designated to form the case-study circuit that is shown in Fig. 2. The operation of proposed inverter can be explained as follows: when S_1 is in ON-state a $(2E)$ volt is produced across the pole (V_{A0}), whereas, when S_2 and S_3 are in ON-state, (E) volt is applied across the pole. In order to generate the (0) volt across the pole (V_{A0}), both S_2 and S_4 should be turned on while S_1 and S_3 are turned off.

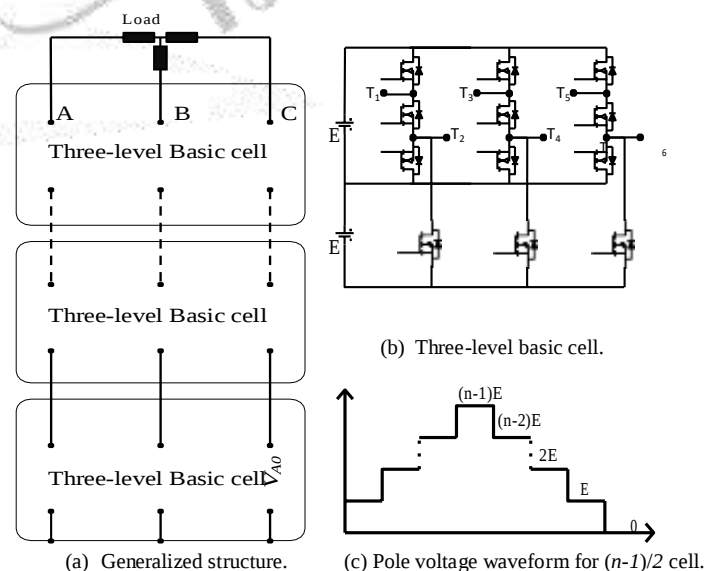


Fig. 1. Proposed three-phase symmetrical MLI.

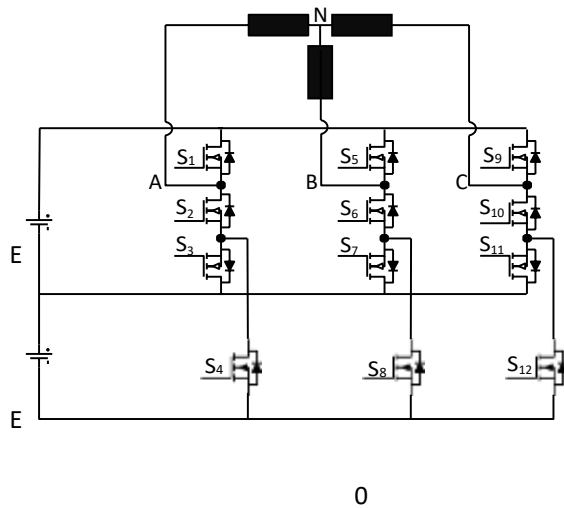


Fig. 2. Proposed three phases MLI (Case-study).

It is notable that for each basic cell, there are three switching states are not allowed in the switching algorithm to avoid short-circuit across the used dc-voltage sources. These states are a) S_1 , S_2 , and S_3 are in ON-state, b) S_1 , S_2 , and S_4 are in ON-state, and c) S_3 , and S_4 are in ON-state.

III. THE PROPOSED MLI TOPOLOGY MODULATION TECHNIQUES

The modulation techniques of the MLI are classified to two main groups, according to switching frequency: (a) Low-frequency modulation techniques such as (staircase modulation, selective harmonic elimination (SHE)), (b) Pulse-width modulation (PWM) techniques, such as (sinusoidal pulse-width modulation (SPWM), space vector pulse-width modulation (SVPWM), sub-harmonic pulse-width modulation (SH-PWM), or switching frequency optimal pulse-width modulation (SFO-PWM). It should be noted that, modulating the MLIs using high switching frequencies techniques that based on the carrier signals are properly increasing switching losses compared to low frequencies modulations [24]-[26].

So, in this paper two modulation schemes are investigated to achieve the sinusoidal waveforms on the output: (a) low-frequency modulation scheme, (b) sinusoidal pulse-width modulation (SPWM) scheme. Both of them are described in the following subsections. It is worth noting that any other technique for high frequency can be applied to the proposed

topology, however SPWM is chosen here as a case-study.

A. Low-Frequency Modulation Scheme

Low-frequency modulation techniques are preferred in MMLIs, since the switching losses are minimized due to its operation with low-frequency. Either SHE or the staircase modulation can be applied to MMLIs, however the staircase

modulation is preferred in the MLI control than SHE, because the switching angles calculations in SHE become more complex as the number of output voltage levels increases. Compared to SHE, the performance of staircase

modulation is comparable and its implementation is not complicated [27]. The suggested MLI has twelve modes of operation per one cycle (50 Hz) as shown in Table I.

B. Sinusoidal pulse width modulation (SPWM)

As mentioned previously, the SPWM is categorized as carrier based modulation strategies. The direct way to generate the SPWM signals is to compare a sinusoidal waveform with high frequency carrier signals. The comparing operation will generate the Boolean signals that it used to synthesize control-pulses of switches. Since the phase disposition (PD) scheme achieves the lowest THD on the line-to-line voltage, as addressed in [28], [29], the applied modulation pattern on the proposed topology is based on PD scheme where all carriers are in phase. In this scheme, for obtaining n output voltage levels a $(n-1)$ carrier signals with the same frequency and amplitude are required. Therefore, in the investigated case-study, two triangular carrier signals are selected and compared with a sinusoidal modulation signal to generate the main signals G_1 and G_2 as shown in Fig. 3. By executing few logical processes on these two control signals, the required switching pulses S_1 , S_2 , S_3 , and S_4 can be generated as specified in (1) to (4) for leg A. By using sinusoidal signals shifted in phase by -120° and 120° the above process is repeated for leg B, and leg C respectively.

$$S_1 = G_2 \quad (1)$$

$$S_2 = \overline{G_2} \quad (2)$$

$$S_3 = (G_1 \times \overline{G_2}) \quad (3)$$

$$S_4 = \overline{G_1} \quad (4)$$

TABLE I
DIFFERENT SWITCHING STAGES OF THE PROPOSED MLI TOPOLOGY

States	V_{AB}	V_{BC}	V_{CA}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	E	$-2E$	E	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
2	$2E$	$-2E$	0	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
3	$2E$	$-E$	$-E$	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	ON	OFF
4	$2E$	0	$-2E$	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON
5	E	E	$-2E$	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON
6	0	$2E$	$-2E$	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON
7	$-E$	$2E$	$-E$	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON
8	$-2E$	$2E$	0	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON
9	$-2E$	E	E	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF
10	$-2E$	0	$2E$	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
11	$-E$	$-E$	$2E$	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
12	0	$-2E$	$2E$	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF

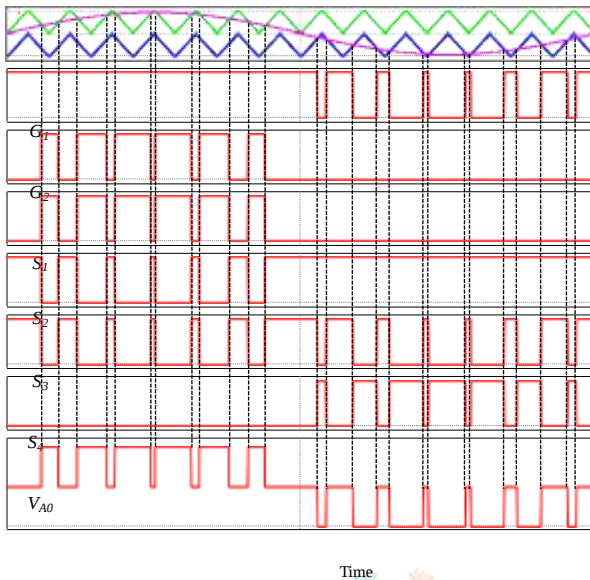


Fig. 3. Switching patterns and the pole voltage (V_{A0}) of the proposed MLI.



Fig. 4. Experimental setup of the proposed MLI.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Both of the simulation and experimental results are conducted to validate the operation of the proposed topology for the aforementioned switching schemes. *MATLAB/Simulink* environment is used to carry out the simulation model. The *AOT22N50L* metal-oxide-semiconductor field-effect transistor (*MOSFET*) is used to setup the laboratory inverter prototype. The control algorithms are executed by using the digital signal processor (*DSP*) of type *TMS320F28335*.

Fig. 4 shows the proposed *MLI* experimental setup, which includes two dc-voltage sources, twelve switching devices, measurement tools (i.e. current probe, voltage probes, and oscilloscope), *DSP* controller, voltage sensors kit, and three-phase resistive-inductive load. All system specifications are listed in Table II.

The pole voltages V_{A0} , V_{B0} , and V_{C0} are demonstrated in Fig. 5, and it is considered as the key elements in the operation of the proposed inverter. The three line-to-line voltages are obtained from these three pole voltages as in (5).

$$\begin{aligned} V_{AB} &= V_{A0} - V_{B0} \\ V_{BC} &= V_{B0} - V_{C0} \\ V_{CA} &= V_{C0} - V_{A0} \end{aligned} \quad (5)$$

TABLE II

SYSTEM SPECIFICATIONS		Value
Two dc-voltage sources		80 volt/each
Load value (at 50 Hz)		$R=30\ \Omega$, $X_L=45.8\ \Omega$
Switching Frequency (f_s)		3 KHz
Open loop	Modulation Index (m_i)	0.9
Closed-loop	Reference voltage	$V_{ref}=120\text{ V}$
	PI parameters	$K_p=0.001$, $K_i=5$
	Step-change percent	100%

By this manner, the three voltage levels in the pole voltages are producing five-level in the line-to-line voltages V_{AB} , V_{BC} , and V_{CA} waveforms (i.e. $2E$, E , 0 , $-E$, $-2E$) as shown in Fig. 6, where each one of them have five voltage levels and shifted by phase angle equal to 120° from each other. However, the load-phase voltage (V_{AN} , V_{BN} , and V_{CN}) are related to the pole voltages (V_{A0} , V_{B0} , and V_{C0}) as in (6) [30].

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \times \begin{bmatrix} V_{A0} \\ V_{B0} \\ V_{C0} \end{bmatrix} \quad (6)$$

The number of voltage levels across the load-phase voltage is seven i.e. (0 , $2E/3$, E , $4E/3$, $-2E/3$, $-E$, and $-4E/3$) according to (6) and it is shown in Fig. 7.

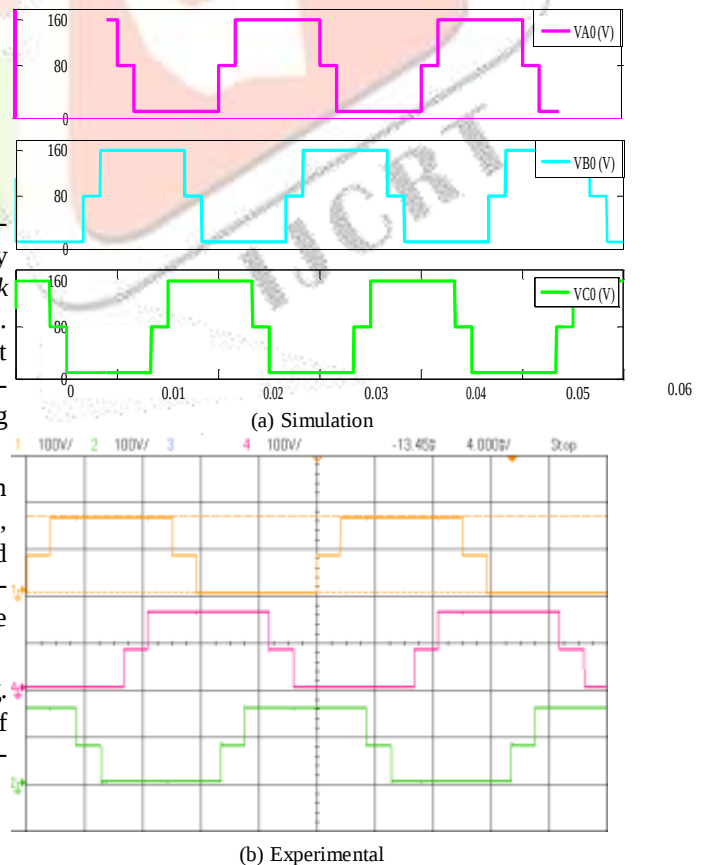


Fig. 5. Pole voltages (V_{A0} , V_{B0} , V_{C0}) with low-frequency modulation technique

The ability of the proposed topology to feed $R-L$ load is illustrated in Fig. 8 which shows the line-to-line voltage (V_{AB}), the load-phase voltage (V_{AN}), and the load current for phase A (I_A), respectively.

In addition, the performance of the proposed inverter under $SPWM$ is demonstrated as shown in Figs. 9, 10 and 11. The output line-to-line voltages are demonstrated in Fig. 9(a) and (b) for the simulation and experimental results respectively. Also, Fig. 10 shows the load-phase voltages (V_{AN} , V_{BN} , and V_{CN}), which have nine levels (i.e. 0 , $E/3$, $2E/3$, E , $4E/3$, $-E/3$, $-2E/3$, $-E$, and $-4E/3$). It is different from the load-phase voltage-

es under staircase modulation which previously shown in Fig. 7 (in Fig.7 load-phase voltages have only seven levels). Two extra levels are appeared on the load-phase voltages waveforms (i.e. $E/3$, $-E/3$). This can be clarified by using (6) to deduce the load-phase voltages from the poles voltage when the $SPWM$ scheme is applied. These states cannot appear in the pole voltages under staircase modulation (as shown in Fig. 5). This new possibility will produce an extra two levels on load-phase voltages. The new two pole voltages combination states are listed in Table III.

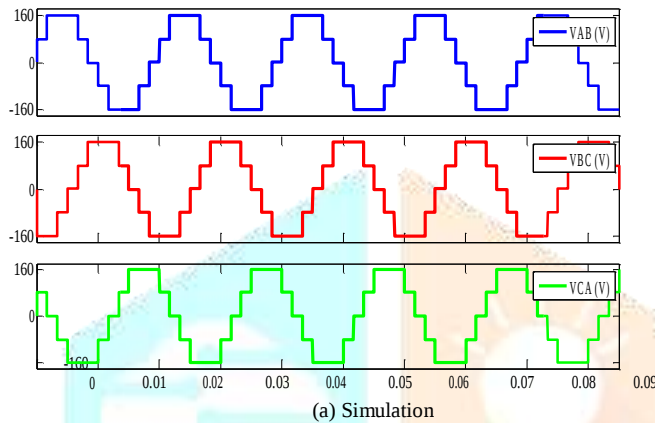


Fig. 6. Output line-to-line voltages (V_{AB} , V_{BC} , and V_{CA}) with low-frequency modulation technique.

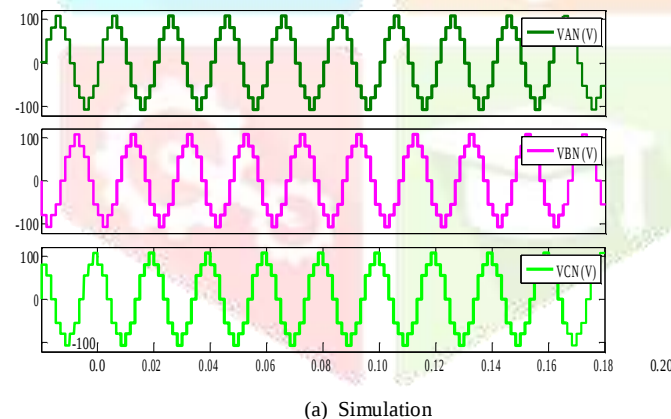
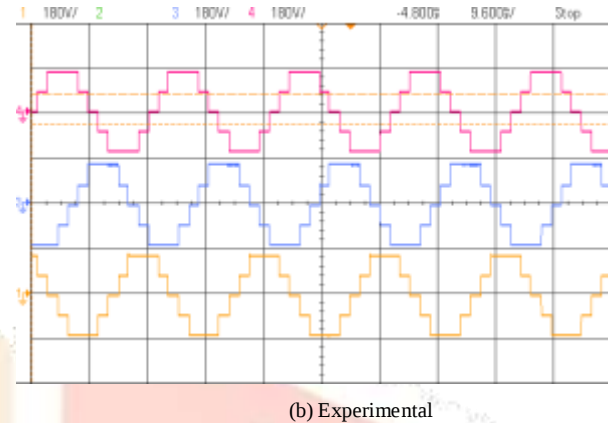


Fig. 7. Output load-phase voltages V_{AN} , V_{BN} , and V_{CN} with low-frequency modulation.

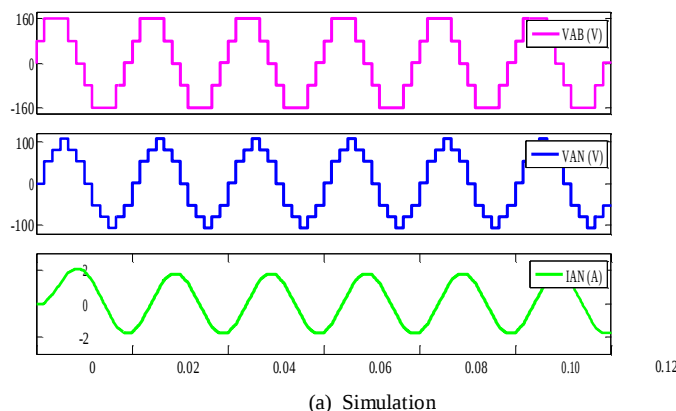
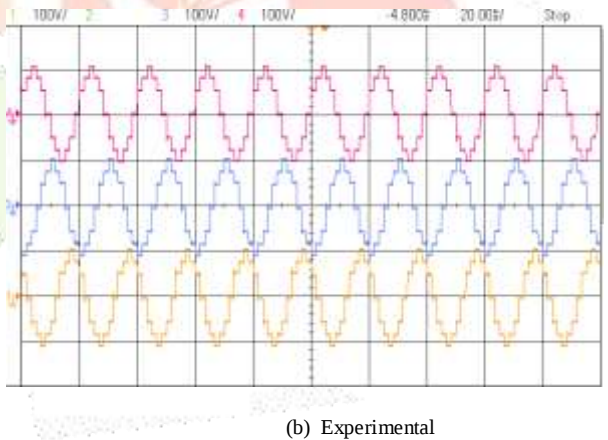


Fig. 8. Inverter outputs with $R-L$ load (V_{AB} , V_{AN} , and I_{AN}) with low-frequency modulation.

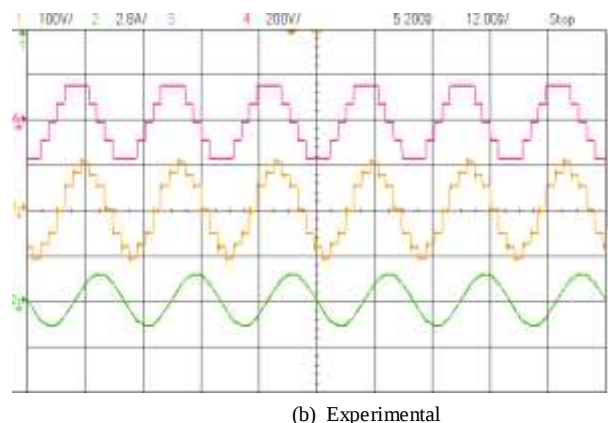
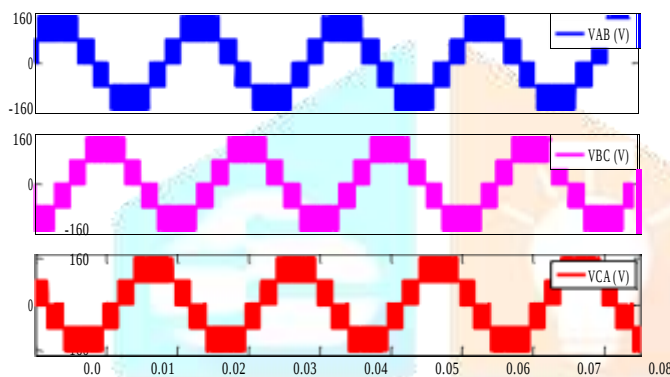


TABLE III
TWO EXTRA STAGES THAT APPEARED IN SPWM AND THE CORRESPONDING
LOAD-PHASE VOLTAGES

State	V_{A0}	V_{B0}	V_{C0}	Load-phase voltage according to (6)
State one	E	0	E	$V_{AN} = \frac{2E - 0 - E}{3} = \frac{E}{3}$
State two	E	E	$2E$	$V_{AN} = \frac{2E - E - 2E}{3} = \frac{-E}{3}$

Furthermore, the proposed topology performance under both highly inductive/capacitive loads is examined. Figs. 11(a) and (b) show the simulation obtained results of the proposed circuit operation under highly inductive/capacitive loads, respectively. Results demonstrate the ability of the proposed circuit to operate under these different modes and keep the waveforms of the output voltage with multi-level. It is worth noting that the load current is smoother in the case of highly inductive load.

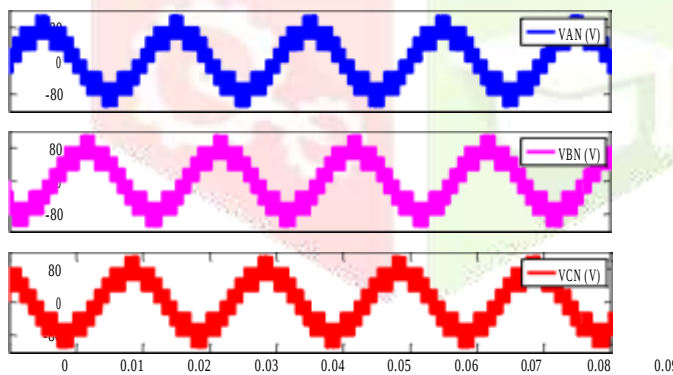


(a) Simulation

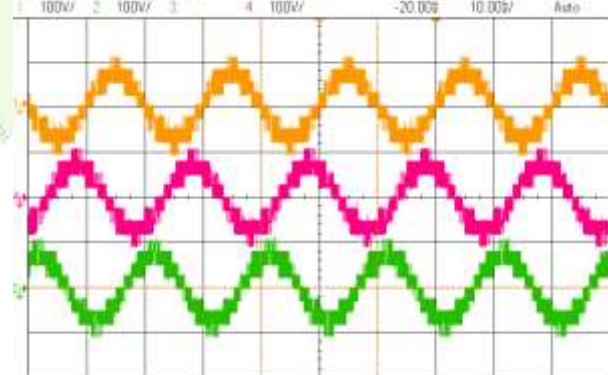


(b) Experimental

Fig. 9. Output line-to-line voltages V_{AB} , V_{BC} , and V_{CA} for SPWM scheme, $m_i = 0.9$ and $f_s = 3$ kHz.

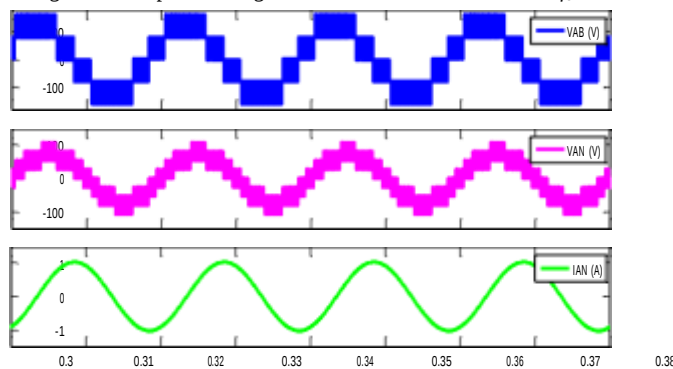


(a) Simulation

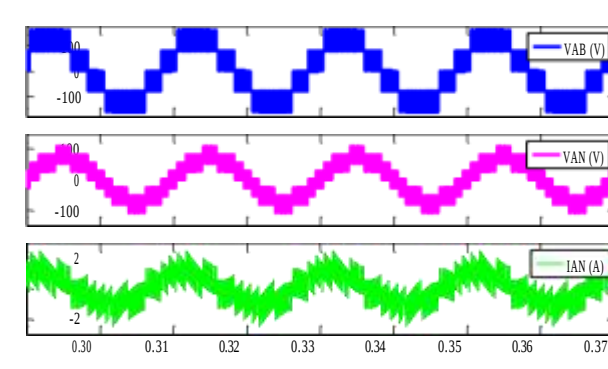


(b) Experimental

Fig. 10. Load-phase voltages for SPWM scheme, $m_i = 0.9$ and $f_s = 3$ kHz.



(a) Highly inductive load ($R = 30\Omega$, $X_L = 63\Omega$).



(b) Highly capacitive load ($R = 30\Omega$, $X_C = 63\Omega$).

Fig. 11. Inverter outputs: line-to-line voltage V_{AB} , load-phase voltage V_{AN} and the phase current I_{AN} , for SPWM scheme, $m_i = 0.9$ and $f_s = 3$ kHz.

For modulation index $m_i = 0.9$, the THD of the line-to-line voltage waveform (V_{AB}) is found to be 39.31% as illustrated in Fig. 12(a). The THD value is decreased due to increasing of modulation signal (m_i). Fig. 12(b) shows the THD for the line-to-line voltage against m_i variation.

The overall efficiency of the proposed MLI has been investigated experimentally with different loading and different modulation indexes as shown in Fig. 13 and Fig. 14, respectively. The efficiency is recorded for both low-frequency case and $SPWM$ case ($m_i = 0.9$, $f_s = 3$ kHz and full load power of 360W). Then, the same test is repeated at 50% load. It is clear that the converter exhibits high efficiency with increasing the load. Peak experimental efficiency of more than 98% for low-frequency and more than 93% for $SPWM$ have been recorded.

These high efficiency values are occurred as a result for the low on-resistance of the used *MOSFET* switches (R_{ds-on} is about 0.3Ω). In addition, it is clear that efficiency for the low-frequency control case is higher than that of *SPWM* due to lower switching losses. Then, to examine the effect of the modulation index on the system efficiency, the *SPWM* control has been adjusted to vary the modulation index from 0.3 to unity and the inverter efficiency is recorded as shown in Fig. 14. The peak recorded efficiency is more than 97% at unity modulation index.

The performance of the suggested *MLI* for stand-alone applications is improved by using a proportional integral (*PI*) controller. The *PI* controller is designed to regulate the load voltages with the reference voltage (V_{ref}). The closed-loop system is successfully designed and simulated via *MATLAB* software tool. The parameters of the overall closed-loop system are listed in Table II. Fig. 15 shows the architecture of the closed-loop system.

The simulation and the experimental results of the closed-loop performance of the proposed inverter under *R-L* load with load step change are shown in Fig. 16. Fig. 17 shows good inverter dynamic performance, the output voltage attains its value under the step change of the load current.

V. COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND OTHER *MLIs*

In order to confirm the achievability of the proposed *MLI*, it is compared with *MLIs* topologies recently published and addressed in [15]-[23] and [31]. All addressed topologies have

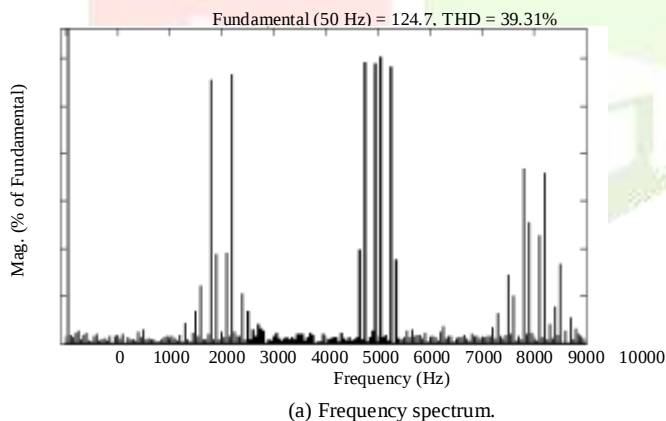


Fig. 12. Total Harmonic Distortion of line voltage (*THD*).

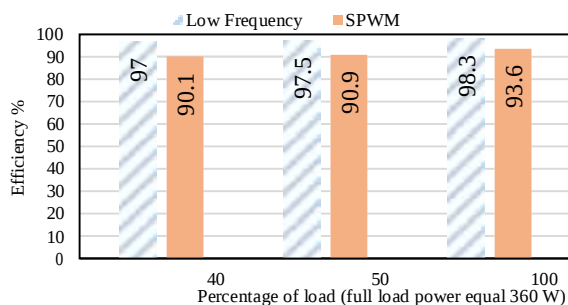


Fig. 13. Experimental inverter efficiency for the two proposed switching techniques (low-frequency versus *SPWM*, $m_i = 0.9$) at different load percentage.

been adapted to produce identical number of the voltage levels per pole (n) such as 0, E , $2E$. The comparison strategy is based on the count of the required components i.e. switching devices, electrolyte capacitors, power diodes, and dc-voltage sources. In order to hold a reasonable comparison between the addressed topologies, the count of all switches and diodes are based on the peak voltage stress (E). However, the count of electrolytic capacitors has been done according to the multiplication of capacitance voltage ratings (CE). Moreover, the count of dc-voltage sources and power transformers has been done based on their voltage-ampere ratings (VA). In these comparison, all system components are assumed to be rated with the load peak currents.

All components rating have been normalized to the pole step voltage (E). For example, in [18], this topology requires one voltage source with voltage rating equals ($2E$) which is equivalent to two equal dc-sources each of them rated by (E). Therefore, this topology is considered to have two dc-voltage sources as shown in Table IV. On the other hand, this topology uses 12 switches, 6 of them have a voltage stresses equal ($0.5E$), and the others withstand a voltage stresses equal ($2E$). Therefore the equivalents number of switch is $(6 \times 0.5E + 6 \times 2E)/E$, which equals 15 switches. This means that, the 12 switches with different voltage stresses are equivalent to 15 switches with equal voltage stress (E). Therefore, by monitoring Table IV, the proposed topology requires only two dc-voltage sources, and 15 switches to produce three voltage levels across the pole terminals. In addition, the necessity of electrolyte capacitors and the power diodes are eliminated.

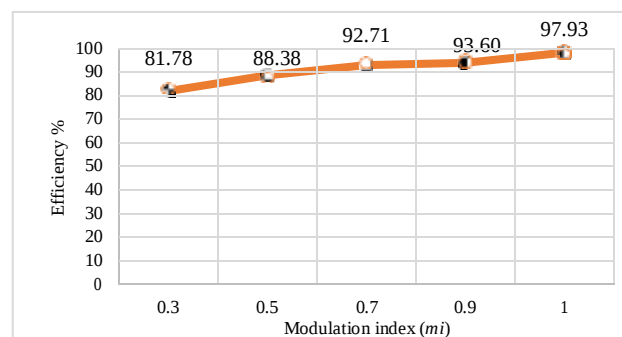
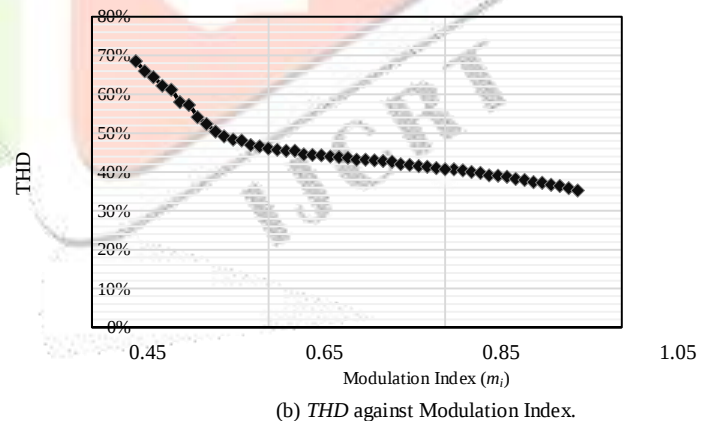


Fig. 14. Experimental inverter efficiency at different modulation index, $R = 23.15\Omega$, $V_{in} = 160V$ and $f_s = 3\text{ kHz}$.

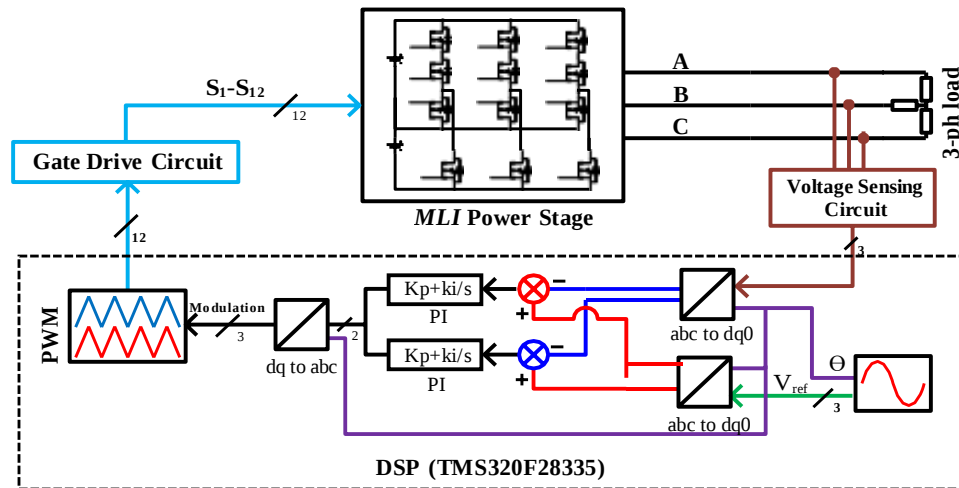


Fig. 15. Implementation blocks for the closed-loop system.

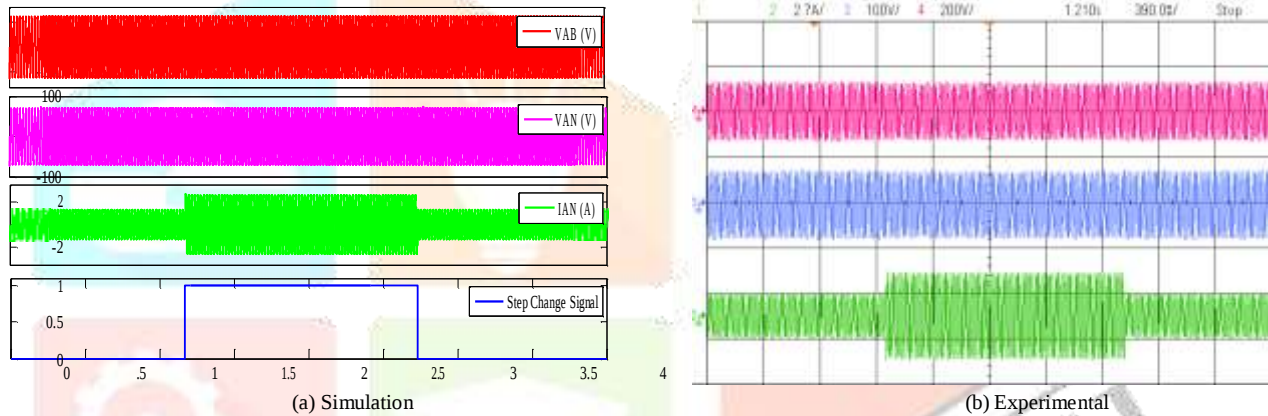
Fig. 16. Line-to-line voltage, load-phase voltage and the phase current under R-L Load of the proposed multi-level inverter at $V_{ref}=120$ V (Peak Value) under step change: wide-range view.

TABLE IV

COMPARISON OF THE PROPOSED INVERTER WITH OTHER ADDRESSED MLIS. (N_{DC} : NUMBER OF DC-VOLTAGE SOURCES, N_{SW} : NUMBER OF SWITCHES, N_D : NUMBER OF DIODES, N_C : NUMBER OF CAPACITORS, N_{TRS} : NUMBER OF TRANSFORMERS, AND NTE: NORMALIZED TO E)

Topology	N_{Dc}		N_{Sw}				N_D			N_C			N_{Trs}	
	Num.	NTE	Num.	Voltage Stress		NTE	Num.	Voltage Stress	NTE	Num.	Voltage Rating			NTE
[15]	$3 * E$	3	18	$6 * E$	$12 * (n - 1/2) E$	18	0	0	0	0	0	0	0	0
[16]	$6 * E$	6	12	$12 * E$	0	12	0	0	0	0	0	0	0	0
[17] Primary cell based on FC	$1 * 2E$	2	12	$12 * E$	0	12	0	0	0	6	$3 * E$	$3 * 2E$	9	0
[17] Primary cell based on NPC	$1 * 2E$	2	12	$12 * E$	0	12	6	$6 * E$	6	6	$6 * E$	0	6	0
[17] Clamp double	$1 * 2E$	2	15	$15 * E$	0	15	6	$6 * E$	6	6	$6 * E$	0	6	0
[18] T-connected NPC	$1 * 2E$	2	12	$6 * 0.5E,$	$6 * 2E$	15	0	0	0	6	$6 * E$	0	6	0
[18] Alternative Active 3-L NPC	$1 * 2E$	2	18	$18 * E$	0	18	0	0	0	6	$6 * E$	0	6	0
[19]	$1 * 2E$	2	24	$24 * E$	0	24	0	0	0	6	$6 * E$	0	6	0
[20]	$1 * E$	1	28	$24 * 0.5E$	$4 * E$	16	0	0	0	0	0	0	0	3
[21]	$4 * E$	4	12	$12 * E$	0	12	0	0	0	0	0	0	0	0
[22]	$4 * E$	4	12	$9 * E$	$3 * (n - 1) E$	15	0	0	0	0	0	0	0	0
[23]	$6 * E$	6	9	$6 * 2E$	$3 * E$	15	3	$3 * E$	3	0	0	0	0	0
[31]	$2 * E$	2	12	$9 * E$	$3 * (n - 1) E$	15	0	0	0	0	0	0	0	0
Proposed	$2 * E$	2	12	$9 * E$	$3 * 2E$	15	0	0	0	0	0	0	0	0

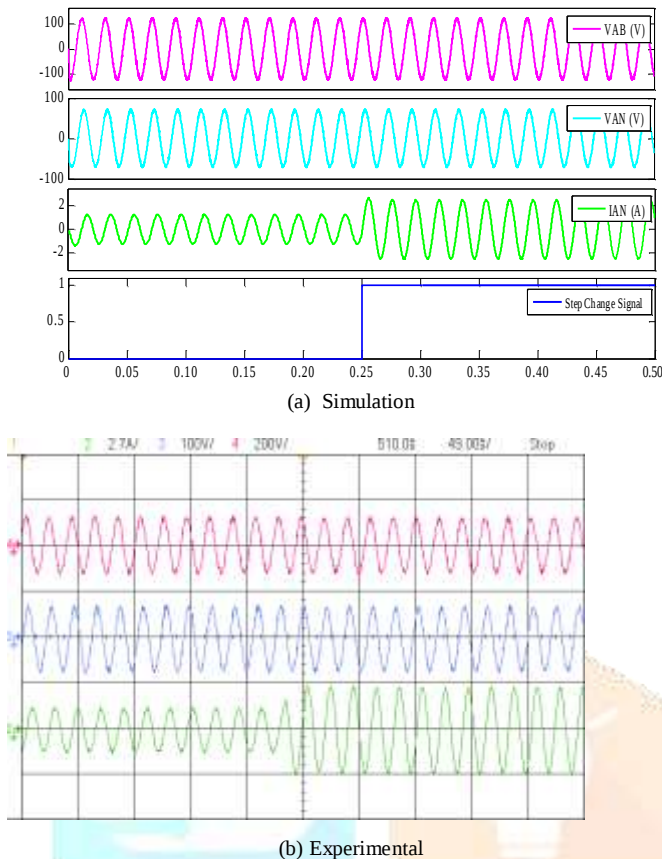


Fig. 17. Line-to-line voltage, load-phase voltage and the phase current under R - L Load of the proposed multi-level inverter at $V_{ref}=120$ V (Peak Value) under step change: narrow-range view.

VI. CONCLUSION

A new three-phase modular *MLI* topology is proposed. The suggested inverter when compared with the other *MLI* topologies, gains many advantages such as it utilizes reduced dc-voltage sources number and low switching devices count.

In addition, it does not require any electrolytic capacitors or power diodes, so their limitations are eliminated. Moreover, the proposed topology can be extended to n voltage levels without increasing the voltage stresses across the power switches. Therefore, it is suitable to low, medium, and high voltage applications. It exhibits modularity shape, simplified control algorithm, and small inverter footprint. Both staircase modulation and *SPWM* are applied effectively. In order to examine the performance of the proposed *MLI* topology, a three-level case-study is simulated, and its prototype has been implemented and tested for both open-loop and closed-loop operations.

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