IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Design of an Energy Efficient multiplexer using Adiabatic Diode Logic for Low Power Applications

[1] Aswini Addepalli, [2] Satya Sri, [3]Anjali U , [4]Siva Priya. E, [5]K.N.V.S.VIJAYA LAKSHMI

[1]Under Graduate Scholar [2] Under Graduate Scholar, [3]Under Graduate Scholar, [4] Under Graduate Scholar, [5] Assoc Professor

[1]Electronics and Communication Engineering,

[1]ISTS Women's Engineering College, Rajahmundry , India

Abstract: ***Power*** consumption and delay optimization has been the main concerns for the VLSI technology. In this project, we propose a new adiabatic technique using diode-connected transistors. This technique emphasizes on reduction of power by lowering the non-recoverable power consumption in adiabatic circuits. This technique achieves full adiabatic operation by providing separate charging and discharging paths. The PMOS devices provide the charging path while the diode-connected NMOS devices provide a low-resistance discharge path which helps in the reduction of power dissipation in the circuit. In this project, we have used the T-Spice tool to implement.

Index Terms **– Adiabatic Logic, CPL, PFAL, EEPL, ADDL, T-Spice.**

I. INTRODUCTION

''Adiabatic'' is a term of Greek origin that has spent most of its history associated with classical thermodynamics. It refers to a system in which a transition occurs without energy (usually in the form of heat) being either lost to or gained from the system. In the context of electronic systems, rather than heat, the electronic charge is preserved. Thus, an ideal adiabatic circuit would operate without the loss or gain of electronic charge.

The power supplies of adiabatic logic circuits have also used circuit elements capable of storing energy. This is often done using inductors, which store the energy by converting it to magnetic flux. There are a number of synonyms that have been used by other authors to refer to adiabatic logic type systems, these include: "Charge recovery logic", "Charge recycling logic", "Clock-powered logic", "Energy recovery logic" and "Energy recycling logic" [1]. Because of the reversibility requirements for a system to be fully adiabatic, most of these synonyms actually refer to and can be used interchangeably, to describe quasi-adiabatic systems. These terms are succinct and self-explanatory, so the only term that warrants further explanation is "Clock- Powered Logic"[1]. This has been used because many adiabatic circuits use a combined power supply and clock, or a "power- clock". This variable, usually a multi-phase, power-supply which controls the operation of the logic by supplying energy to it, and subsequently recovering energy from it.

The never-ending need for low-power and low-noise digital circuits has intrigued designers to explore new options in the world of circuit design. One approach that seems to be very promising is the famous energy-recovering (adiabatic) logic. Adiabatic circuits pursue low energy dissipation by restricting the current to flow across devices with low voltage drops and by recycling the energy stored in the capacitors[3]. In order to reduce dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching, has been proposed in the last few years[2]. In such an approach, the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and recovery of the energy stored on the capacitors is achieved. In this paper, we have proposed a new adiabatic technique. We have analyzed the various low-power techniques like CPL, EEPL, PFAL, and Proposed logic i.e. adiabatic diode discharge Logic (ADDL)[3]. Power and delay are the important factors calculated in this paper with the variation of power supply and frequency. The work is concentrated on the design of low power multiplexer as Multiplexer is a basic block used extensively in communication systems, combinational circuits, data paths, and FPGAs to implement logic functions[3]. There are numerous designs of the multiplexer which are based on pass transistors or transmission gates. The use of pass transistors provides the optimum solution for multiplexer design with a minimum number of devices. The inherent disadvantage involved in this technique is low output swing. Different techniques have been proposed in designs like EEPL to restore the logic level at the output

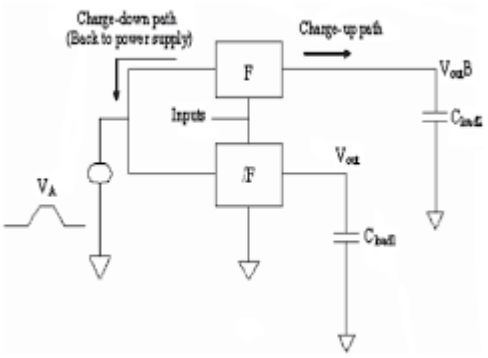


Fig. 6. Adiabatic Logic Gate showing charging and discharging path [7]

Adiabatic operation of the circuit is an ideal condition that may only be approached asymptotically as the switching process is decelerated. In most practical cases,the energy dissipation associated with a charge transfer eventis conventionally composed of an adiabatic component and anon-adiabatic component. Therefore, reducing all the energyloss to zero may not be possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requisites, this approach can sometimes be acclimated to reduce the power dissipation of digital systems.

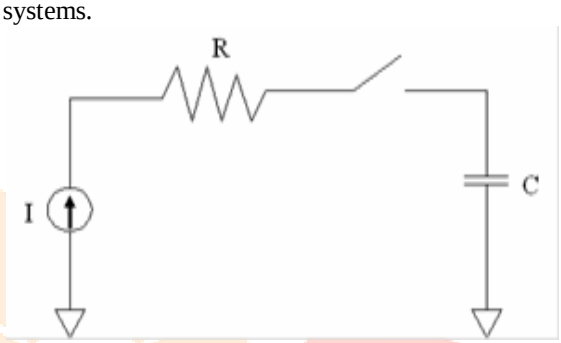
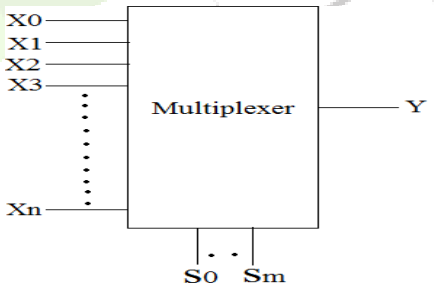


Fig: Discharge Process of Adiabatic Logic Circuit

II. MULTIPLEXER

A Multiplexer is a device that allows one of several analog or digital input signals which are to be selected and transmits the input that is selected into a single medium. Multiplexer is alsoknown as Data Selector. A multiplexer of 2n inputs has n- select lines that will be used to select the input line to send to theoutput. Multiplexer is abbreviated as Mux. MUX sends digital or analog signals at higher speeds on a single line in oneshared device. It recovers the separate signals at the receivingend. The Multiplexer boosts or amplifies the information thatis later transferred over the network within a particular bandwidth and time.



CPL

The complementary Pass-Transistor Logic (CPL) gate consists of two NMOS logic networks (one for each signal rail), two small pull-up PMOS transistors (as shown in fig2.1) for swing restoration, and two output inverters for the complementary output signals. The figure depicts a two-input multiplexer which represents the basic and minimal CPL gate structure (ten transistors). When the input S is logic 1, then input A is selected as output. If the input S is logic 0, then input B is selected as output. The output will be available in both inverted and non-inverted forms.

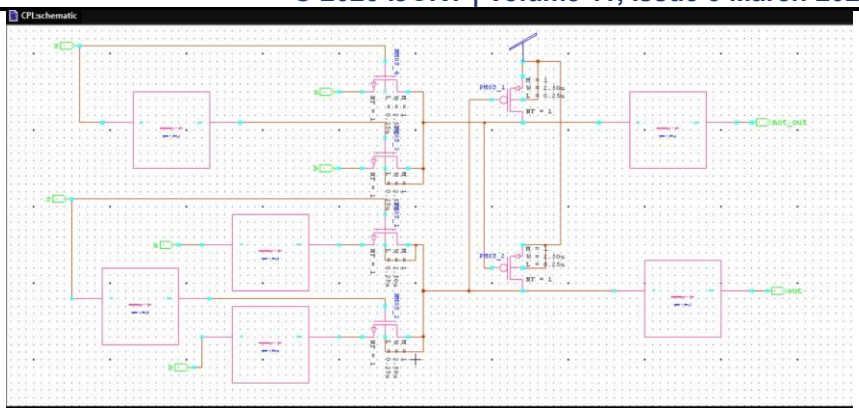


Fig:2 to 1 Multiplexer in CPL

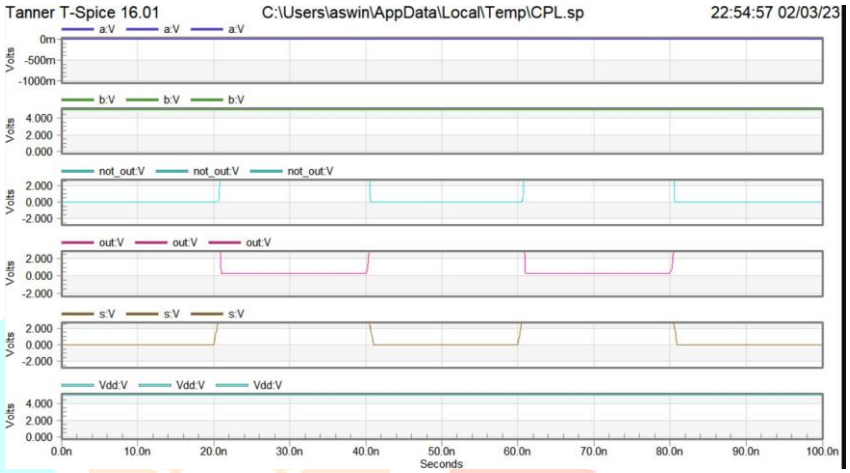


Fig: Waveform of CPL

EEPL

In the energy-economized pass-transistor logic (EEPL), we use 4 NMOS transistors and 2 PMOS transistors as shown in fig 2.2. Inverters are used for obtaining complementary output signals. In this logic, the sources of the PMOS pullup transistors of a CPL gate are connected to the complementary output signal instead of Vdd. The main advantage of this design is smaller delay and smaller power dissipation compared to CPL. Because of regenerative positive feedback, this logic provides a shorter delay than CPL logic. If the input S is logic 1, then input A is selected as output. If the input S is logic 0, then input B is selected as output. This circuit produces output in both inverted and non-inverted forms..

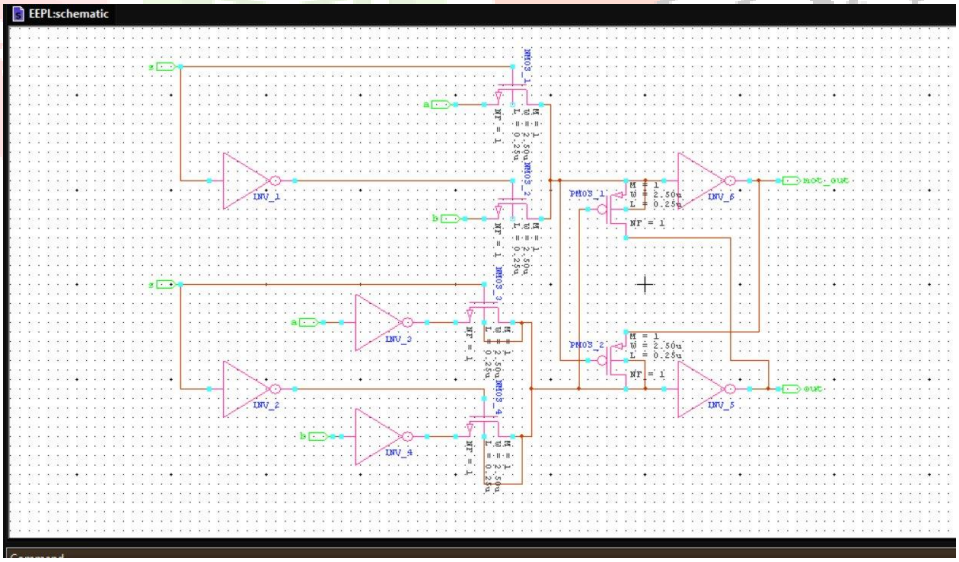


Fig: 2 to 1 multiplexer in EEPL

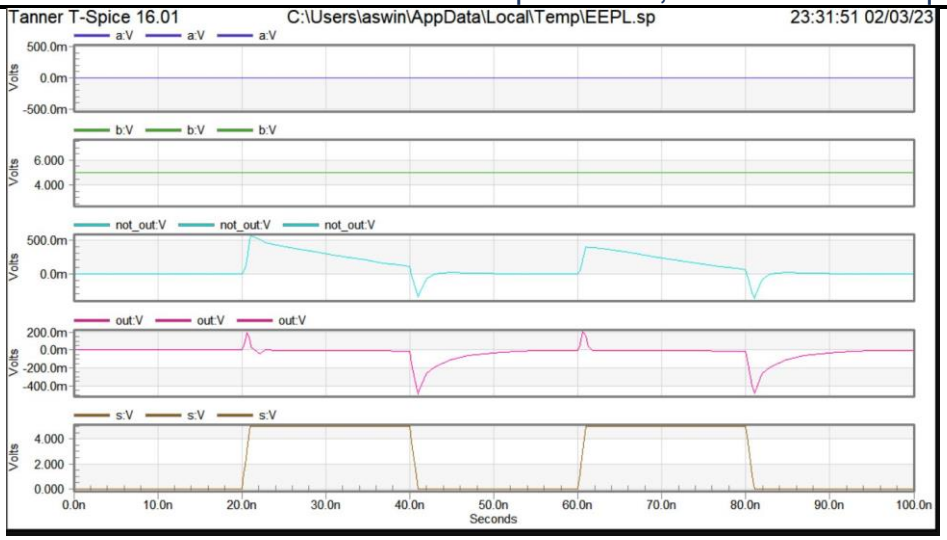


Fig: Waveform of EEPL

PFAL

PFAL uses a power clock instead of a normal one as it is also used to energize the logic networks. That is no extra dc power source is used and a time-varying ac signal is used to actuate the circuit elements along with the clocking control. In PFAL a 4-phase clock is used namely ideal, evaluate, hold, and recover stages. The ideal stage is inherently used for the pipeline of the different stages. During the evaluation phase, logic 13 is evaluated as per the input vectors which is kept retained during the hold stage. The charge is recovered back during the recovery stage. But PFAL does not provide full recovery of charge and hence it is considered as partial recovery adiabatic logic family

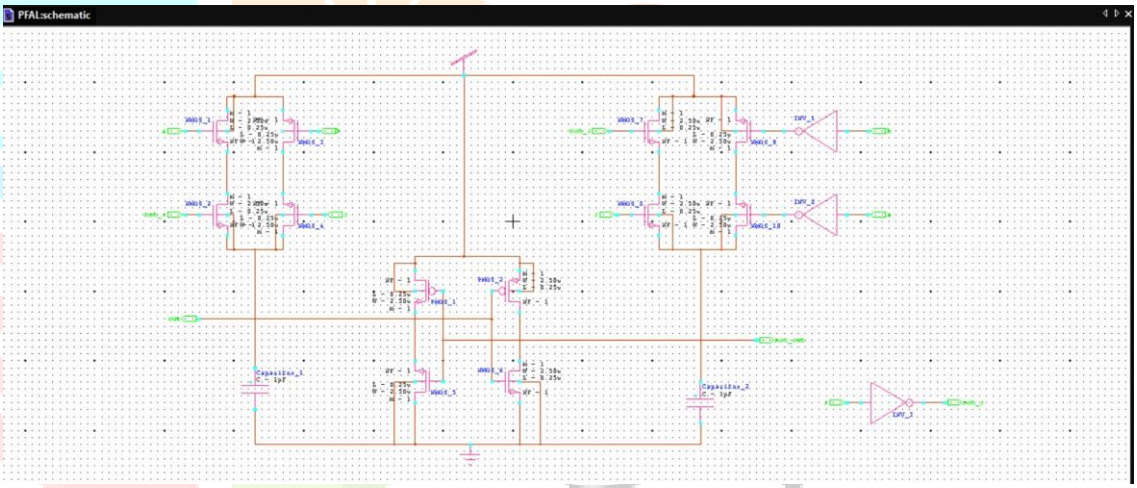


Fig : 2 to 1 Multiplexer in PFAL

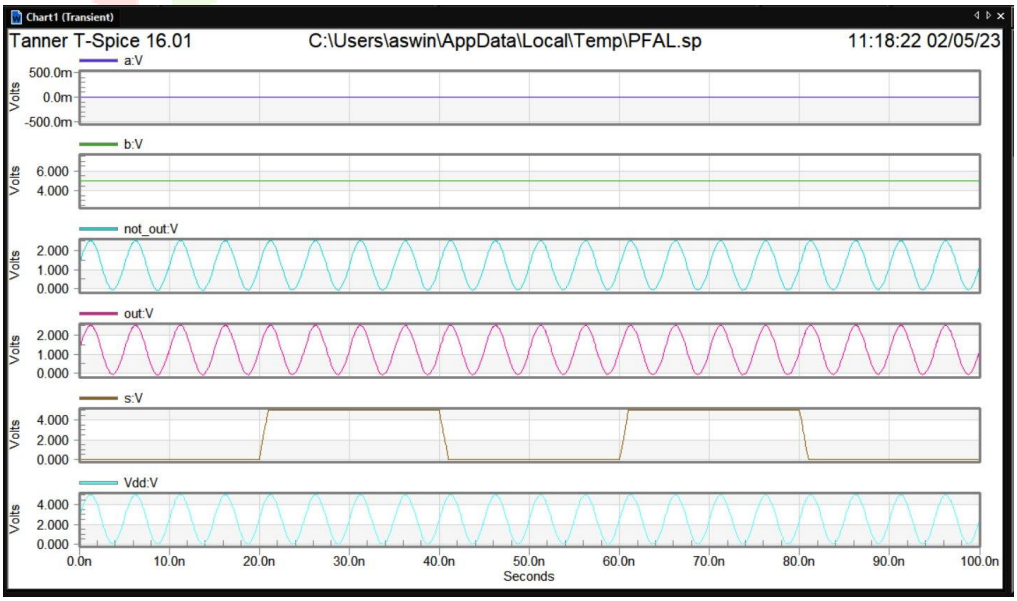


Fig: Wave form of PFAL

ADDL

This is the proposed logic. In this proposed 2:1 multiplexer logic the 2 PMOS & 10 NMOS transistors are used. This is the adiabatic diode discharge logic (ADDL) which consumes very less power as compared to PFAL Logic. In this circuit, the PMOS used here for the purpose of providing a path for the capacitor to charge. In this logic style, we use 2 NMOS transistors to provide a discharge path for the capacitor to discharge. Given below is the schematic for the proposed multiplexer logic. The new design is using diode-connected transistors to achieve fully adiabatic operation without any residual charge at the output nodes. The PMOS devices provide the 15 charging path once the voltage at its gate (which is connected to out/outb) crosses the threshold. During charging of outputs, the diode-connected NMOS devices remain off as the Vgs (Gate to source voltage) is below Vt. Once the output charges completely, the discharge cycle begins. During this cycle, the diode connected to NMOS turns on and provide a low resistance (in comparison to logic branches) discharge path to pck. The low resistance path reduces power consumption in two ways in comparison to other designs. First is the design becomes fully adiabatic as there is no discharge path to ground in comparison to PFAL. Second is Low resistance path reduces the power output depends upon input 'a'; if input 'a' is logic 1, then output follows pck and if input 'a' is logic 0, then output is '0'. If the input S is logic '1', then output depends upon the input 'b'; if input 'a' is logic 1, then output follows pck and if input 'a' is logic 0, then output is '0'.

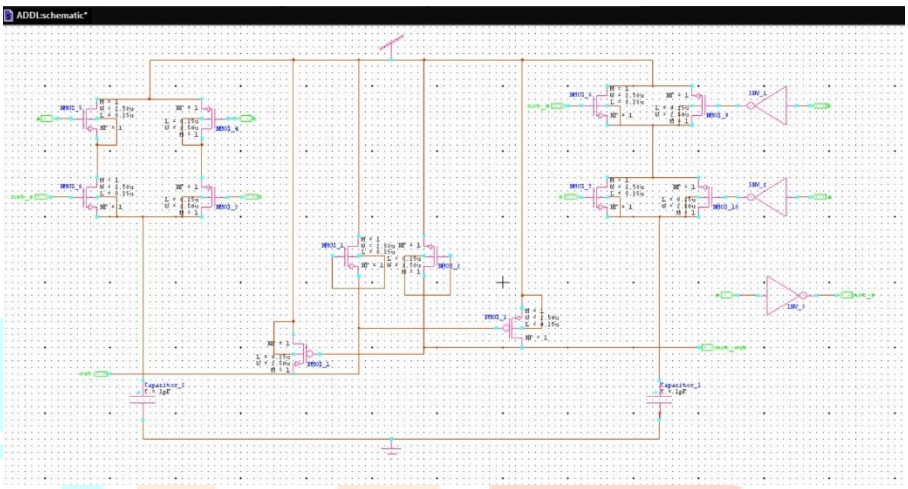


Fig: 2 to 1 multiplexer in ADDL

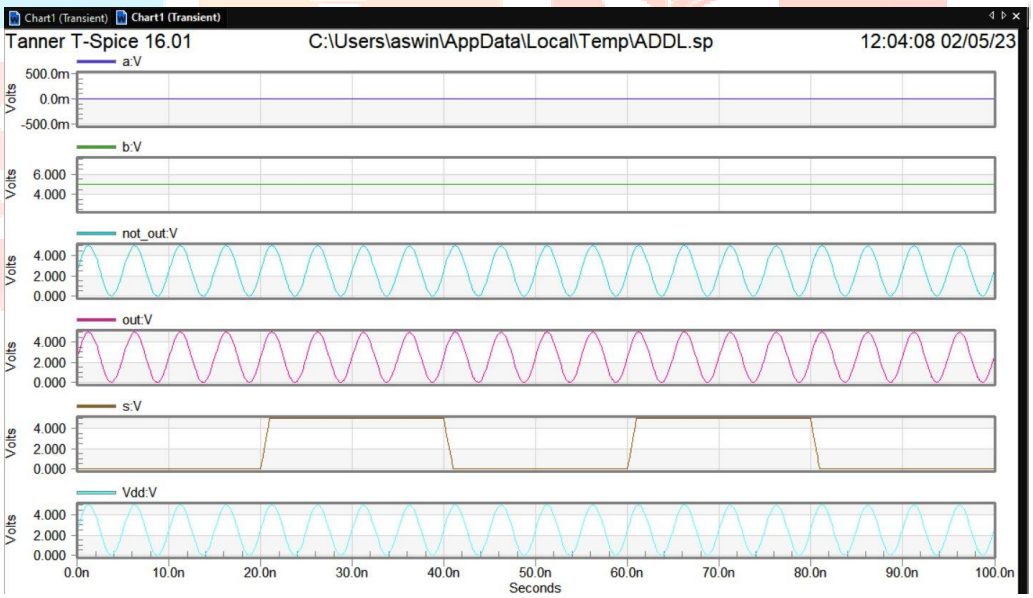


Fig : Waveform of ADDL

Results:

Vdd	Power (mW)			
	CPL	EEPL	PFAL	ADDL
5V	1.6 e-002 watts	7.2 e-006 watts	3.533358e-003 watts	1.07e-003 watts
3V	4.9 e-003 watts	1.638 e-003 watts	0.9159e-009watts	0.74877 e-002 watts
2V	1.6 e-003 watts	0.5824 e-001 watts	0.3055 e-009 watts	0.2491e-001 watts

Comparison of CPL, EEPL, EEPL, and Proposed logic in terms of Power (mW) and VDD

Comparison of PFAL Logic and proposed logic:

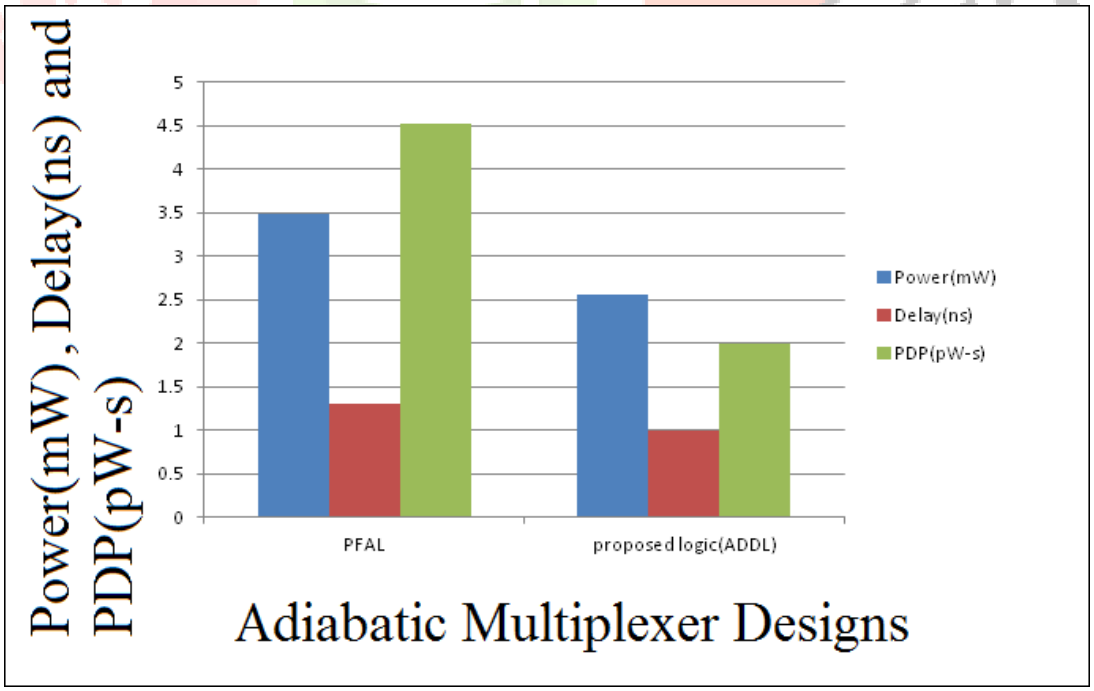


Fig: : Comparison of PFAL and ADDL in terms of power, delay and PDP at Vdd= 5V

Graphical Representation :

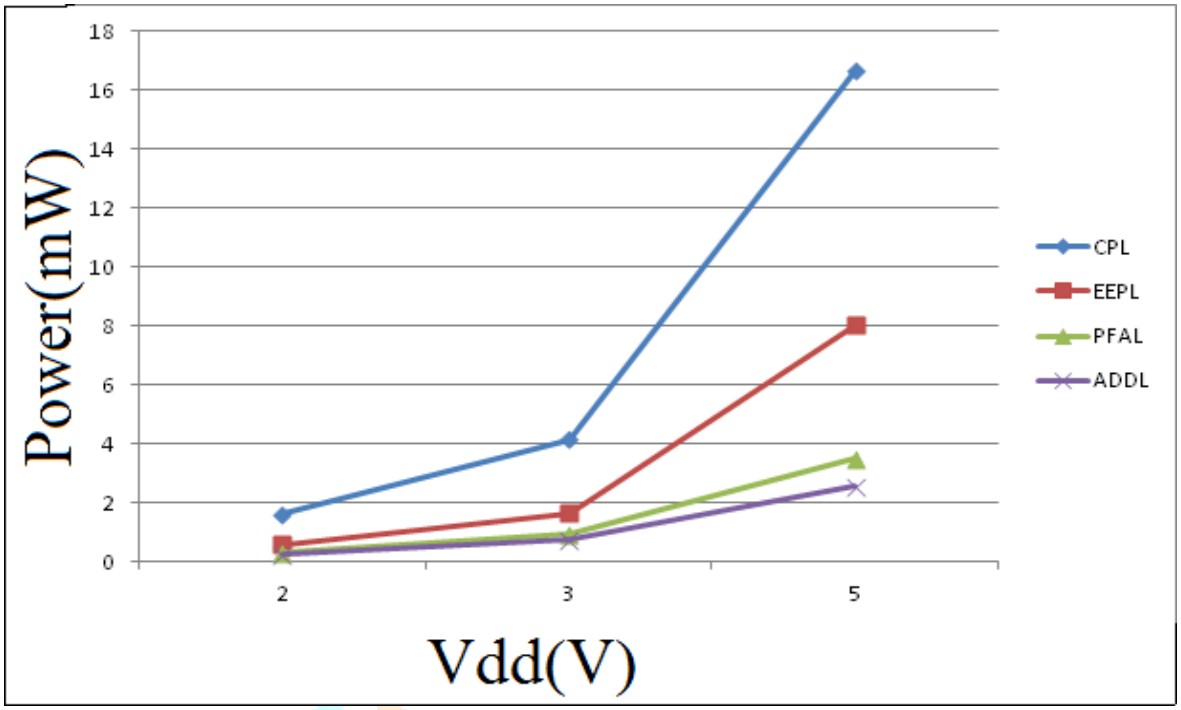


Fig :: Variations of CPL, EEPL, PFAL, ADDL in terms of power (mW) and Vdd

Conclusion

We have designed and analyzed a new technique for the power reduction in the 2:1 multiplexer and by taking that into consideration a new nibble multiplexer has been designed the results show that the Proposed Multiplexer shows good performance with supply voltage variations as compared to EEPL, CPL, and PFAL multiplexer. When we compare the two adiabatic logics i.e., PFAL and Proposed Logic (ADDL), the Proposed Logic saves power up to 26.2% at a 5V power supply. Finally, we declare from the results that the proposed logic (ADDL) is better logic than CPL, EEPL, and PFAL.

III. Future Scope

The adiabatic technique is the latest in reducing power dissipation in digital circuits. There can be an improvement in the techniques of adiabatic logic. We have proposed one such Design Adiabatic diode discharge logic (ADDL). Realizing 4:1, 8:1, and 16:1 multiplexers using 2:1 multiplexer with the help of adiabatic logic families. Adiabatic circuits need a nonconventional power supply which causes overhead in terms of the area hence the overall cost is increased. So design a new adiabatic logic family which can be operated using a conventional power supply. The future scope for the proposed design would be of great importance for the VLSI technology as the VLSI engineers are steadily working for power reduction and higher performance.

References

[1] Preethi bhakti, Navaid Z Rizvi, "An Alternative Approach to Low power application Cricut'', 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT) 03-05 March 2016

[2] Richa Singh and Rajesh Mehra, "Power Efficient Design of Multiplexer Using Adiabatic Logic", International Journal of Advances in Engineering & Technology, IJAET ISSN: 2231-1963Vol. 6, Issue 1, pp. 246-254Mar. 2013.

[3] M.Padmaja, V.N.V. Satya Prakash, "Design of a Multiplexer In Multiple Logic Styles for Low Power VLSI", International Journal of Computer Trends and Technology- volume3Issue3- 2012.

[4] N.L.S.P.Sai Ram and K.Rajasekhar, "Power Optimized Energy Efficient Hybrid Circuits Design by Using A Novel Adiabatic Techniques", International Journal of Engineering Research & Technology (IJERT) Vol. 1 Issue 7, ISSN: 2278-0181 September – 2012.

[5] Anu Priya and Amritha Roy, "Adiabatic Technique for Energy Efficient Logic Circuits Design", The International Journal of Electronics and Communication Engineering Technology (IJECT) Vol. 5, Issue Spl-1, Jan - March 2014.

[6] Tanuja Jaggi and Ravinder Kumar, "Performance Analysis of Positive Feedback Adiabatic Logic for Low Power", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 2, Issue 9, September 2013.

[7] Gaurav Singh, Ravi Kumar, Manoj Kumar Sharma, "Comparative Analysis of Conventional CMOS and Energy Efficient Adiabatic Logic Circuits", International Journal of Emerging Technology and Advanced Engineering ,ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3, Issue 9,September 2013.