IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Quantum-Dot Cellular Automata-Based Error Detecting Circuits

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Abstract: Quantum-dot cellular automata(QCA) has become a reliable feature to nanotechnology as a viable replacement for CMOS technology. It is based on cell-to-cell coulombic contact. Unlike conventional system which propagates data as charge flow, QCA coveys it as **charge configuration**. A novel design of an even parity generator is presented in this paper which is composed of only 21 cells and occupies a 0.03μm^2 area. It possesses fewer cells lower latency and reduced complexity than the most well-known designs. The proposed parity generator could be employed in a wide range of digital data transmission error detection circuits. The design and simulation are done in QCADesigner2.0.3.

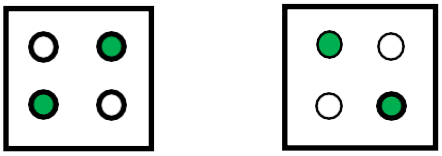
KEYWORDS - Quantum Dots, QCADesigner, Quantum Dot Cellular Automata (QCA), Qubits, Nanotechnology, Nanoelectronics Devices

I. Introduction

Quantum bits (also described as Qubits) are used to store information in quantum computing and can have several states, store enormous amounts of data, use less energy, and work at a faster rate. The encoding is achieved by the charge configuration of a QCA cell [11-15]. Power dissipation is extremely little since current is not flowing out of the cell. The ability to recognize a message that contains an error is crucial for digital communication [4].

2.1 QCA CELL UNIT:

The core building element of QCA technology is the QCA cell, which has four quantum dots and two moveable electrons. Within each cell, four quantum dots are arranged in form of a square fashion, and two extra electrons deflect each other. As a result, we have two stable states as indicated in Fig1 below.

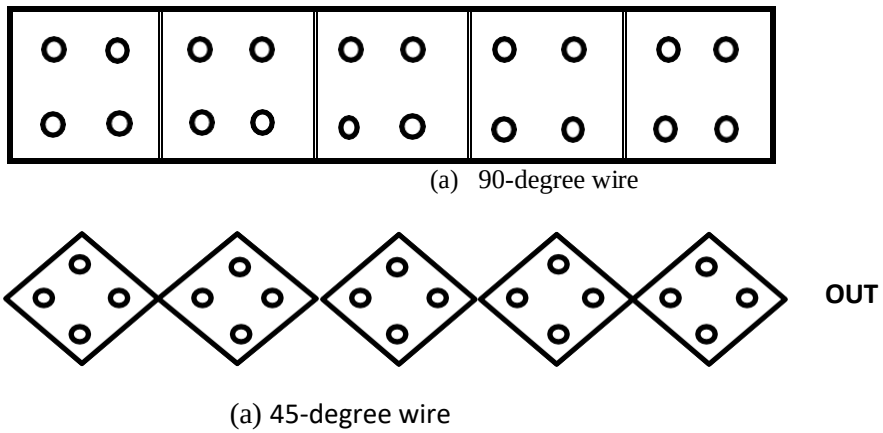


(a) **P =" + 1"** **(b) P =-1**"

Fig1: QCA cell with polarization states for fig1(a): P = "+1", fig1(b) P = " -1"

2.2QCA WIRE:

Data is sent from input to output using QCA wire, which is made up of QCA cell units. Polarization circulates from one cell to the succeeding due to coulombic encounters amongst electrons. The QCA wire has two configurations to achieve wire crossing in the same circuit layer: normal (90° wire) and rotated (45° wire). To span single-layer wires, clocking control is used.



(a) 90-degree wire

(a) 45-degree wire

Fig2: QCA wires: 2(a) 90-deegree wire; 2(b) 45-degree wire

2.3QCA GATES:

In QCA, inverter and majority voter are two primary logic gates. A majority voter, which is usually 3 or 5 input cells, usually stimulates the transition. In a normal majority gate, a single cell's polarization drives a 3-input cell. In a cell, the majority rules. By altering the polarization of **p =" +1", and p ="-1"** in one cell, the majority gate is utilized to produce AND and OR gates in QCA. The equation is described as:

$$O(P, Q, R) = PQ+QR+RS \quad ..(2)$$

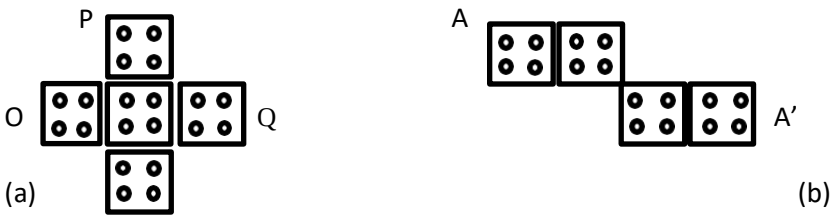


Fig3:(a) QCA Majority Gate(b) QCA inverter

2.4 QCA CROSSOVERS:

In QCA circuit design, there are two types of crossovers, coplanar and multilayer. Due to the limited connection between normal and rotated cells when they are placed close to each other, two distinct signals in a coplanar outline can be conveyed individually. While this arrangement has a few issues, such as crosstalk, other strategies must be used to address these issues. The multilayer technique allows the signal to pass via the higher level, which extends benefits including tolerance to cell movement deficits and decreased extent of occupation, as seen in Figure 4. (b). According to Coulomb's repulsion, three layers are needed to implement the multilayer crossing.

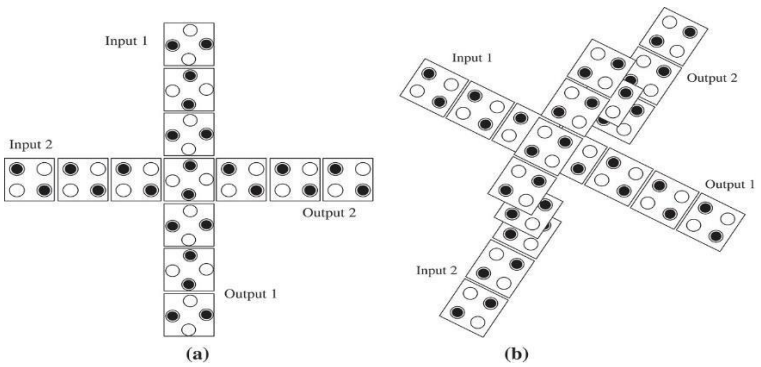


Fig4: (a) Coplanar Crossover (b)Multilayer crossover [21]

3. MATERIALS AND METHODS:

3.1 XOR GATE:

In the logic circuit, a 2-input XOR gate is prominent. Many types of XOR gates were introduced by QCA researchers. As demonstrated in fig4, the best design for the XOR arrangement was proposed by "Haotian Chen et al." as referenced in [3]. In this study, 2-input XOR is plied to implement a 3-bit even parity generator.

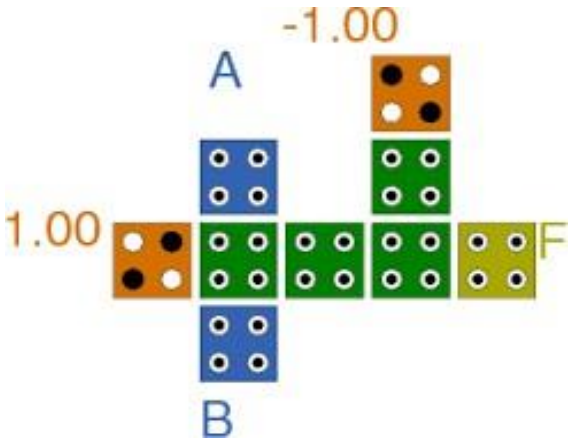


Fig5 Optimum XOR gate as depicted in [3]

3.1: PARITY GENERATOR:

A **parity generator**, which is a combinatorial logic circuit produces the transmitter's parity bit. For a system that carries crucial and sensitive data, they are critical to signal integrity.

Let's presume we are sending a three-bit message with an even parity bit. With the parity bit O as the output, three inputs J, K, and L are being applied to the circuit. The **total number of bits** must be **even** in order to generate even parity bit. With 1 acting as a parity bit to make all 1s in the truth table even when the number of 1s is odd, the truth table of an even parity generator is shown below in Table1,

TABLE1: Truth Table for 3-bit Even Parity Generator

Three-bit input message			Generated even-parity bit
J	K	L	O
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Boolean The function is given as

O (J, K, L) = (J XOR K) XOR L..... (1)

4. PROPOSED THREE-BIT EVEN PARITY GENERATOR:

The suggested QCA even parity generator structure is presented in Fig5. It follows the Boolean function. The parity bit is produced by XORing the bits together. This is made up of two 3-input majority gates. The presented block has 3-inputs J, K, and L respectively, and output(E) of that gives generated parity bit. The inputs (J) and (K) are exored together and then fed to the input of the next exor which generates the output parity bit(E) as shown in Fig6. Data can be damaged when binary information is sent through the communication system because of noise which can change binary digits from 1s to 0s or vice versa. At the ending of binary data, this extra bit (parity bit) is inserted.

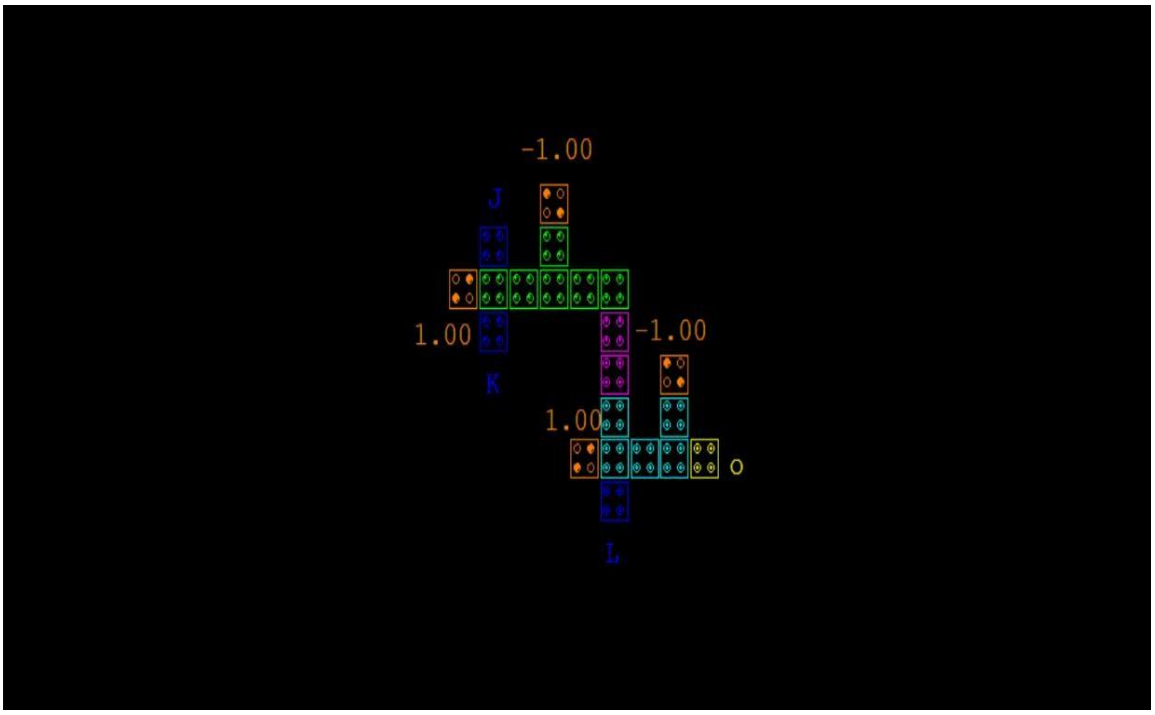


Fig6: Proposed design of 3-bit even parity generator.

The proposed design comprises 21 cells, 0.75 latency, and occupies a 0.028μm^2 area and hence lower complexity than best-reported designs.

TABLE2: Comparative analysis of different 3-bit even parity generators

Design	Cell Count	Area	Latency
J Das et. Al [4]	52	0.061μm^2	0.75
Dharmendra Kumar et. Al	49	0.039μm^2	0.75
Proposed design	21	0.032μm^2	0.75

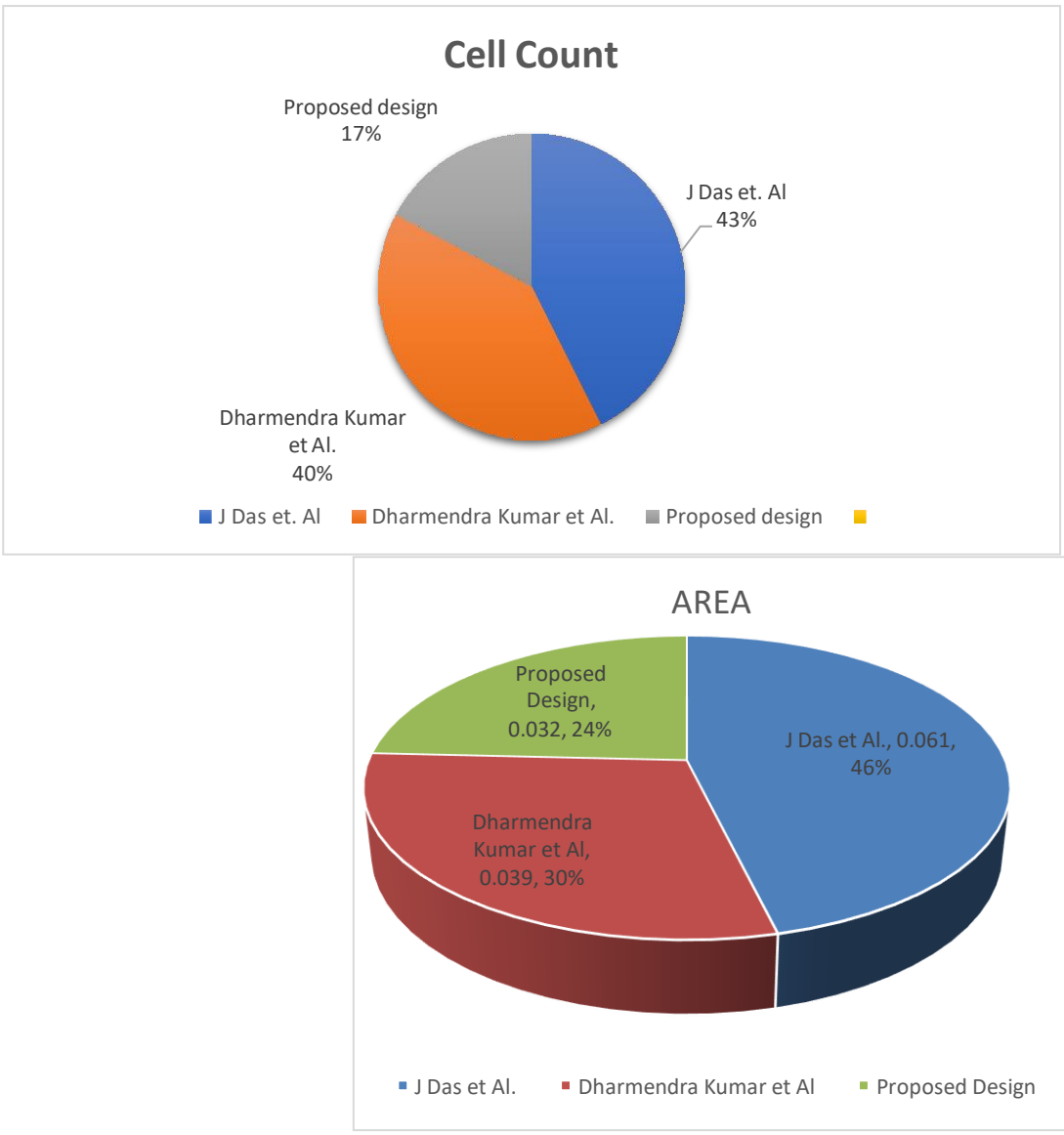


Fig7: Pie chart depicting area and cell count of our proposed design and best-reported designs.

The above pie chart clearly depicts that the area occupied and cell count in our proposed design is lesser than best-known designs.

5. SIMULATION RESULTS:

The design and simulation are done in QCA Designer2.0.3 and are a bistable approximation. The other parameters are taken as default QCA parameters. The simulation results are shown in fig7 below. The output waveform is obtained precisely with a delay 0f 0.75 clock cycle.

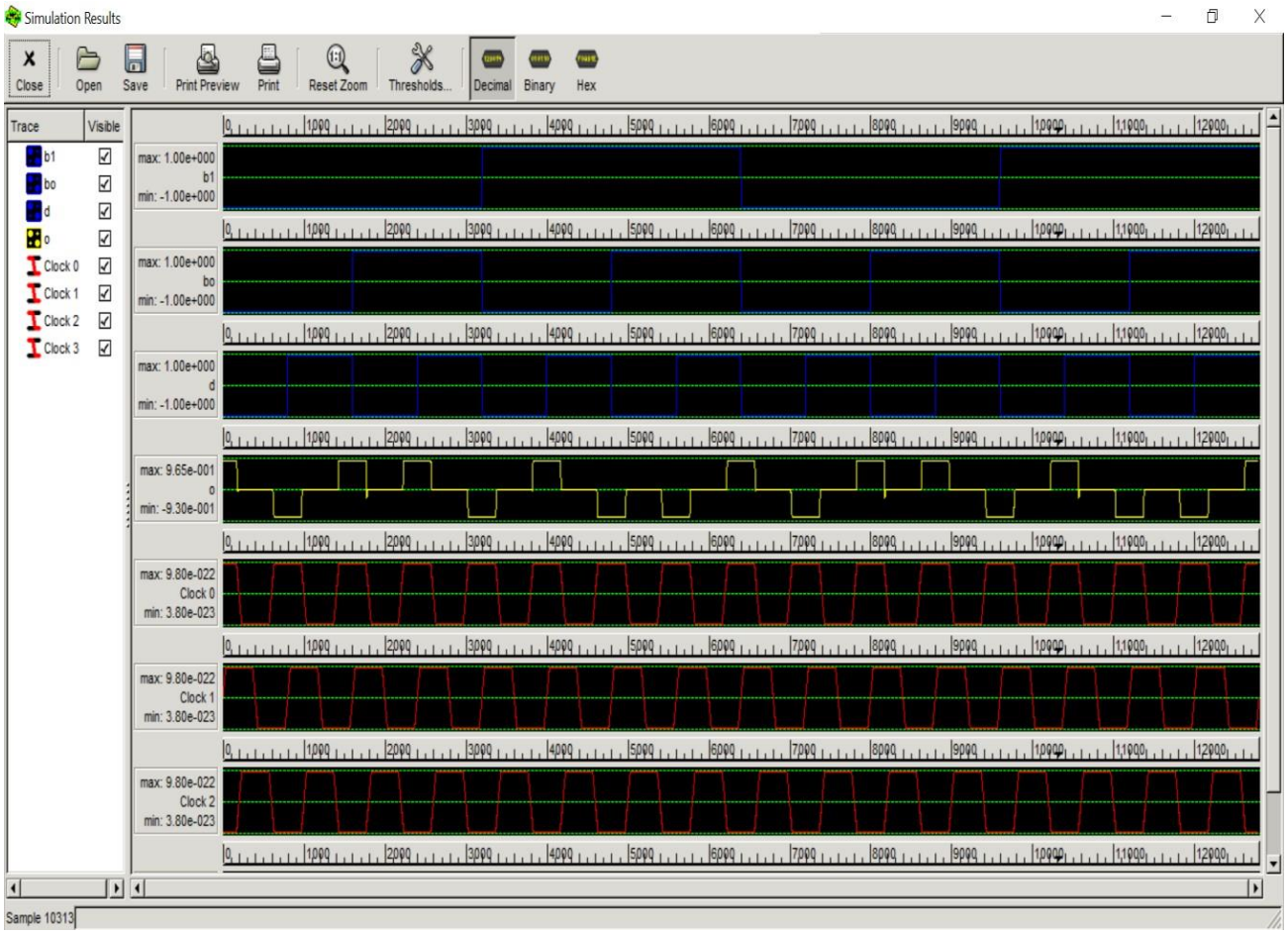


Fig8: Simulation results of three-bit even parity generator

6. CONCLUSION:

A unique block with modest cell numbers and area was proposed in this study. The layout is designed by QCA Designer2.0.3. Through comparison and pie chart, the simulation findings were plainly seen demonstrating that the performance of the suggested layout is superior to that of its contemporaries. As the output is present on the outer portion of the proposed design, this design could be more optimized and extended to newer circuits in the future.

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