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DESIGN OF TG BASED HIGH STABLE 9T SRAM CELL

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Abstract-- **This article describes the made-up design of a 9T Static Random Access Memory single bit cell with enhanced performance. For this proposed 9T SRAM cell, the supply voltage is varied and simulations are done using Monte-Carlo, and the results are compared with conventional (Conv) 6T, conventional 7T, and conventional 8T SRAM cells in the 22nm technology. The proposed 9T shows 1.122x, 1.256x times lesser read delay when compared to 6T and 7T respectively. Whereas it shows 1.058x times lesser delay than 7T during write operation.**

Keywords—Read Delay; Write Delay; Read SNM; Read Power; Write Power; Hold Power.

1.INTRODUCTION

Memory is the essential part in the growth of technology. Without its presence it's impossible to imagine the development in technology. Based on the requirement there are different designs of memory. One among them is an SRAM memory. The SRAM memory circuits are designed using transistors. The transistors are used for switching and amplifying the signals in a circuit. The applications of SRAM ranges from ICs to embedded systems.

The recent advancement in mobile, and other battery-operated devices as well as increase in data transfer rates demands that these systems use less power and reduce operational working delay. Thus, this fast-growing technology demands low power consumption and increased speed circuits. Based on these technological demands these SRAM circuits have

different designs. SRAM is designed using different number of transistors. They may consist of 6,7,8 transistors and any number based on requirement. The idea behind using different number of transistors is to improve the performance of the circuit. There are various parameters like read delay, write delay, read power, write power, Read SNM, Write SNM, hold power that should be analyzed for assessing the performance of a circuit. A block of SRAM consists of row decoders, input buffers, bit-line conditioning circuitry and output sensing logic. These single bit cells are arranged in rows and columns and each row can be accessed using row decoder and column can be accessed using column decoder. Thus, different sized memory can be designed like 64x32 etc. (i.e., A 2 KB memory).

There are different techniques for designing a 6T SRAM circuit. Each technique improves certain parameters like reducing power consumption or increasing speed of writing or reading but each of them uses same number of transistors.[1]-[5]

Fig-1 shows the conventional 6T SRAM circuit. It has two storage nodes L and H where a single bit is stored either 0 or 1. Worldline (WL) is used to switch on the access transistors. This enables the circuit to read or write. The bit lines are precharged using capacitors and discharge if a path is created to ground. Thus, bit line voltage changes and sense amplifiers are used to sense the change in bit line voltages

While designing 6T SRAM circuit there are some limitations in RSNM and WSNM. This can be improved by a conventional 7T SRAM cell where it has improved read and write static noise margins

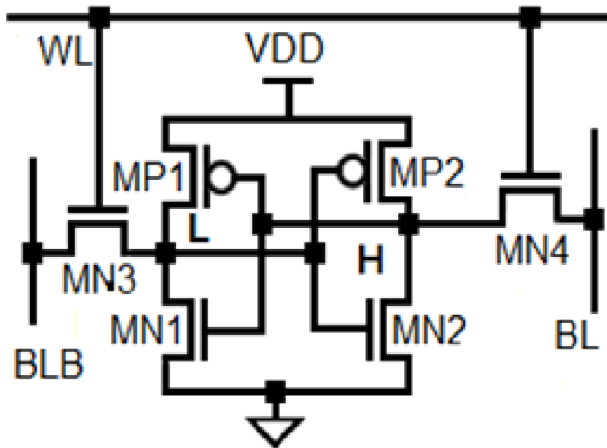

Fig-1. Conv 6T Static-RAM Single Bit-Cell.

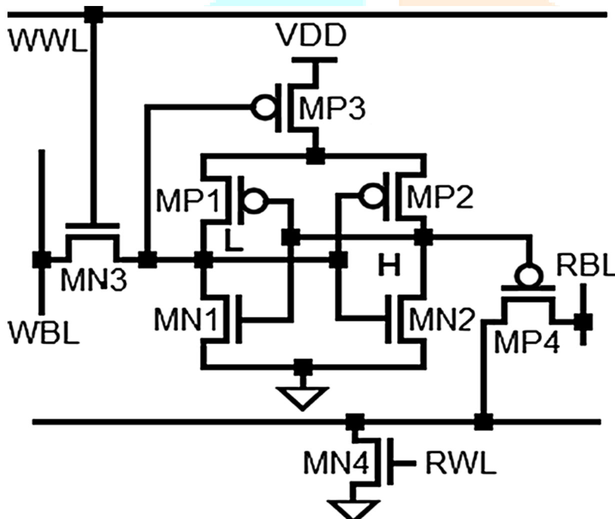

Fig-2. Conv 7T Static-RAM Single Bit- Cell.

Fig 2 depicts conventional 7T SRAM circuit. In this circuit read and write operations occurs separately. During read operation WWL is OFF and while writing RWL is OFF. Here, transistor MP3 acts as supply feedback in order to bring down the pull up path while the writing operation is taking place [2].

We use transistor named as MP4 like read access transistor because PMOS transistors have a high level of susceptibility to fundamental error. Furthermore, due of the pace of reading and writing saturation, PMOS transistor has less effect. It also includes a read access transistor (MN4), where it serves as the same for the entire or entire row. The remaining MOS transistors are used to build the basic 6T SRAM single Bit-Cell [3]-[7]. This compensates for the substantial decrease in R-SNM (Read-Static-Noise-Margin) caused by voltage division among access Field Effect Transistors and Pull-Down Network.

Despite the fact that maximal stability is attained when the read operation is taking place, the read current path is separated from the storage node.

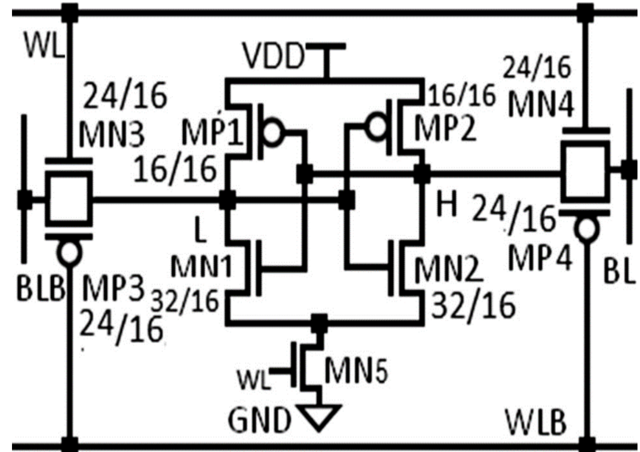

Fig-3. Conv 8T S-RAM Single Bit-Cell

However, increasing a greater number of transistors increase the volume of the SRAM circuit. To counter these design constraints, a more effective S-RAM including one extra transistor, referred as 8T S-RAM cell is proposed. In comparison to the conventional 6T SRAM method, the conventional 8T SRAM shown in figure-3 is designed with two transmission gates, implying the use of two NMOS access pass gate transistors [4],[9].

Pre-charging BL and BLB, then making WL line high and WLB line low, completes the read operation in the SRAM cell. When both BL line and BLB line have been pre-charged, one of the bit-lines discharges, and the data is kept at nodes L and H. This proposed 8T takes very less time to read the data when compared to 6T and 7T.But the leakage power for this circuit is high which is a limitation of this circuit.

2.PROPOSED DESIGN

Based on the study of working of various existing SRAM circuits, A new circuit is designed that has better stability (tolerance to noise) when compared to some of the existing circuits. The proposed circuit consists of 9 Transistors. In this proposed design while reading the write circuitry part is OFF and during writing the read circuitry

part is OFF. This technique makes the circuit to use less power during reading and writing processes.[5],[11]

The proposed circuit is designed and simulated in HSPICE simulator to obtain various parameters like read delay, write delay, read SNM, write SNM, Hold power etc. The circuit is simulated with the help of 22nm technology library's the lengths of all the MOSFETS are taken to be 22nm and width is varied based on the functionality of the MOSFET. The width of the access transistors is taken as 33nm and 44nm for the NMOS in the main circuitry. The width of PMOS in the main circuitry is taken as 22nm.

The designed circuit has following labels RWL, WWL, BL, BLB, RBL, MP(X), MN(X) (where symbol X denotes an index number). RWL is the read word line that enables the read circuitry part when it is enabled high. Similarly, WWL is the write word line that enables write operation when it is set high. Bit Line (BL), Read Bit Line (RBL) and Bit Line Bar (BLB) are pre-charged using capacitors. Thus, reading data from the cell is done with the help of the change in voltages of these bit lines. Sense Amplifiers are used to sense the change in bit line voltages. In fig-4 MN3 and MN4 are write access transistor, MN6 is a read access transistor.

Figure-4 depicts the suggested construction of a 9T Static RAM Bit-Cell with a Bit-Line (BL) connected to the source terminal of an MN3 transistor. Also includes a Write-Word-Line (WWL) and a Read Word-Line (RWL) (RWL). The MN5 and MN6 are Read Access Transistors.

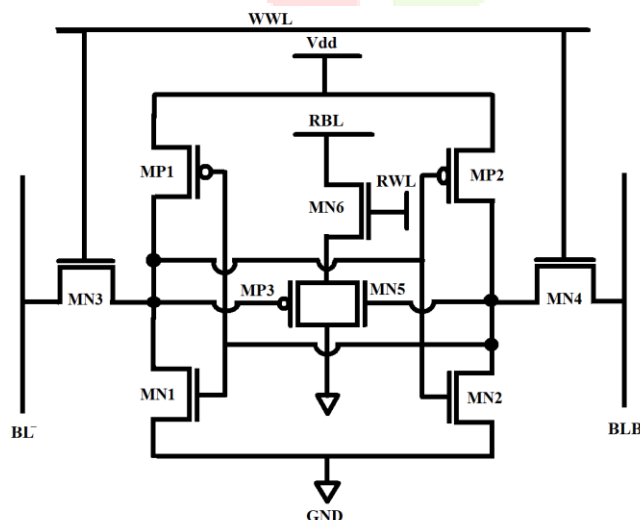

Fig.4. Proposed Read-Decoupled 9T Static RAM Single Bit-Cell.

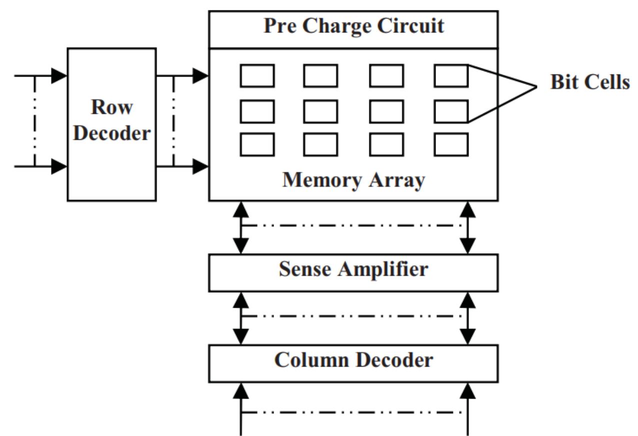

Fig. 5. Architecture of proposed 9T Static RAM.

Because a 22nm technology library is used for simulation, the channel lengths of all transistors are chosen to be 22 nm, and the widths of the P type MOSFETs are chosen as shown below:
MP1 and MP2 have widths of 22 nm, 44 nm for MN1 and MN2, and 33 nm for MN3 and MN4. the MP3 transistor has 33nm and MN5, MN6 has 33nm and 44nm respectively. Figure 5 depicts the architectural design of the proposed Static RAM.

3.SIMULATION RESULTS & DISCUSSIONS

A). Simulation Setup:

All simulations are run on a 22-nm PTM with a variable supply voltage to achieve varied results. According to ITRS 2011, a 10% variation in VDD is projected in progressively scaled technology nodes [2]. As a result, the design metrics have been approximated for a supply voltage range of 0.68 V to 0.40 V in 0.4V steps.

B). Read Delay Time Analysis:

Read operation starts when RWL set to high, When RWL is high then the NMOS access transistor which is connected to RBL becomes ON. MOSFETS MP3 and MN5 are connected to nodes L and H respectively. Assume node L stores '0' and node H stores '1', then both MP3 and MN5 are Switched ON. Now a path is created from RBL to ground and RBL slowly discharges. In contrast if node L stores '1' and node H stores '0' then both MP3 and MN5 becomes OFF and no current flows from RBL to ground. Thus here RBL does not discharge. Sense amplifiers sense the change in bitline voltage and read the data. the time necessary to discharge by 50mv is known as the read delay time. During the read process WWL is OFF.

TABLE I

READ ACCESS TIME (T_{READ})

V_{DD} (V)	Conv-6T(ns)	Conv-7T(ns)	Conv-8T(ns)	Prop9T (ns)
0.68	0.404	0.492	0.121	0.362
0.64	0.466	0.539	0.132	0.407
0.60	0.542	0.607	0.146	0.483
0.56	0.622	0.690	0.162	0.623
0.52	0.704	0.810	0.182	0.706
0.48	0.799	0.970	0.207	0.806
0.44	0.934	1.230	0.240	0.958
0.40	1.200	1.880	0.288	1.260

Table-1 shows comparative analysis of read access time with various existing circuits. These results are plotted as a graph for better comparison. Fig-6 clearly compares the results.

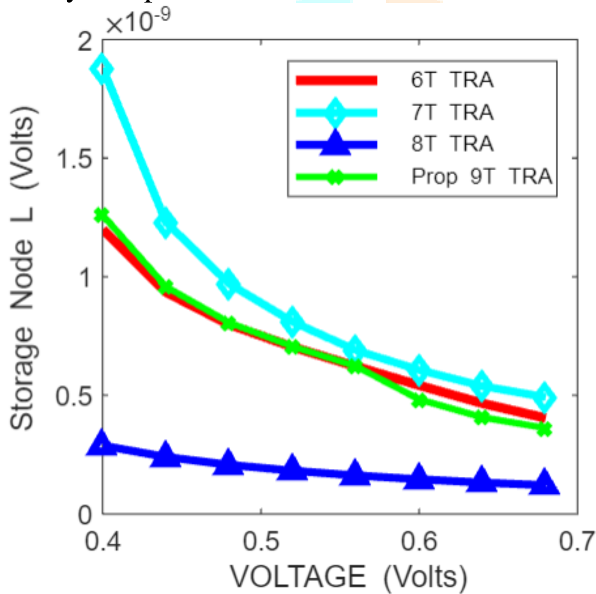

Fig-6. Read access time versus supply voltage.

Fig-6 depicts the graph of read access time of various existing circuits and our proposed circuit.

The read access time of proposed circuit is better than 7T SRAM cell and at high voltages it is slightly better than 6T SRAM.when compared to 8T TRA the values of proposed circuit TRA is poor.

C). Write Delay Time Analysis:

In the proposed circuit when WWL is set high then both the access transistors MN3 and MN4 is switched ON. Assume that BL is charged and BLB is not charged and also assume that node L is storing 0 and node H is storing 1.Now the charged BL discharges through node L and its value raises. parallelly BLB is set to zero and node H slowly decreases its value and changes its value. Thus write operation occurs and RWL is set to 0 during the write operation.

The time it takes to write a logical one that increases its value by 90% of VDD is referred to as write access time. The write delay time to write '0' is defined as the time it takes the 'H' node to reduce its value by 90% of the supply voltage.

Table II

WRITE-ACCESS-TIME (T_{WRITE})

V_{DD} (V)	Conv 6T(ns)	Conv 7T(ns)	Conv 8T(ns)	Prop9T (ns)
0.68	0.751	0.754	0.626	0.750
0.64	0.782	0.807	0.548	0.786
0.60	0.823	0.873	0.445	0.825
0.56	0.877	0.966	0.321	0.878
0.52	0.953	1.100	0.204	0.955
0.48	1.040	1.330	0.179	1.040
0.44	1.180	1.790	0.109	1.180
0.40	1.480	2.790	0.040	1.470

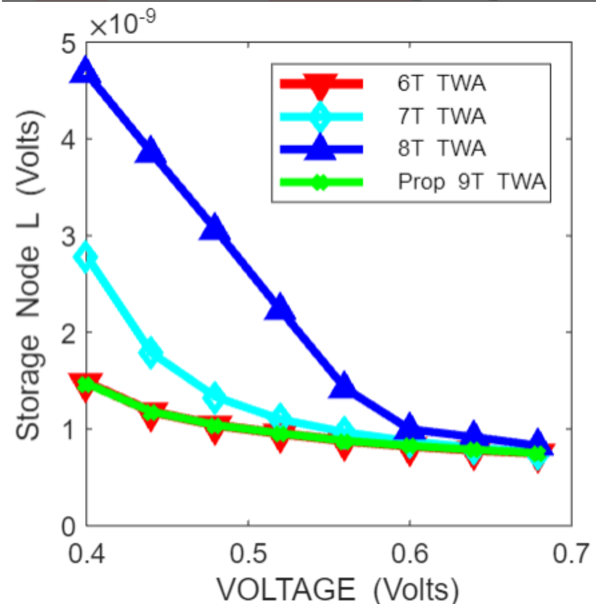

Fig-7 Write access time versus supply voltage.

Fig-7 shows the graphs of write access time of various existing circuits and proposed circuit.
From the figure it is clear that the TWA of proposed circuit is much better than 8T TWA and better than conventional 7T. When compared to 6T SRAM the values are almost similar.

D) Static Noise Margin Analysis:

The maximum noise that a circuit may tolerate during a reading or writing operation is specified as the static noise margin. The noise margin when writing is known as Write Static Noise Margin (WSNM), and the noise margin during reading is known as Read Static Noise Margin (RSNM) (RSNM) [10]-[15].

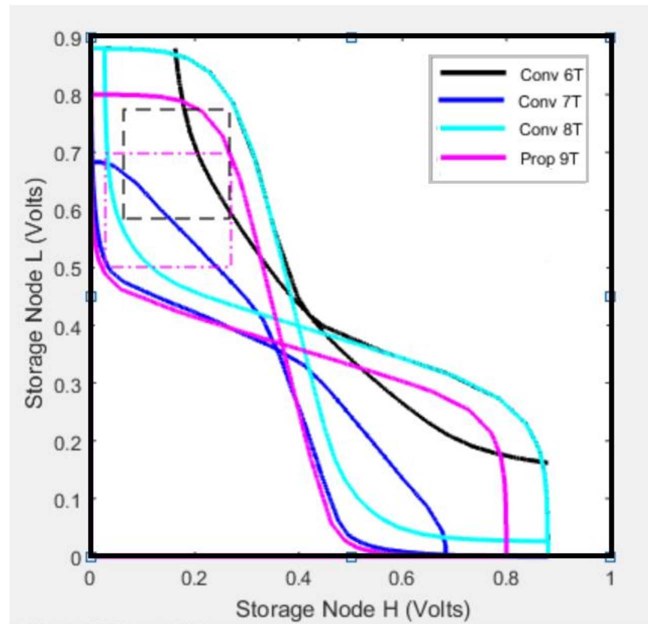

Fig-8 Read Static Noise margin vs Supply voltage

It specifies the amount of noise that can flip the current state of the bit line during a write operation and the amount of noise that can be tolerated in order to maintain the original data during a read operation [16]. Fig-8 shows RSNM figures for various circuits and proposed circuits.The read SNM is very good for the proposed 9T SRAM cell. The proposed circuit can tolerate high noise compared to other existing circuits.

E) Read Write Power Dissipation:

The power required to perform read or write operation is called read and write power of that circuit. The power while reading operation is called read power and the power while write operation is write power [17]-[21]. Fig-9 and 10 shows comparative analysis of read power and write power with existing design. Even though the proposed circuit consists of 9 transistors the power consumed by the circuit is less. This is due to individual working of read and write operations.

The power consumption during reading is almost similar to 6T ,7T and better than 8T. The power consumption during writing is almost similar to 7T and better than 8T

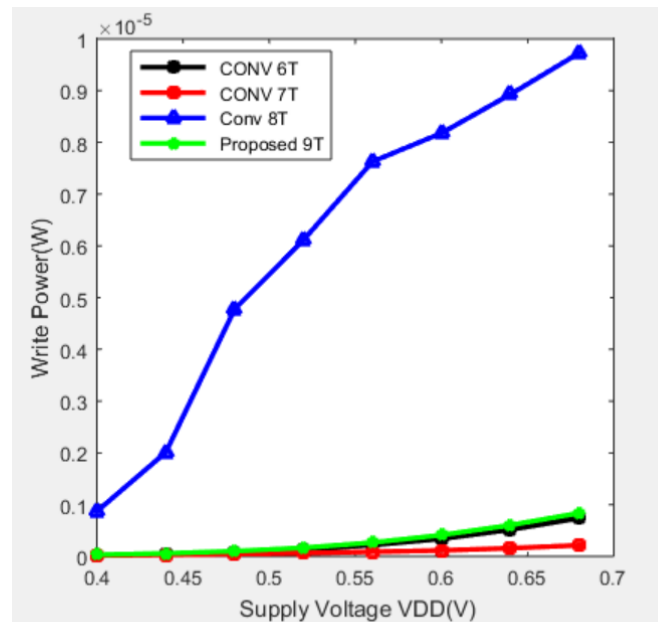

Figure-9 supply voltage vs write power

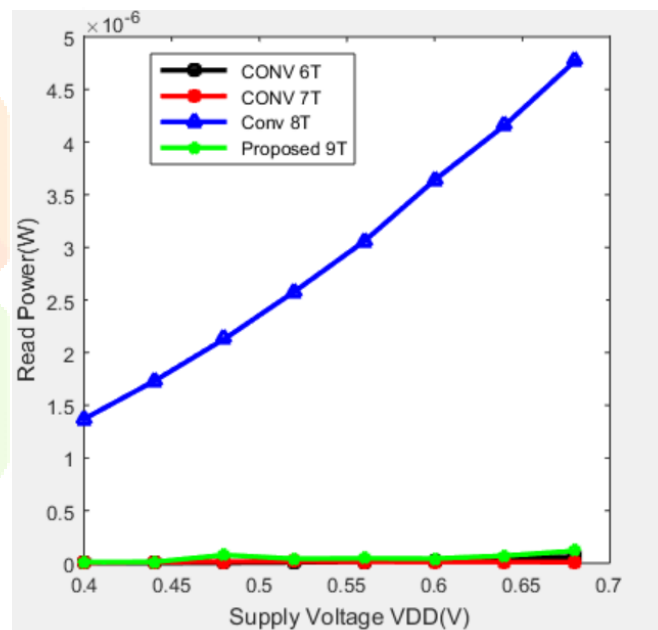

Figure-10 supply voltage vs read power.

F).Hold Power:

The leakage power when SRAM cell is not under use is known as hold power. Power consumption while circuit not under use it depending on the components used in the circuit. In the proposed model we used transmission gate in order to reduce hold power [21]-[23]. While read operation the writing part of circuit is off in order to consume less power and vice versa. The comparative results of hold power are shown below.

Table III

HOLD-POWER (P_{HOLD})

V_{DD} (V)	Conv 6T (W)	Conv 7T (W)	Conv 8T (W)	Prop 9T (W)
0.40	1.5E-09	1.1E-09	5.40E-06	1.50E-09
0.38	3.4E-09	9.1E-10	4.50E-06	3.40E-09
0.36	1.9E-09	7.3E-10	3.80E-06	1.00E-09
0.34	8.3E-10	5.9E-10	3.10E-06	8.30E-10
0.32	6.5E-10	4.7E-10	2.50E-06	6.50E-10
0.30	5.1E-09	3.7E-09	2.00E-06	5.10E-10

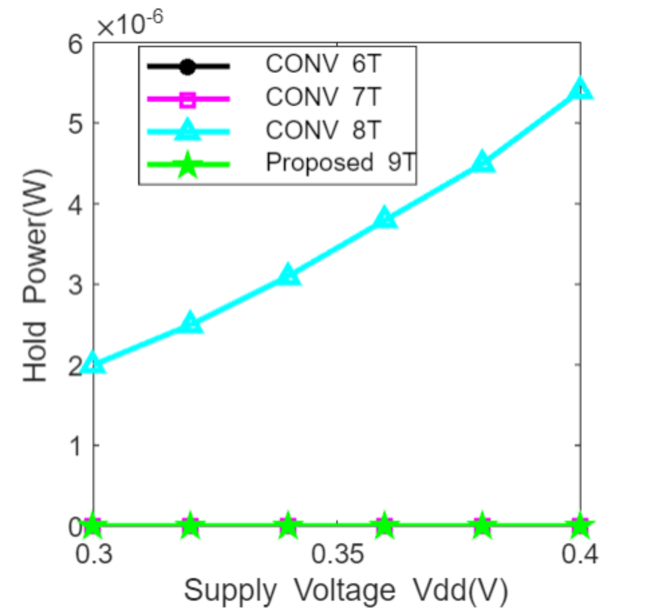

Figure-11 supply voltage vs hold power.

4.CONCLUSION

This paper presents working of our proposed 9T SRAM cell and showing better performance when compared to existing circuits. Especially the proposed circuit is showing high read stability. Most important design metrics of SRAM cell are investigated. The designs offering lower read/write delay, read/write power, enhanced RSNM are reported, to aid the designers in selecting the best cells depending on specific requirements.

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