



LOW POWER DYNAMIC RAM BASED SAR ADC FOR BIOMEDICAL APPLICATIONS

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Abstract- Analog-to-digital converters (ADCs) are used for digital signal processing in biomedical wearable devices, in implantable medical devices such as pacemakers, sensor interfaces such as in temperature and image sensors, and in the Internet of Things (IOT) applications . Several works have aimed to reduce the power consumption as the previously mentioned applications require low power for long term operations where the primary source of power is usually batteries. This introduces a new successive approximation register circuit (SAR) for SAR analog to digital converter (ADC) based on Dynamic Random Access Memory (DRAM) cells. Based on the proposed DRAM based SAR ADC and a differential capacitive DAC, a 10-bit ADC is designed in 0.18um CMOS technology.

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are one of the most important components in most electronic systems because they convert analogue signals to digital signals that are then processed by a digital signal processor (DSP). It is, in other words, the link between the analogue and digital worlds. The performance of the ADC has a direct impact on the data that the DSP processes. A appropriate ADC architecture should be carefully chosen and designed to match the performance requirements (resolution, sampling rate) while consuming the least amount of power possible. The tradeoff between performance and power consumption is of tremendous importance for applications such as portable devices or

implanted biomedical equipment where power is highly constrained. Biomedical devices, such as blood glucose monitors and pacemakers, frequently operate solely on batteries. As a result, it is preferable to completely utilise the energy without jeopardising the system's performance. Various strategies should be studied from the system level to the circuit level to obtain ultra low power consumption. Furthermore, the nature of bio-signal allows more options for power reduction.

A low-power, area-efficient 11-bit SAR ADC for biological applications is shown in [2]. An error cancelling capacitor network is used to provide an energy-efficient switching mechanism. The ADC was built using 0.18-um CMOS 2P4M technology, with a power consumption of 250nW at 0.75V supply voltage.

The author of [3] offers a new SAR circuit for SAR ADC based on DRAM cells. At 2V supply voltage and 100KHz sampling frequency, a 10-bit SAR ADC was developed using the DRAM circuit and a differential capacitive DAC in 0.18um TSMC technology. The suggested SAR was compared to the classic SAR to ensure that the new SAR reduces the static power of SAR ADC for biological applications. The suggested SAR consumes 26.24uW of power, and the Effective Number Of Bits (ENOB) for the proposed task is 9.26, with a maximum sampling frequency of 1MHz.

Later, for biomedical applications, a low-power 6-bit successive approximation logarithmic ADC is built [4]. To get a piece-wise linear approximation of the needed logarithmic function, the logarithmic ADC is constructed using a two-step consecutive approximation. 0.35- μm 2P4M technology with a supply voltage of 1.8V was chosen for the simulation and proposed ADC implementation. The ADC's power consumption ranges from 4.36 μW to 14.6 μW , according to simulation data.

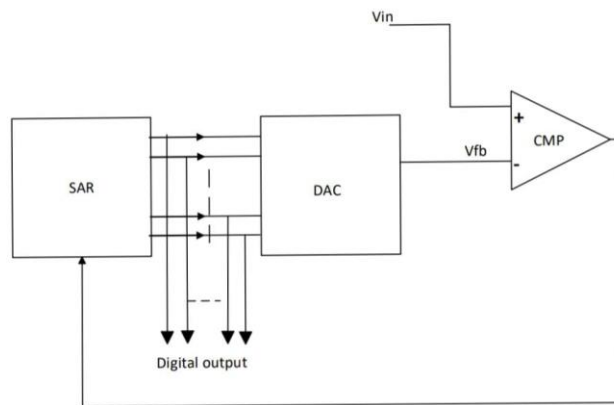


Fig.1. SAR ADC Block Diagram

The authors of [5] suggest a SAR ADC for biomedical applications that are portable. They used a D-Flip Flop to create an 8-bit low-power timed SAR ADC (DFF). The D-Flip Flop is used to implement the SAR's control logic. The simulations were carried out on LT-Spice utilising 90nm CMOS technology, with the SAR ADC drawing 88.76nW from 0.85V. A 10-bit SAR was proposed in [6] for the use of neural recording. To achieve low power consumption and a smaller footprint, a switching system based on energy-efficient common-mode voltage (V_{cm}) is used. Bootstrapped sample switches were employed in order to increase linearity. The ADC was made using 180nm CMOS technology and consumes 2.97 μW of power.

In [7], the authors provide a 12-bit SAR ADC for biological signal processing systems. We offer a multi-segmented DAC design as well as a hybrid switching strategy. To reduce leakage current and improve conversion accuracy, a novel ultra-low leakage switch for sample and hold and capacitor switch blocks is presented. The suggested SAR ADC is built in 130nm CMOS technology and runs on a 110nW supply voltage.

For biomedical implants, the authors suggest a 10-bit SAR ADC running at 0.3V [8]. They offer suggestions for improving ADC performance. To take use of the benefits of dynamic comparators while reducing kickback noise, a pipelined comparator is used. To fix the voltage offset without impacting the comparator's running speed, weight-biasing modification was applied. The use of a unity gain buffer improved the bootstrap switch leakage problem during the hold period while also lowering parasitic capacitances on the DAC. The ADC consumed 6.6 μW at 0.3V and was manufactured using 90nm CMOS technology. [9] presents an ultra low-power 10-bit SAR ADC for implantable medical devices. To attain nanowatt power consumption, a new switching strategy is proposed. The ADC was made in 0.18 μm 1P6M CMOS technology, with a power consumption of 38nW at 0.6V.

The authors of [10] present two low-power SAR ADC design approaches for biomedical applications. The proposed approaches include a dual split switch for the DAC to reduce leakage current and a set and reset phase to define the comparator's comparison and amplification phases, with the comparator's delay duration reduced. The ADC was constructed using UMC 180nm technology and consumed 13.99 μW at 0.5V supply voltage. The authors of [11] present a novel temperature and process-resistant comparator. A conventional comparator architecture used in SAR ADCs for biomedical applications was compared to this. 65nm CMOS was used to replicate the comparator's performance, which used 375 μW of power.

This work introduces a new SAR circuit and a two-stage comparator circuit for SAR ADC based on Dynamic RAM (DRAM) cells. A 10-bit SAR ADC was implemented using the DRAM circuit and a C2C DAC in 0.18um TSMC technology at 2v supply voltage and sampling frequency 100KHz

II. PROPOSED SUCCESSIVE APPROXIMATION REGISTER USING DRAM CELL

A. Dynamic memory cell (DRAM)

Dynamic random-access memory (dynamic RAM or DRAM) is a type of random access semiconductor that stores each bit of data in a memory cell, usually consisting of a tiny capacitor and a transistor, both typically based on metal-oxide-semiconductor (MOS) technology. Some DRAM memory cell designs merely employ two transistors, whereas others use a capacitor and transistor. When a capacitor is employed, it can be charged or discharged; these two states are used to represent the two values of a bit, which are commonly referred to as 0 and 1.

The electric charge on the capacitors gradually leaks away; without intervention the data on the capacitor would soon be lost. DRAM requires an external memory refresh circuit to prevent this, which rewrites the data in the capacitors on a regular basis, restoring their original charge. This refresh process is the defining characteristic of dynamic random-access memory, in contrast to static random-access memory (SRAM) which does not require data to be refreshed. DRAM is volatile memory (as opposed to non-volatile memory) since it loses data quickly when power is disconnected. However, DRAM does exhibit limited data remanence.

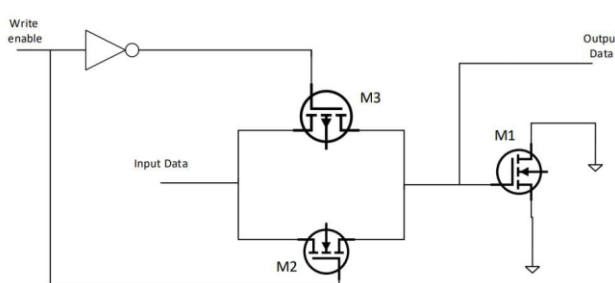


Table 1. Transistors sizing for DRAM cell

Transistor	W/L(um)
M1	2/1
M2	2/0.18
M3	4/0.18

Fig.2. DRAM cell used in SAR circuit

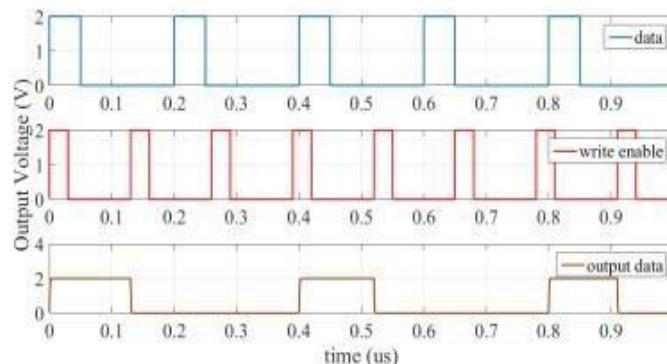


Fig.3. Simulation of proposed DRAMA cell

The parasitic capacitance of the transistor M1 is used by the memory cell in Figure 2 to store the data value. When the write enable signal is high, transistors M2 and M3 act as transmission gates, buffering data for M1. Furthermore, the read enable transistor is removed from this cell because the SAR's entire cells must be read once the read session is completed. The removal of the read enable transistor boosts cell speed while reducing cell area. As a result, the DRAM cell used with the SAR block is a custom cell to optimise the SAR performance. The proposed DRAM cell's performance is shown in Figure 2.

With a loading capacitance of 1pF, the simulation time is set to 1us. When the write enable signal is low, the parasitic capacitance of transistor M1 stores the value identically as a conventional DRAM cell, as demonstrated in the simulation. As this DRAM reading process is destructive, a data refreshment circuit is frequently used to keep the stored data safe. However, because the memory block is short and the data is read-only once, the SAR does not require a data refreshment circuit. The maximum storage duration, which is governed by parasitic capacitance, on the other hand, restricts the lowest speed of the DRAM cell and thus the SAR. Because of the smaller number of components used in the circuit, the DRAM cell is significantly smaller than the typical DFF; as a result, the SAR area is lowered, and the whole ADC area is also reduced.

B. SAR BLOCK

A ripple counter and a memory cell for each bit of the block are the fundamental components of traditional SAR. Flip-flops are a form of static memory structure that serves as a memory cell for data bits. The purpose of utilising a static memory structure is to save data for as long as possible or until the control system clears it. However, this is not required in the applications based on the SAR, where the data is read directly after the ready signal. Hence, the feature of data storage for a long time is not required for the case of the SAR. The static memory cell used for data storage is replaced with a dynamic memory structure to minimize the area and power consumption.

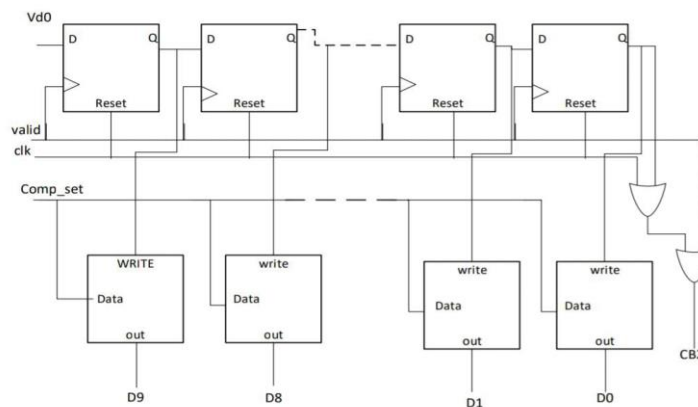


Fig.4. Block diagram of proposed SAR using DRAM cell

The suggested ADC generates the required clock signals internally using an asynchronous control circuit. Clk_s is the sampling clock, Valid is the signal that the comparator has completed its work, and Clk_c is the comparator control clock. The DFF array's output samples the digital output and controls the CDAC logic. Clk_s is high at the start of the process for the required sampling period, and the comparator is reset, which means that the Valid signal is zero because $Comp_{out}$ is coupled to VDD. When the sampling clock ends and Clk_s becomes 0, Clk_c becomes 0 as well, and the comparator begins to compare its inputs as Clk_c approaches its negative edge. $Comp_{out}$ is changed to 0 or 1 depending on the polarity of the input when the comparator reaches a judgement.

When the Valid signal is changed to 1, the first flip-flop is triggered, and the first DFF output is changed to 1. $Write_1$ is the clock that samples the first digital output bit and uses the SAR switching mechanism to operate the DAC. When Valid is set to 0, Clk_c is set to 1 and the comparator is reset. The Valid signal is then reset to 0, and $Comp_{out}$ returns to 1. Clk_c returns to 0 when the Valid signal flips to 0. So the comparator continues comparing its inputs again, and so on, until all of the appropriate clocks have been generated, and the next sampling phase has reset all of the flip-flops.

However, because the memory block is short and the data is read-only once, the SAR does not require a data refreshment circuit. The maximum storage duration, which is governed by parasitic capacitance, on the other hand, restricts the lowest speed of the DRAM

cell and thus the SAR. Because of the lesser number of components utilised in the circuit, the DRAM cell is significantly smaller than the typical DFF; as a result, the SAR area is lowered, and the whole ADC area is also reduced.

III. APPLYING THE PROPOSED SAR LOGIC IN 10-BIT ADC IMPLEMENTATION

A. Comparator design

For low-power applications, designing a comparator with low power and high speed is a challenging task. Analog to digital converters generally use comparators. A one-bit analog to digital converter is also known as a comparator. Because a comparator compares two voltages or currents and produces a digital signal that indicates which is larger. A comparator is built up of differential amplifiers with particular functions. These are commonly found in ADCs (analog to digital converters) and relaxation oscillators, which measure and transform analogue signals into digital form. The output value of the comparator indicates which of the inputs is greater or lesser. The comparator falls under non-linear applications of IC's. An op-amp has two input terminals, hence an op-amp based comparator compares the two inputs and outputs the result of the comparison.

A comparator requires a differential input and sufficient gain to be able to achieve the desired resolution. As a result, the two-stage op amp is an ideal comparator implementation. Because the comparator is typically used in an open-loop mode, it is not necessary to compensate the comparator. In reality, it is preferable not to compensate the comparator so that it has the widest possible bandwidth, as this will result in a faster response. Comparators that use a high-gain stage to drive their outputs between VOH and VOL for extremely small input voltage variations are an important category.

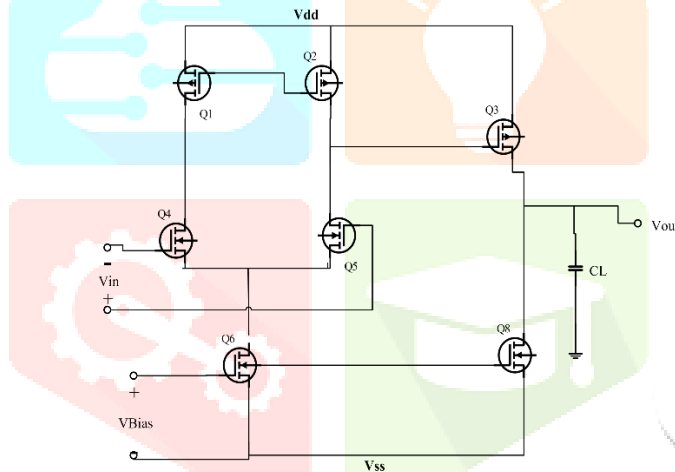


Fig.5. Comparator Schematic

B. DAC Design

For DAC design, capacitor arrays are commonly used. C2C DAC is the most used capacitive DAC design because of its tiny capacitance ratios, high conversion rate, and low power consumption. The C2C DAC schematic is shown below. The 10-bit Successive Approximation Register (SAR) controls the digital inputs to the DAC. As illustrated in the diagram, SAR digital bit outputs are sent to switches. The digital bits are sent through DAC switches, which then switch the output voltage between Vref and GND. The output of the DAC in digital bits is computed as

$$V_{out}C_{total} = C_{effective} * V_{ref} * \left(\sum_{i=0}^{N-1} b_i 2^{-(N-i)} \right)$$

Where b_i is the SAR control logic's digital input bits. C_{total} is the total effective output capacitance of the C2C ladder network which is equal to $2C_u$, where C_u is the unit capacitance. The overall capacitance spread of the C2C 10-bit DAC is $29C_u$, which is significantly less than the $1024C_u$ capacitance of a binary weighted capacitor array DAC. The originality of the developed C2C DAC now rests in the unit capacitor value selection in order to achieve high performance with little parasitic capacitance effect.

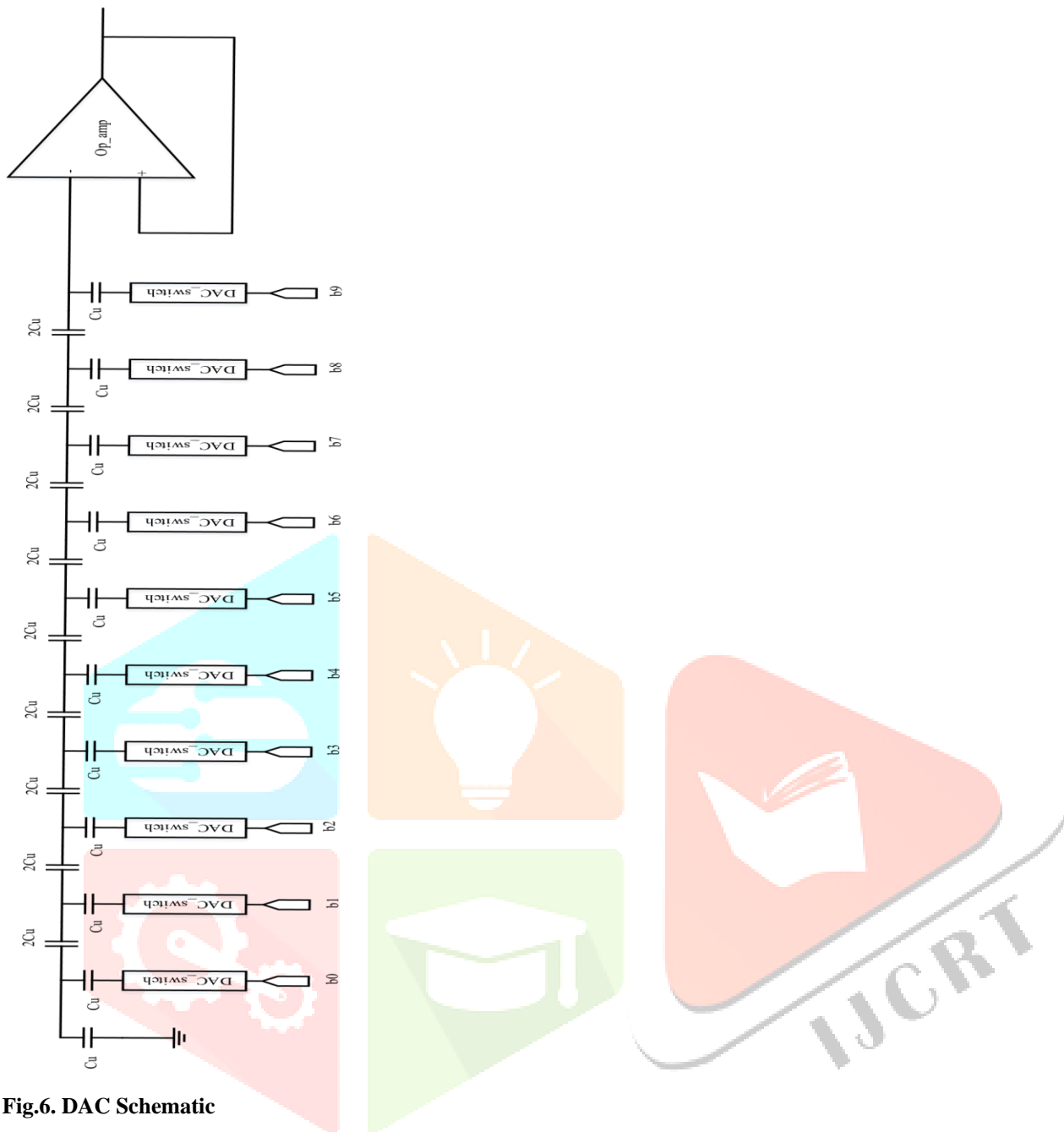


Fig.6. DAC Schematic

Op Amp Design

To maintain stability for the output DAC signal, this DAC design uses a two-stage op amp with miller compensating capacitor (C_c) and nulling resistor (R_z). As shown in Figure, the first stage is an NMOS differential pair, followed by a PMOS common source amplifier.

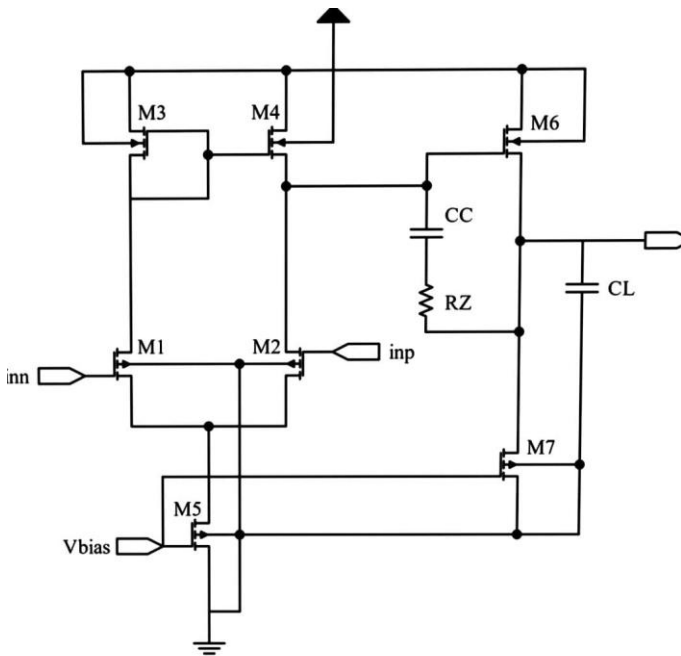


Fig.7. OP AMP Schematic

IV. CONCLUSION

This paper proposes a DRAM-based successive approximation register (SAR). When compared to the typical SAR block, the proposed SAR had a lower power consumption. From the simulation results, the proposed SAR, performs the same as the conventional SAR block. ADC is built based on the proposed SAR and compared to an ADC based on the traditional SAR to test SAR performance.

At 100KHz sampling frequency , the static power of an ADC based on the proposed SAR is 22.34uW, classic SAR-based ADC is 43.56uW. These findings support the hypothesis that SAR ADCs based on DRAM cells consume less power. The simulations were carried on using 0.18um TSMC.

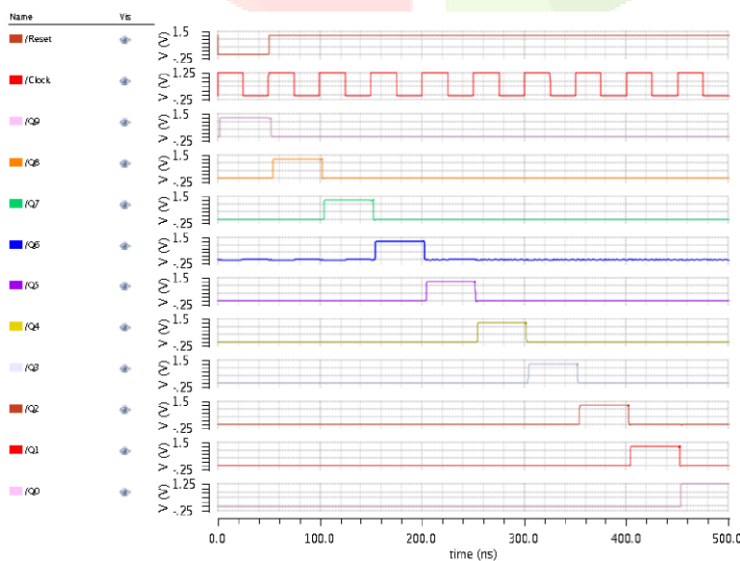


Fig.8. Output of SAR ADC

Table 2 Comparison table

Points of comparison	Proposed SAR	Traditional SAR
Resolution(bits)	10	10
Supply voltage(V)	2v	2v
Power Cumption	22.34uW	43.56uW

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