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DESIGN OF CMOS TWO STAGE OP AMP AND DIFFERENTIAL AMPLIFIER USING CADENCE VIRTUOSO

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INTRODUCTION

In VLSI design of Op-amp is classified under the category of analog-integrated circuits. Op-amp is operational amplifier providing various characteristics such as large bandwidth, High input impedance, Large gain, Low output impedance It requires 2 supplies with positive and negative equal magnitude, practically, inverting non-inverting. Actual design of Op-amp using CMOS consists of 5 NMOS and 3 PMOS transistors. Based on the configuration Op-amp can also be used as a integrator, differentiator, ADC converter etc

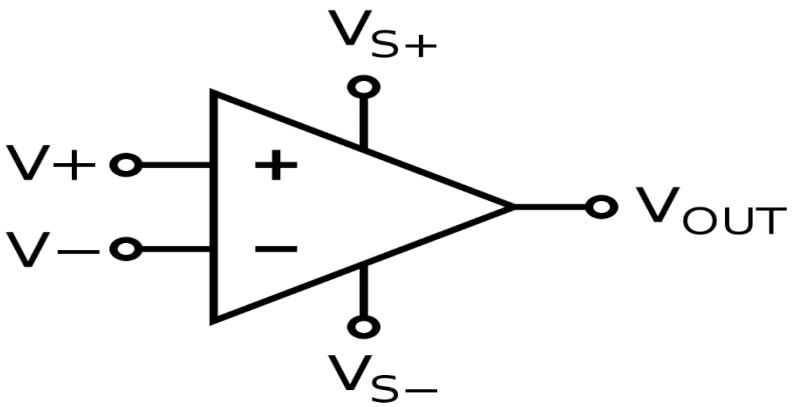
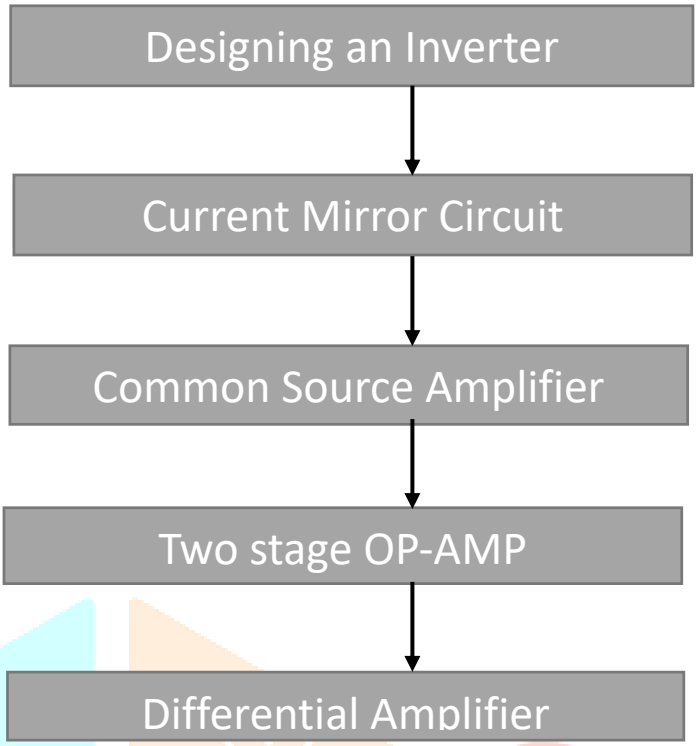


Fig 1. Differential amp

DIFFERENTIAL AMPLIFIER DESIGN FLOW



MOSFET

The behaviour of an enhancement n-channel metal oxide field transistor (NMOSFET) is largely controlled by the voltage at the gate (usually a positive voltage). For the usual drain- source voltage drops (i:e , the saturation region positive voltages from or few volts up to some breakdown voltage) the drain current Id is nearly independent of drain-source voltage Vds and instead depends on gate voltage Vg. In field-effect transistors (FETs), depletion mode and enhancement mode are two major transistors types, corresponding to whether the transistor is in an ON state or OFF state at zero gate-source voltage.

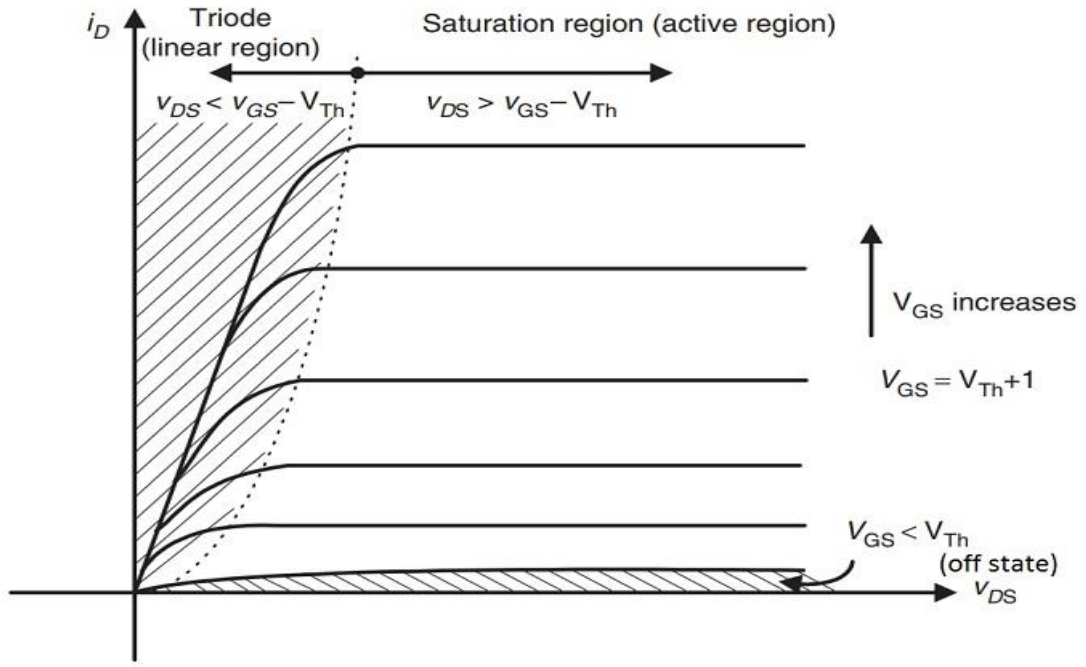


Fig 2. Charatersitics of mosfet

The characteristics of an nMOS transistor can be explained as follows. As the voltage on the top electrode increases further, electrons are attracted to the surface. At a particular voltage level, which we will shortly define as the threshold voltage, the electron density at the surface exceeds the hole density. At this voltage, the surface has inverted from the p-type polarity of the original substrate to an ntype inversion layer, This inversion region

A differential amplifier is a circuit that amplifies the difference between two input signals. Differential amplifiers are significant components in analogue systems' ICs (integrated circuits). The voltage difference present at the inverting and non-inverting terminal gets amplified where the output is received.The below figure shows the differential amplifier circuit designing.

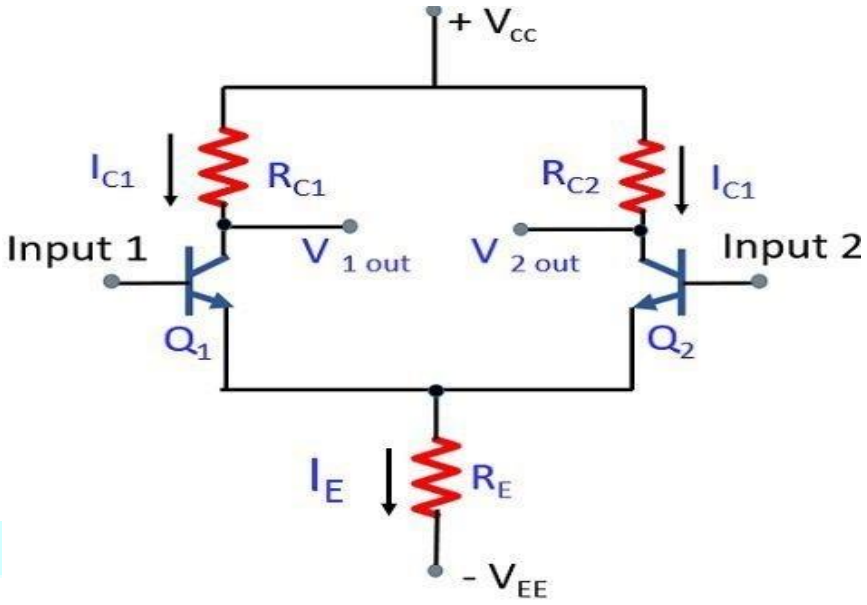


Fig 3. Differential amplifier

The differential amplifier's output can be represented in terms of Differential and Common modes. When both biases are at the same potential, common mode is the average of the two input signals.

Differential Mode

In differential mode, the transistor Q1 at the base a signal is applied and at transistor Q2 at the base no signal is applied. The Q1 functions in two methods, the first of which is the common emitter amplifier, where the input is applied at Q1 and the inverted output is produced at Q1.The common collector amplifier is shown next, with the signal appearing at Q1, which is in phase with the input. When the input signal drives the Q_1 transistor at the base it turns ON by the positive input signal and voltage drop across R_{C1} will be more and collector of Q_1 to be less positive.

SCHEMATIC DIAGRAM

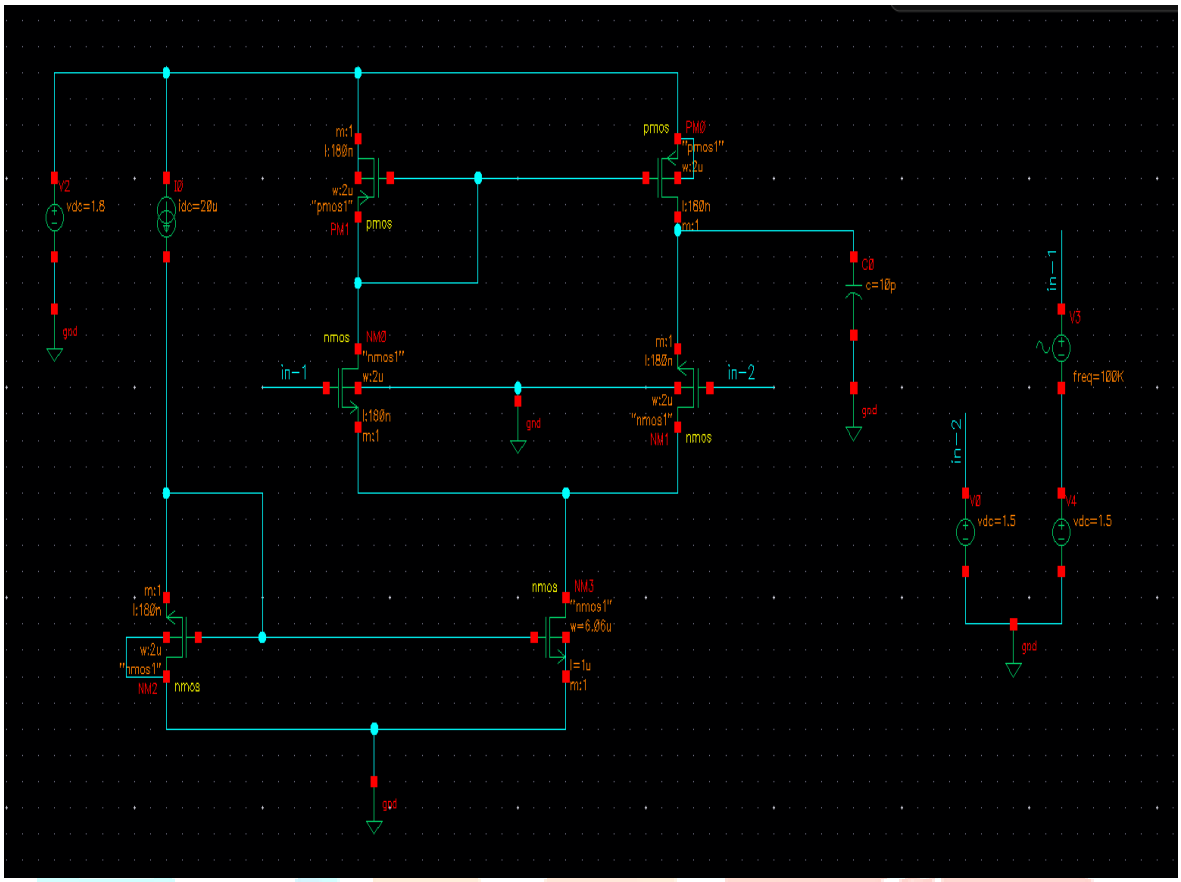


Fig 4. Schematic view

RESULTS

TRNASISTORS	Width (um)	Vds (mV)	Length(um)	Transconductance (uv)
PM0	6.06	952	1	123
PM2	6.06	952	1	125
NMO	13	-598	1	102
NM1	13	952	1	105
NM2	10.5	630	1	198
NM3	10.5	249	1	202

OUTPUT WAVEFORM

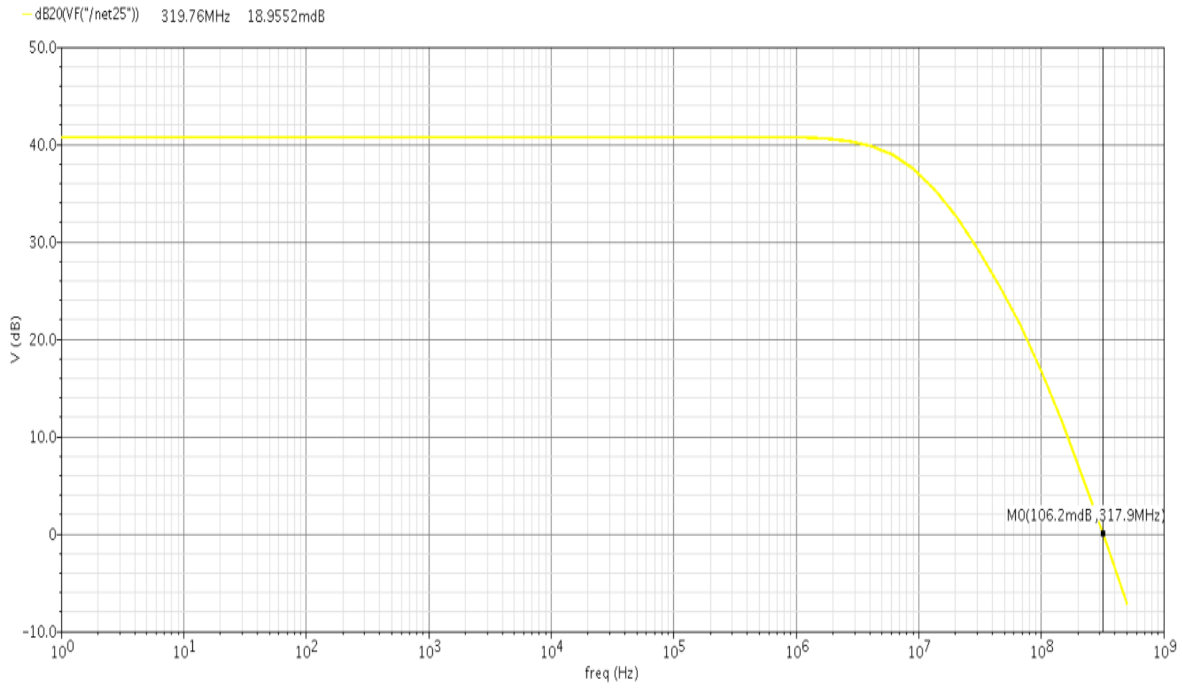


Fig 5. Output

These values were acquired by running a dc simulation with a schematic supply voltage of 1.8 v.Because power dissipation is a significant consideration in IC design.The above output shows the AC response of the schematic view.The frequency range is between the 100Hz to 100GHz and we get the frequency operating point at the 319.76MHz.Ad is the voltage gain for the difference signal, while AC is the voltage gain for the common mode signal. The common mode rejection ratio measures a differential amplifier's capacity to reject a common mode signal (CMRR).The ratio of differential gain Ad to common mode gain AC is what this term refers to.

TWO STAGE OP-AMP

Operational Amplifiers regularly known as Op-amps, that are worked with various levels of many quality to be utilized to acknowledge capacities going from the dc inclination era to rapid enhancements.In electronic hardware the operational amplifier is the standard among all the helpful gadgets.The operational amplifier has more number of applications in circuit designing like exchanged capacitors, square wave generators sigma delta A/D converter, test and hold speakers etc.Operation amplifier is the are direct one which have about every one of the commodity required for exact DC amplification.As well as the output waveforms are broadly used for the different operations like shifting.

SCHEMATIC DIAGRAM

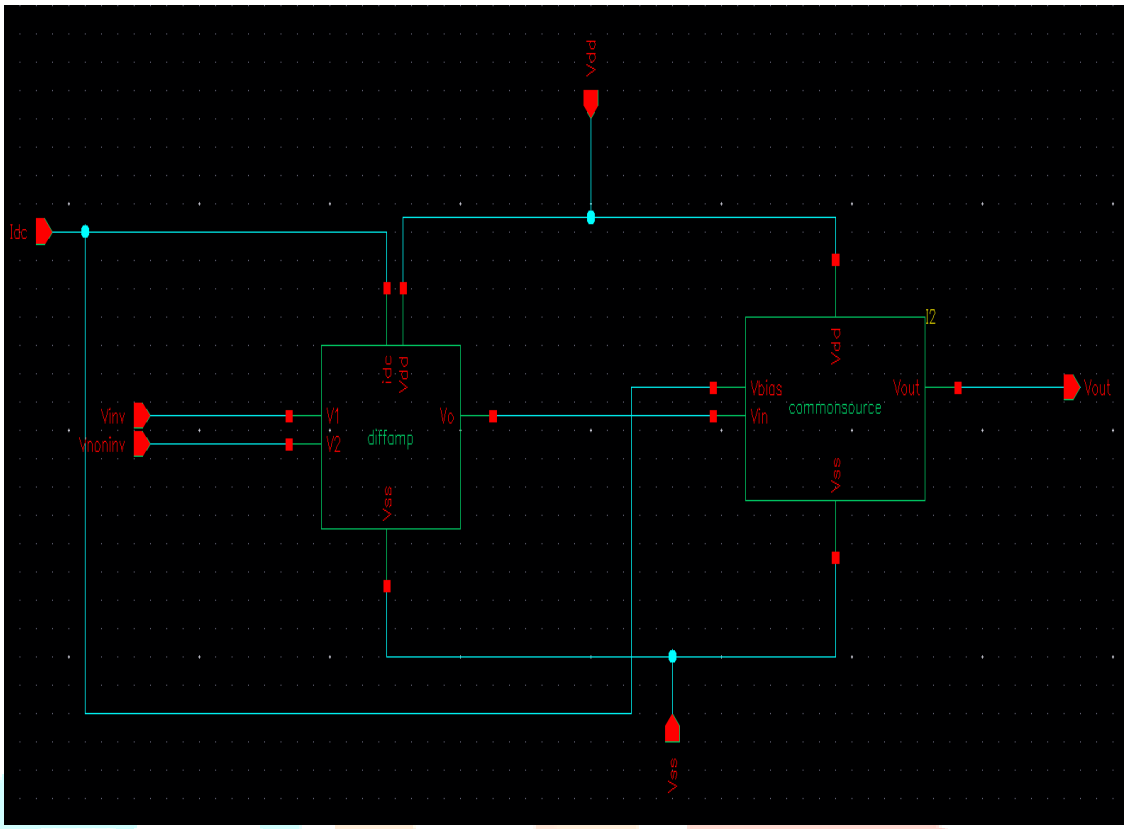


Fig 6. Schematic view

The open-loop gain of the OP AMP should be very high, so when the closed-loop gain becomes independent of open-loop gain then it takes negative feedback.The below schematic shows the two stage of the operational amplifier. The schematic shows the combinations of CMOS two stage op amp with the differential amplifier and the common source amplifier. Differential Amplifier provides the high gain pick up signal and common source amplifier also extends the gain and gives high gain voltage swing.The differential amplifier has an altering input and non-inverting input and also it has the two data sources which gives the differential voltage gain. Common Source amplifier produces current gain and voltage gain.

OUTPUTWAVE FORM

TRANSIENT RESPONSE

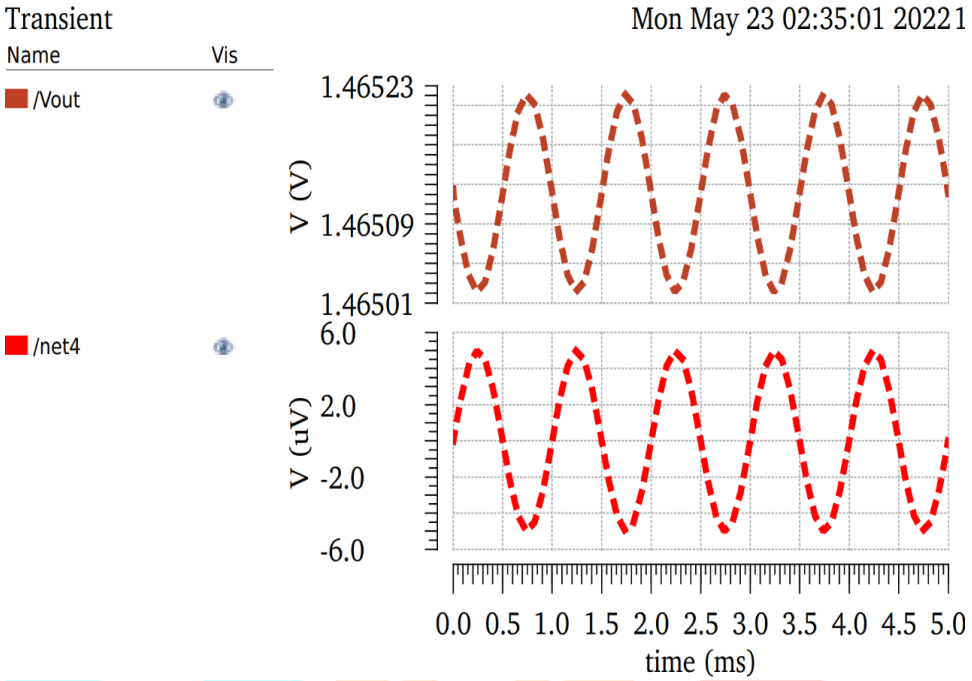


Fig 6. Transient response

AC RESPONSE

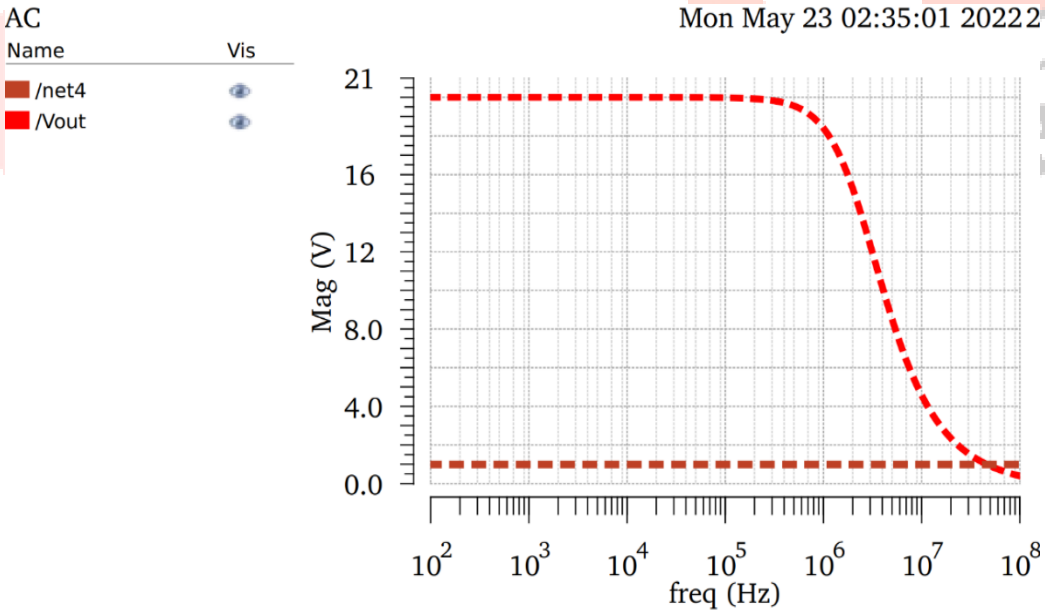


Fig 7. AC response

Parameters	Values
Vdd	5V
Vss	-2.5v
I_{dc}	30µA
Frequency	1k

CONCLUSION

From results and gain bandwidth analysis it can be concluded that variation is MOSFET parameters that is device width results into increase in bandwidth but is mandatory of a MOSFET to operate in Saturation region. Another conclusion can be made that If the MOSFET is not in saturation region the increase in width causes the current to increase which may lead to burn out of circuit. dominant pole effect has to be considered in order to achieve good stability. By keeping the device parameter i:e length constant channel modulation effect is reduced.

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