IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

# DESIGN OF LOW POWER HIGHER ORDER MULTIPLIER USIGN XILINX

**1Mr.M Rama Krishna,2 K.S wathi Swarupa ,3CH.Sravani, 4T.Keerthi**
**1Assistant professor, 2FinalB.Tech, 3FinalB.Tech, 4FinalB.Tech, 5FinalB.Tech**
**1Department of Electronics and Communication Engineering,**
**1 Andhra Loyola Institute of Engineering and Technology, Vijayawada, India**

*Abstract*— - **Nowadays the world becomes digital day by day. In this digital world arithmetic operations are playing the main role. In those multiplier plays a crucial role. But it takes more power than other arithmetic operations. When we perform with higher order multiplicants it takes more power to reduce the partial products.**

**For electronic world reduction of power consumption is the main objective. The proposed model mainly focused on the power consumption and time delay. When the power and delay decreases then automatically efficiency also increases. In the existed multiplier the technology node is 90nm, in this area is high so the proposed model also focused on technology node then size is reduced compared to the existed model. So, we are using Xilinx Vivado as it has additional features when compared with Xilinx ISE which is used in the existed model. The proposed model is efficient in power, delay and area. These all parameters are compared with the existed model.**

***Index Terms***—- **Multiplier, Xilinx Vivado, compressor, Verilog, field programmable gated array.**

## Introduction

Multiplication is the one of the four basic operations of arithmetic operations. It gives the results of combining groups of equal sizes. Nowadays these multipliers are widely used in the image processing and signal processing applications. Multiplication can be performed by a series of recursive additions. When the number to be added is multiplicants, these number of times it is added to the multiplier and the result is product. Each step of addition generates a partial products.

When comparing both exact multiplier and approximate multiplier there is no change in delay but the utilization varies. Due to this the transistor count is decreases when compared to the exact multiplier. Because of the count the power consumption and area decreases. The basic working of multiplier is to fold. That is computation of sub products and gathering of the shifted sub products. The speed of the multiplication can be increased by two methods first method is reducing the sub product and second method is increasing the speed of partial product. Partial products stages can be reduced by using compressors.

Compressors are the devices which is used to reduce the size of the partial products. we have different types of compressors. A compressor is a useful element that is mostly used in VLSI circuits and systems. Compressors are designed by using full adders, Ex-or mux and half adders. Here we are going to design a compressor with Ex-or mux that is called approximate compressor. That is more efficient in power [1] based on this parameter we are designing a multiplier using approximate compressor. The approximate compressor that is used in multiplier is 4:2 compressor.

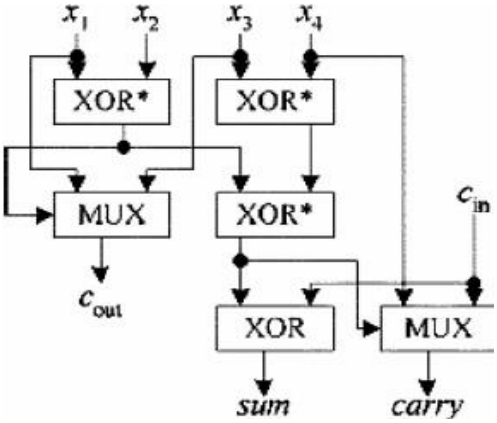



**Fig 1: Optimized 4:2 compressor**

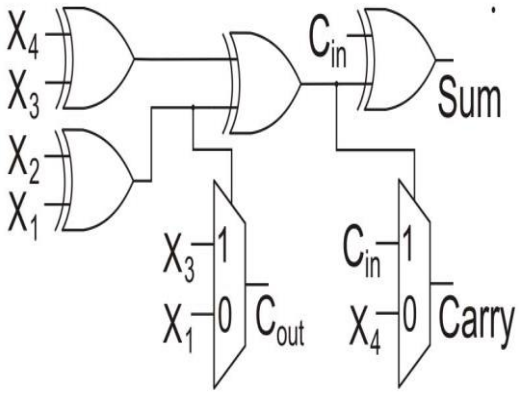



**Fig2: 4:2 Compressor using Ex-or-Mux**

## EXISTING SYSTEM:

4:2 COMPRESSOR IS CONSISTING OF TWO SERIALLY CONNECTED FULL ADDERS WITH MINIMAL CARRY PROPAGATION. HERE WE USE COMPRESSOR ADDER INSTEAD OF USING OTHER ADDERS. COMPRESSOR IS A DIGITAL MODERN CIRCUIT WHICH IS USED FOR HIGH SPEED WITH MINIMUM GATES REQUIRES DESIGNING TECHNIQUE. IN THIS 4:2 COMPRESSOR THE INPUT IS 4 BITS AND THE PRODUCED OUTPUT IS 2 BITS THAT IS SUM AND CARRY.

The multiplication is concluded with three steps as follows:

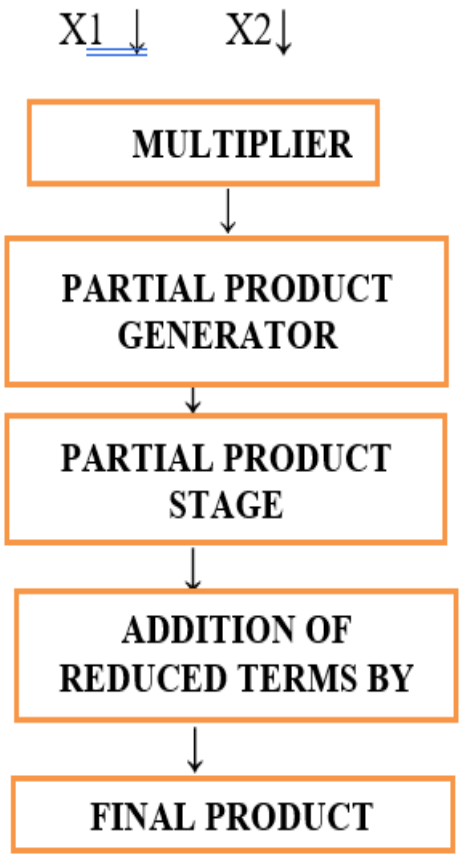



**Fig 3: Steps involved in multiplier using 4:2 compressor**

## SOFTWARE TOOL:

we are using Xilinx software for designing of Multiplier.It is founded by Mr. James V. Barnett II Ross in the year 1984, developed by integrated circuits industry in san jose,california, U.S.

Xilinx has two versions Xilinx ISE, Xilinx Vivado. Xilinx ISE is 2014 version with spartan 3A,3E,3,6 andVirtix 5,6 families. The technology node of Xilinx ISE is180nm-45nm. Its operating voltage is 5v.The new version of Xilinx is Xilinx Vivado. It is used from 2015 - till now. In the proposed design 2019.1version is used. It has additional features whencompared with Xilinx ISE based on the power, area and operating voltage (operating voltage is 1.8v-3.3v). It'stechnology node is 22nm-14nm. In this 7-seriesamilies are introduced. In the proposed model artix-7 series is used. Because it is ready -to- use platform designed by 7TM FPGA from Xilinx.

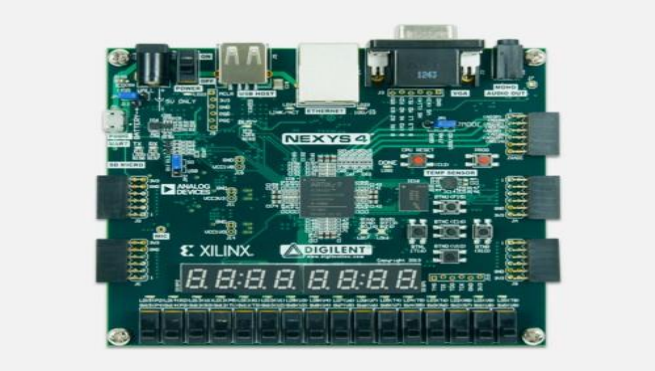



**Fig 4: Artix-7 series FPGA boar**

## Related work:

In the ancient days digital multipliers are designed by using Karnaugh map(k-map) and truth tables [2] which are complex multipliers. After they are replaced with compressors for designing low power multipliers. By using compressors four approximate subtractor [3] are designed for developing dividers. Generally, compressors are designed by using full adder [4] which are high power consumption multipliers. Now the multipliers are designed by using exact compressor [5] which is used to reduce power, area and delay. But it removes the noise so the degradation of quality is not effected the performances. New Noval compressor 4:2 compressor are designed with Ex-or-mux architecture to ensure low power approximate multiplier. The multipliers are designed with low area then the power consumption is reduced

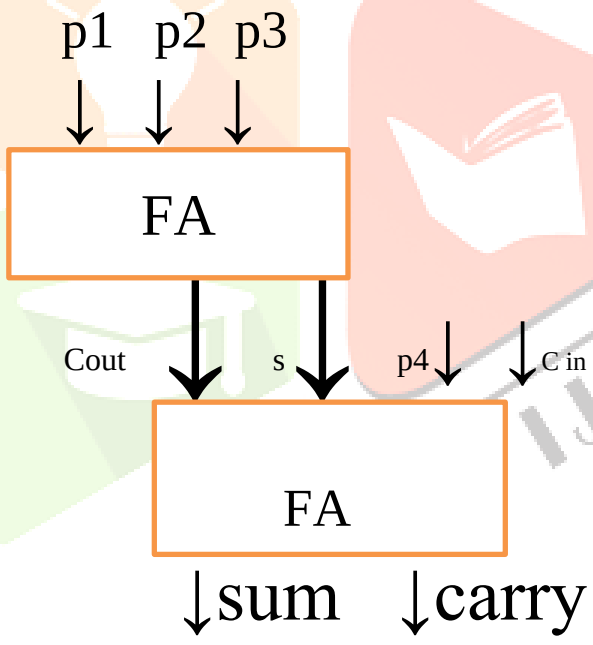



**Fig 5: 4:2 compressor using full adder**

## Existed model:

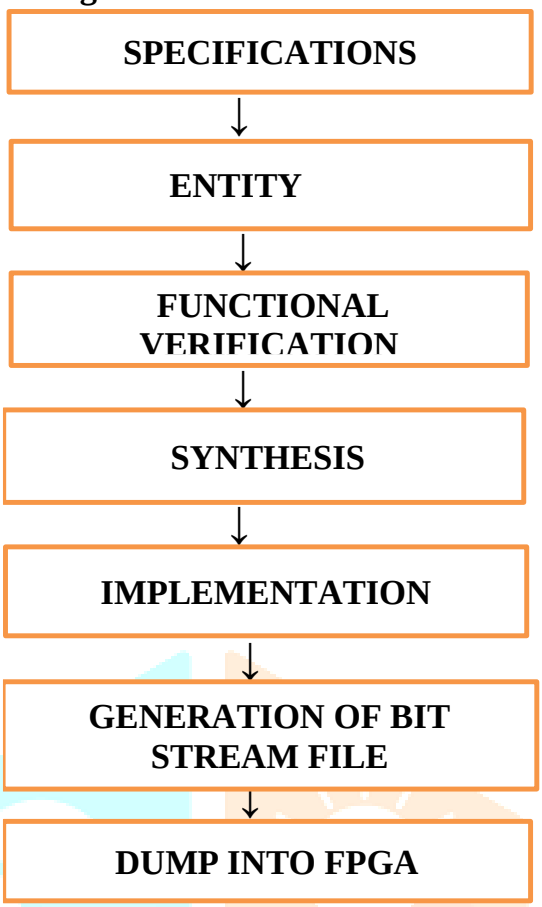
In the existed paper 8*8 ,16*16 and 32*32 bit exact multipliers are designed using Xilinx ISE software.Time delay, power consumption and area of the multiplier are observed. The ISE software is the first version of the Xilinx software it have less number of features. In the existed model the compressor which is used to designed the multiplier is designed using full adder.

In the existed model partial product generator is not used that is one of the drawbacks. Because the step to generate partial products is increased, then the consumed power is more and takes more time to produce products.

## Proposed model:

In the proposed model 8*8,16*16,32*32 bit approximate multipliers are designed by using Xilinx Vivado software. In these the multiplier is designed by using Ex-or mux compressor and partial product generator. The proposed model is more efficient when compared with existed in terms of power, time delay and area.

**Design flow:**




## Simulated results:

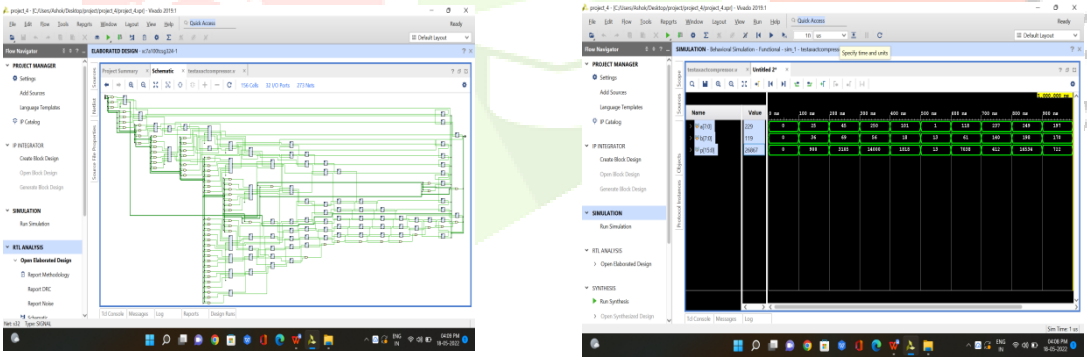


Fig: RTL Schematic of 8-bit multiplier and output waveforms of 8 bit multiplier

# Analysis of multipliers:

| | Time delay | Power consumption | LUT | |
|---|---|---|---|---|
| | | | Utilized | Available |
| 8x8 exact | 14.913us | 14.154uw | 92 | 63400 |
| 8x8 approximate | 10.509us | 9.861uw | 57 | 63400 |
| 16*16 exact | 27.461us | 35.724uw | 313 | 63400 |
| 16*16 approximate | 13.960us | 23.461uw | 187 | 63400 |
| 32*32 exact | 46.599us | 102.943uw | 1293 | 63400 |
| 32*32 approximate | 23.143us | 63.413uw | 724 | 63400 |

**Table1: Comparison table**

# Conclusion:

The design of existing and proposed multiplier is done with Verilog HDL. The power, area and the delay is calculated in the Xilinx Vivado compiler with 22nm technology library. From comparison table it is shown that the power and delay of the proposed multiplier are decreased by 7%. Here the utilization of LUT is reduced than the area of multiplier is also reduced. Then the proposed approximate multiplier is better than the existed multiplier in all performance metrics.

# References:

[1]MMD Savio and Deepa.,2020. Design of higher order multiplier with approximate compressor.IEEE Explore.

[2] Gorantla, A. and Deepa, P., 2019. Design of Approximate Subtractors and Dividers for Error Tolerant Image Processing Applications. Journal of Electronic Testing, pp.1-7.

[3] Kim, Y., Zhang, Y. and Li, P., 2014. Energy efficient approximate arithmetic for error resilient neuromorphic computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23(11), pp.2733-2737

[4] Zhou, Y., Lin, J., Wang, J. and Wang, Z., 2018, October. Approximate Comparator: Design and Analysis. In 2018 IEEE International Workshop on Signal Processing Systems (SiPS) (pp. 1-5). IEEE.

[5] Monajati, M., Fakhraie, S.M. and Kabir, E., 2015. Approximate arithmetic for low-power image median filtering. Circuits, Systems, and SignalProcessing, 34(10),pp.3191-3219

[6] Chang, C.H., Gu, J. and Zhang, M., 2004. Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 51(10), pp.1985-1997.

[7] Taheri, M., Arasteh, A., Mohammadyan, S., Panahi, A. and Navi, K., 2020. A novel majority based imprecise 4: 2 compressor with respect to the current and future VLSI industry. Microprocessors and Microsystems, 73, p.102962.

[8] Moaiyeri, M.H., Sabetzadeh, F. and Angizi, S., 2018. An efficient majority-based compressor for approximate computing in the nano era. Microsystem Technologies, 24(3), pp.1589-1601.

[9] Gorantla, A., 2017. Design of approximate compressors for multiplication. ACM Journal on Emerging Technologies in Computing Systems (JETC), 13(3), pp.1-17.

[10] Marimuthu, R., Rezinold, Y.E. and Mallick, P.S., 2016. Design and analysis of multiplier using approximate 15-4 compressor. IEEE Access, 5,pp.1027-1036.

[11] Guo, Y., Sun, H., Guo, L. and Kimura, S., 2018, October. Low-cost approximate multiplier design using probability-driven inexact compressors. In 2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) (pp. 291-294). IEEE.
[12] Marimuthu, R., Bansal, D., Balamurugan, S. and Mallick, P.S., 2013. Design of 8-4 and 9-4 Compressors Forhigh Speed Multiplication. American Journal of Applied Sciences, 10(8),p.893.
[13] Silveira, B., Paim, G., Abreu, B., Grellert, M., Diniz, C.M., da Costa, E.A.C. and Bampi, S., 2017. Power-efficient sum of absolute differences hardware architecture using adder compressors for integer motion estimation design. IEEE Transactions on Circuits and Systems I: Regular Papers, 64(12), pp.3126-3137.
[14] Schiavon, T., Paim, G., Fonseca, M., Costa, E. and Almeida, S., 2016. Exploiting adder compressors for power-efficient 2-D approximate DCT realization. In 2016 IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS) (pp. 383-386). IEEE.