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Design and Verification of NOR Flash Memory controller for Open Power-based Fabless SoC

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Abstract: Flash memory is a non-volatile electronic computer memory storage medium that can be erased and reprogrammed electrically. Flash memory is extremely durable and can withstand intense pressure or extreme temperatures. Flash memory is widely used for storage and data transfer in consumer devices, enterprise systems and industrial applications. NOR Flash memory is one of the two popular types of flash memory, the other is NAND Flash. NOR Flash is a type of memory cell created by INTELL in 1988. Read, write, erase, and reset are the four main operations available in flash memory. Verification is carried out to ensure the correctness of design. verification is performed to make sure that the design does not contain any bugs.in the process of verification, we are going to verify modules, SOC's (system on chip) by driving correct and an error input in both cases to observe the design is behaving as expected, if not then there will be a bug. This project aims to perform SoC verification of the NOR Flash memory controller which is connected to an Open Power processor, A20 core-based fabless SoC using the AXI4 interface.This SoC verification of the NOR Flash memory controller is done by Universal verification Methodology (UVM). The verification is carried out using software tools from Mentor Graphics Questa® and Xilinx Vivado®, respectively

Keywords: SoC, Memory Controller, NOR Flash Memory, AXI4, A2O

I. INTRODUCTION

NOR and NAND is two non-volatile flash memory technologies. Nand Flash is occupying U disk at a growing rate in terms of development. Nor Flash is used in embedded devices with smaller storage capacities in the embedded market, such as MP3/MP4 and mobile phones. NOR Flash controller design idea and source code analysis, Non-volatile flash memory technologies include NOR and NOR. It altered the circumstance where EPROM and EEPROM were used. NOR Flash was introduced by Toshiba. NOR Memory is a low-cost per-bit memory with good performance. The code must be read back into the system RAM. NOR has a high transmission efficiency and is particularly cost-effective at small capacities.NOR Flash has a high storage cell density but a slow erase and write speed. The data is stored in memory blocks. The blocks are used for erasing and programming. The erase procedure is completed first, and the writing procedure in FlashMemory is initiated only after all empty NOR devices have been wiped. Creating an erase operation in NOR is more straightforward when compared to NOR. On the other hand, Erasing NOR devices are implemented in blocks ranging from 8 to 32KB, and it only takes 4ms to perform the same operation.

A. A20 CORE

The A20 core is an out-of-order, multi-threaded, 64-bit WER Instruction. Set architecture core that was developed as a processor for embedded usage in the system-on-chip. It is best suited for single-thread performance optimization. It maintains the same modular design approach and fabric structure as its parent high-streaming throughput A2I predecessor. The uxiliary Execution Unit (AXU) is firmly coupled to the core, allowing many possibilities for special-purpose designs for new markets tackling the challenges of modern workloads. The A20 has improved single-threaded performance and supports 2-way SMT with POWER IS 2.07. The A20 core was designed to optimize single-threaded performance and is targeted at 3+ GHz in 45 nm technology.

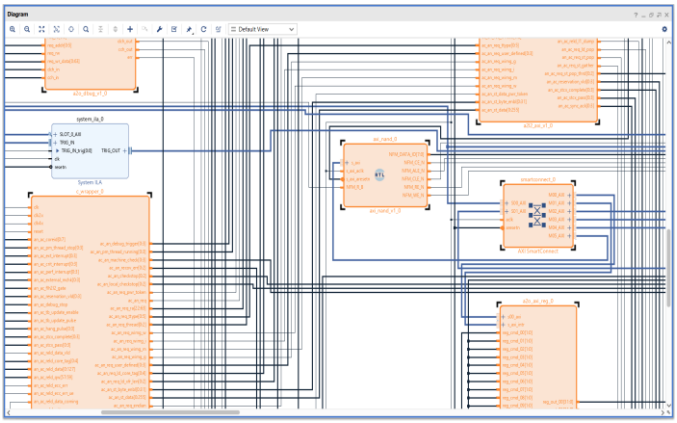

Fig 1. SoC Integration Block Design

Fig 2 contains a2o reg, a2o debug, core wrapper, NOR Flash Controller, AXI Smart connect,a2o_axi_reg and a2l2_axi. These modules Integrate with AXI Smart Connect

II. AXI4 NOR FLASH MEMORY CONTROLLER

1. Design Features

AXI4 host interface supports reset operation, auto select manufacturer ID operation, read operation, program operation, chip erase operation, and sector erases operation of NOR Flash memory.

Supports both Word configuration Flash memory and Byte configuration Flash memory Read/write cycle access time can be optimized for a specific NOR Flash memory through the setting of timing parameters in the design

2. Functional Description

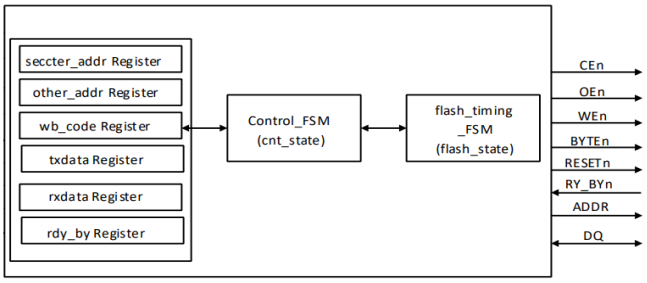

Fig 2. Nor Flash Memory Controller Block Diagram.

The functional block diagram of the NOR Flash Memory controller with the AXI interface. This design has a standard AXI slave bus that connects the NOR Flash memory device with a microprocessor and other on-chip components. From the AXI bus, this design appears as a set of addressable registers that can be read from or written to Through these registers, the AXI master can transmit and receive data and control the operation of the NOR Flash memory.

The control Finite State Machine (FSM) is used to enter the appropriate operational modes of NOR Flash based on the AXI code (wb_code) register which is set by the AXI master. For every operational mode of NOR Flash, the control_FSM calls a timing FSM to generate appropriate control signals to access the NOR Flash based on the NOR Flash memory timing specification

III. PROPOSED DESIGN

Verification environment for emulation in TBX Mode of Flash Memory Controller:

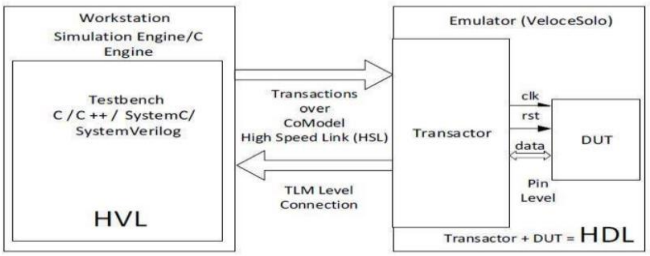

Fig 3. TBX Verification Block Diagram.

Unit testing for memory and the buffer was done. The block diagram shows the verification environment set up for emulation (BFM Hierarchical Access):

Verification Types:

1. Deterministic Approach
2. Functional Verification

Deterministic Approach:

- Establish a test environment
- Interface & Top Module Interactions
- Forcing input test vectors.
- Monitor DUT response on waveforms and transcript

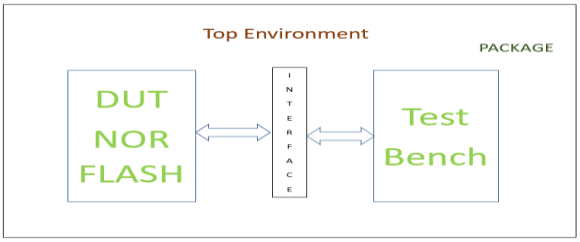

Fig 4. Deterministic Approach

Functional Verification:

- Create a test environment
- Interface
- Test Environment
- Top Environment
- Constraint Randomization
- Generating packets of test vectors
- Driving test vectors
- Monitor the response

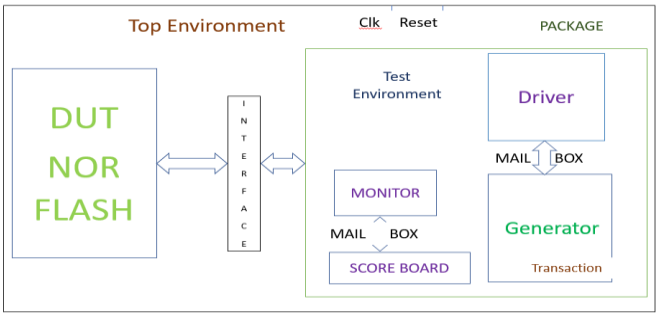

Fig 5. TBX Verification Block Diagram.

IV. SIMULATION RESULTS

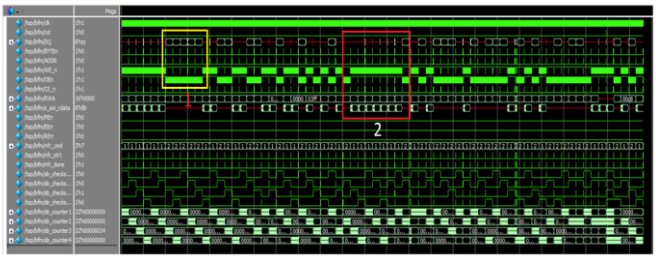

Fig 6. Simulation results of random read and writes data.

COVERAGE REPORT :

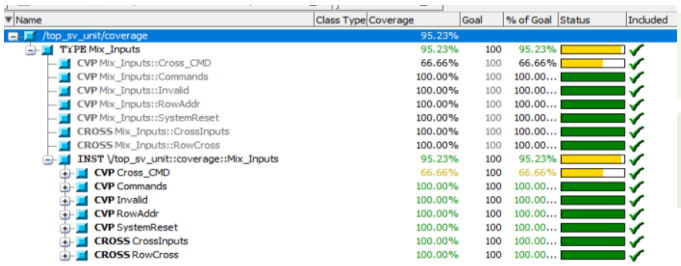

Fig 7. Coverage report of NOR Flash memory controller

Functional Verification Results:

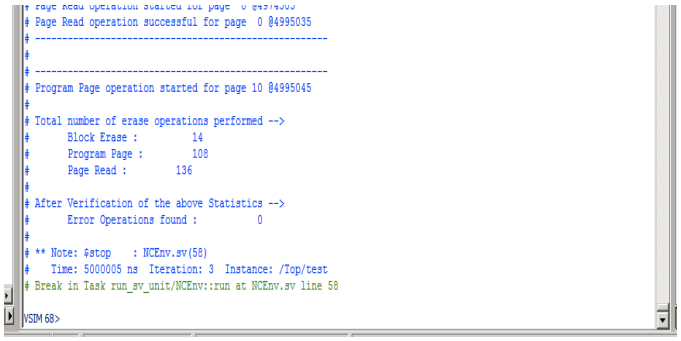

Fig 8. Test case report of Nor Flash memory controller.

TBX Simulation Statistics:

TBX Clock (Uclock) is the emulation clock and all other clocks are derived from Uclock. The clock spent in HDL time advancement is the design run period. The remaining TBX HDL).

TBX clocks spent in HDL due to calls are the clocks consumed by export calls. The percentage of HDL clocks spent in HDL time advance portrays how often the design clock pauses

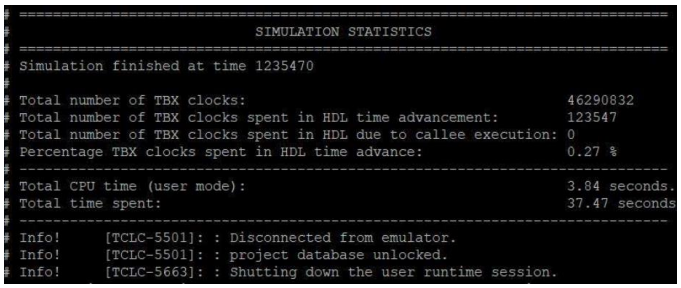

Fig 9. TBX Simulation Report for Nor Flash memory clock.

V. CONCLUSION

This work designed (slave interface and memory), simulated, and Verified the AXI4 NOR Flash Controller, which was utilized in A20 processor-based fabless soc. The Controller achieves great data write and read speeds in NOR Flash Memory. The controller works at This proposed architecture has the potential to Verifiy data transmission performance using AXI4. This design is verified in Xilinx Vivado and Mentor Questa using memory-based function verification. The plan for the future is to increase memory capacity and data transfer speed.

VI. REFERENCES

1. K. Khalifa, H. Fawzy, S. El-Ashry and K. Salah, "Memory controller architectures: A comparative study," 2013 8th IEEE Design and Test Symposium, 2013, pp. 1-6, doi: 10.1109/IDT.2013.6727083.
2. Xiaohu Wang and Zhaoming Huang, "Design and implementation of high-speed QSPI memory controller," 2013 IEEE 4th International Conference on Electronics Information and Emergency Communication, 2013, pp. 82-85, doi: 10.1109/ICEIEC.2013.6835459.
3. L. Bai, M. Wang and J. Yi, "Design of NOR FLASH data read-write controller based on FPGA," 2021 7th International Symposium on Mechatronics and Industrial Informatics (ISMII), 2021, pp. 104-110, doi: 10.1109/ISMII52409.2021.00029.
4. K. Khalifa and K. Salah, "Implementation and verification of a generic universal memory controller based on UVM," 2015 10th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS), 2015, pp. 1-2, doi: 10.1109/DTIS.2015.7127364.