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ENERGY-EFFICIENT QUANTUM-DOT CELLULAR AUTOMATA CIRCUITS

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Abstract: The design proposes energy efficient arithmetic circuits uses placement of QCA cells. These designs use novel logic circuitry called majority logic function and input re-ordering circuits. These circuits reduce the hardware circuitry and hence reduce the area occupancy. Quantum dot cellular automata are emerging nanotechnology that reduces the cell area, and power dissipation compared to CMOS architectures. The approximate full adders show notable improvements in terms of size, power consumption and energy dissipation. Conjunction of approximate computing and emerging nanotechnology could lead to very powerful and energy efficient integrated in frastructures.

Considering two different adder designs such as conventional full adder and approximate full adder. In a complete adder circuit, three one-bit values are added; two of the three bits are known as operands and the third is referred to as the bit C_{in}. Output C_{out} and sum are terms used to describe the 2-bit output that is generated. For approximate adders the hardware metrics like error distance, mean error distance and relative mean error are correlated. Optimized multiplexer to conventional multiplexer methods in terms of cell count, area clock delays and energy consumption.QCAD software used to stimulate the circuits and its waveforms. QCAD-E software is used to calculate the circuit values such as no of cells, area occupancy, total simulation time, energy dissipation

Index Terms **- QCA, Adder, Approximate Adder, Multiplexer, Power Analysis, Energy Dissipation**

I. INTRODUCTION

The world of electronics has been completely transformed by CMOS technology. The device has decreased by several orders of magnitude since it was created more than 40 years ago. Due to its downsizing, there has been continuous improvement in terms of price, effectiveness, and energy efficiency [1].

Due to the considerable scaling of the fundamental MOS transistor, the per-component reduction in VLSI has been made practical. Dennard's notion of scaling served as the inspiration for the successful downsizing of the MOSFET. Moore's forecast that the number of components on an integrated circuit would double every 18 months has held for longer than expected, but a new age has started in which the use of MOSFETs is constrained practically to gate lengths of less t han30 nm [2].

These are a few alternatives in CMOS technologies. Quantum-dot Cellular Automata (QCA), Resonant Tunneling Diodes (RTD) and Single Electron Transistors (SET) [5].

The Quantum Dot Cellular Automata developed by Lent is one of the prospective su bstitutes for CMOS technology. It proposes the idea of employing tiny structures like quantum dots to build cellular automata. The physics of the interaction between the electrons positioned in the potential wells is the basis of QCA. One option for nanost ructures to be employed in QCA is a quantum dot. About ten thousand times smaller than human hair, quantum dots are microscopic semiconductor crystals.

This paper presents the state-of-the-art survey on QCA basics, implementation, adder, approximate adder, and multiplexer. Also, the paper addresses optimizing circuits in QCA implementation. Further, the paper suggests the possible research area of QCA. The rest of the paper is organized as follows, Section II describes the QCA backgroun d. Section III describes the QCA adder, approximate adder, and multiplexer. The paper concludes in Section IV.

II. QCA BACKGROUND

2.1 QCA cell

A QCA cell has 2N quantum dots, where N is the maximum number of electrons that can tunnel through the quantum dots. The high potential barrier, however, prevents tunneling between the cells. To put it another way, we may say that a tunnel junction, which can be opened to allow for electron transit, connects the potential wells inside a cell.

The basis for the QCA's operational mechanism is the columbic interaction and quantum mechanical tunneling between the electrons confined in the wells. According to Coulomb's law, which states that because of columbic repulsion, electrons tend to occupy positions with the greatest amount of separation, the alignment of the electrons in the QCA cell is determined by these positions. By thinking about potential electron alignments in the cell, this may be theoretically grasped. The two potential polarizations are depicted in figure 1 since the QCA cell is a square construction. Binary 0 is represented by polarization at -1.00, and binary 1 by polarization at +1.00[4].

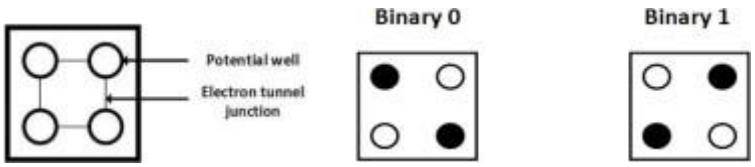

Figure.1: QCA cell and possible alignments of electrons

2.2 QCA binary wire

The idea of a wire is based on Coulomb's law, which directs electrons in nearby cells to align with the input cell to prevent electrostatic repulsion. For example, if the input cell has a polarization of -1.00, i.e. it is logic 0 then the adjacent cells follow the same alignment to achieve the state of maximum stability .

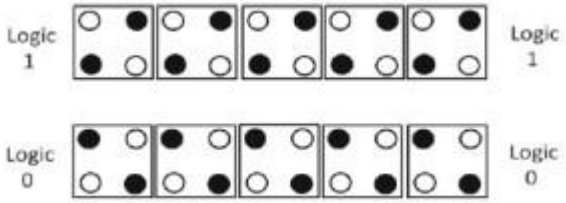

Figure.2: QCA binary wire

2.3 QCA inverter

Because of the inversion of the electron alignment brought on by columbic repulsion at the corner cell, the inverter as seen above functions. This is so that the electrons can anti-align about the input cell since the same polarization as the input would generate the most repulsion and instability .

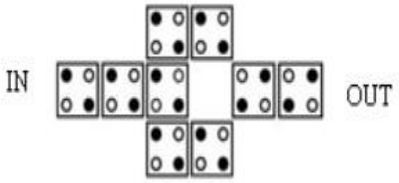

Figure.3: QCA inverter

2.4 QCA majority gate

This gate sets the value of the output cell based on the polarization of the majority of the inputs because that provides a ground state for the device cell (central cell).

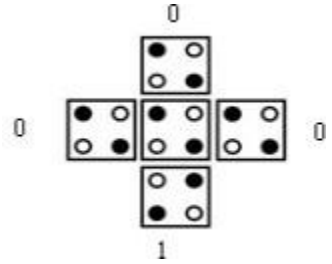

Figure.4: QCA majority gate

III. ADDERS IN QCA

3.1 Conventional full adder

It adds three inputs and generates two outputs. A and B generate the first two inputs, while 'C_{in}'is the third input. The outputcarry is designated as 'C_{out}' and the normal output designated as' S' which is a sum [9].

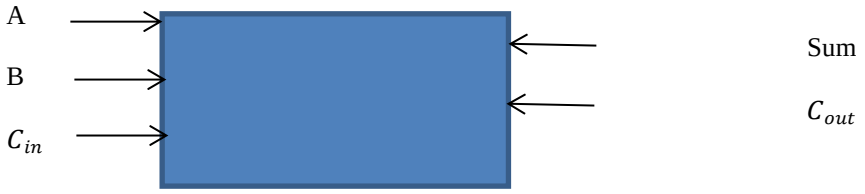

Figure.5: Block diagram of Full adder

'A' and' B' are the input variables. These variables represent the two significant bits that are going to be added. 'C_{in} ' is the third input which represents the carry. From the previous lower significant position, the carry bits are fetched. The 'Sum' and ' C_{out} ' are the output variables that define the output values. The eight rows under the input variable designate all possible combinations of "0" and "1".

Table.1: Truth table of Full adder

.

INPUTS			OUTPUTS	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simulation results of Full adder circuit

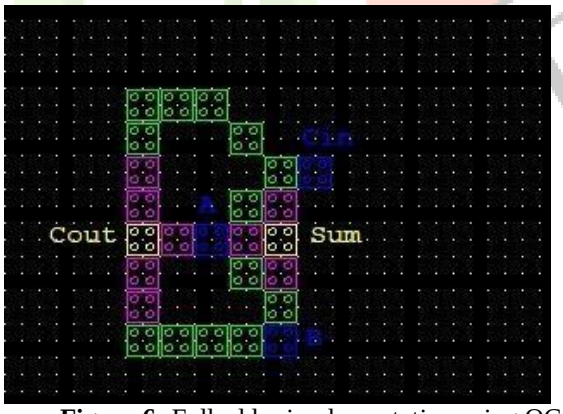

Figure.6: Full adder implementation using QCAD software

In this circuit, A and B are two one-bit inputs and C_{in} carry input and outputs sum, C_{out} .The circuit consists of 28 QCA cells.Two clocking zones are utilized in these circuits as follows: Violet indicates clock zone 1, Green indicates clock zone 0.

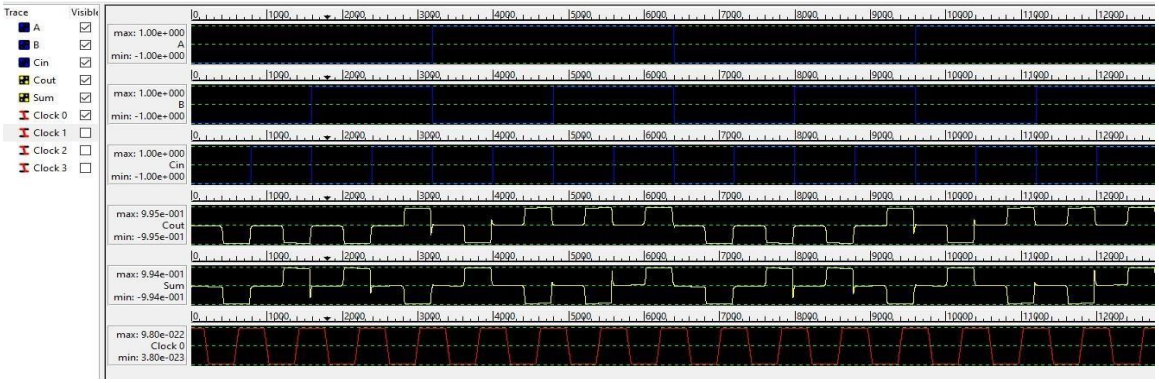

Figure.7: Full adder implementation output using QCAD software

By observing output waveform in QCAD software of Full adder circuit it has three inputs (A, B,C_{in}) and two outputs (Sum, C_{out}) and clocks. A, B, C_{in} represented in blue color. Sum,C_{out} represented in yellow color. Clocks represented in red color.

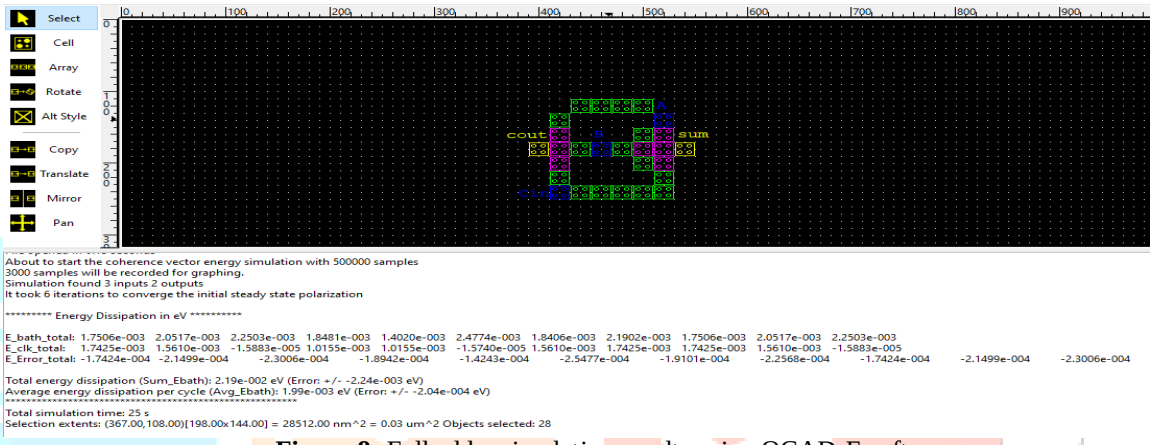

Figure.8: Full adder simulation results using QCAD-E software

Table.2: Full adder simulation result values in QCAD-E software

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_E bath)	Average energy dissipation (Avg_E bath)	Total simulation time	Selection extends	Objects selected
2.3458e-003 2.2840e-003 2.8680e-003 2.9555e-003 2.6183e-003 2.9962e-003 2.0649e-003 2.5988e-003 2.3458e-003 2.2840e-003 2.8680e-003	2.8831e-004 1.0166e-003 -6.1499e-004 5.9830e-004 5.9829e-004 -6.1449e-004 1.0166e-003 2.8833e-004 2.8831e-004 1.0166e-003 -6.1449e-004	-2.4469-004 -2.3711e-004 3.0243e-004 -3.1322e-004 -2.7575e-004 3.1659e-004 -2.1268e-004 -2.7280e-004 -2.4469e-004 -2.3711e-004 -3.0243e-004	2.82e-002 eV (Error: +/- -2.96e-004 eV)	2.57e-003 eV (Error: +/- -2.69e-004 eV)	19 seconds	(404.00, 130.00) [185.00 x 158.00] = 29230.00nm^2 = 0.01 um^2	26 cells

3.2 Approximate full adders

Approximate computing introduces errors, error metrics are required to evaluate the accuracy of approximate circuits. In most of the applications such as image processing, signal processing and video processing accurate calculations are not that much important because of the error-tolerant nature is present in the applications. As the applications are error- tolerant, the deviations cannot be identified by the human eye until it is a large deviation [10]**.** Here proposed approximate full adder using majority gate circuitry is shown in the figure.9.

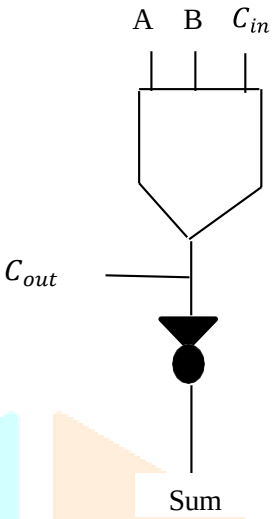

Figure.9: Approximate full adder circuit-1 logic diagram

The execution of the preceding design is based on introducing errors to the output for approximate circuit design. This circuit approximation is carried out utilizing the conventional process for probability calculation. In case:000 and case:111 for both these cases the values will be changed when compared to full adder truth table. Table 5.2 displays the truth table for the current approximate complete adder design**.**

Table.3: Truth table of approximate full adder circuit-1

Inputs			Full adder		Approximate full adder	
A	B	C_{in}	C_{out}	Sum	C_{out}	Sum
0	0	0	0	0	0	1
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	1	1	0

Simulation result of Approximate full adder circuit-1

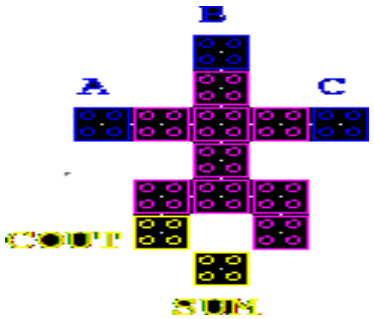

Figure.10: Approximate full adder circuit-1 implementation in QCAD

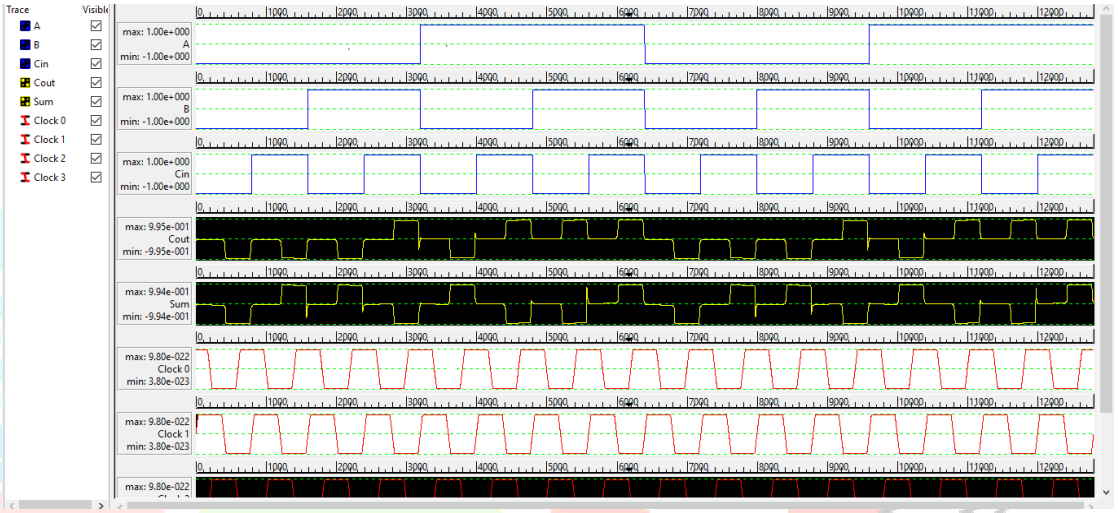

Figure.11: Approximate full adder circuit-1 implementation output in QCAD

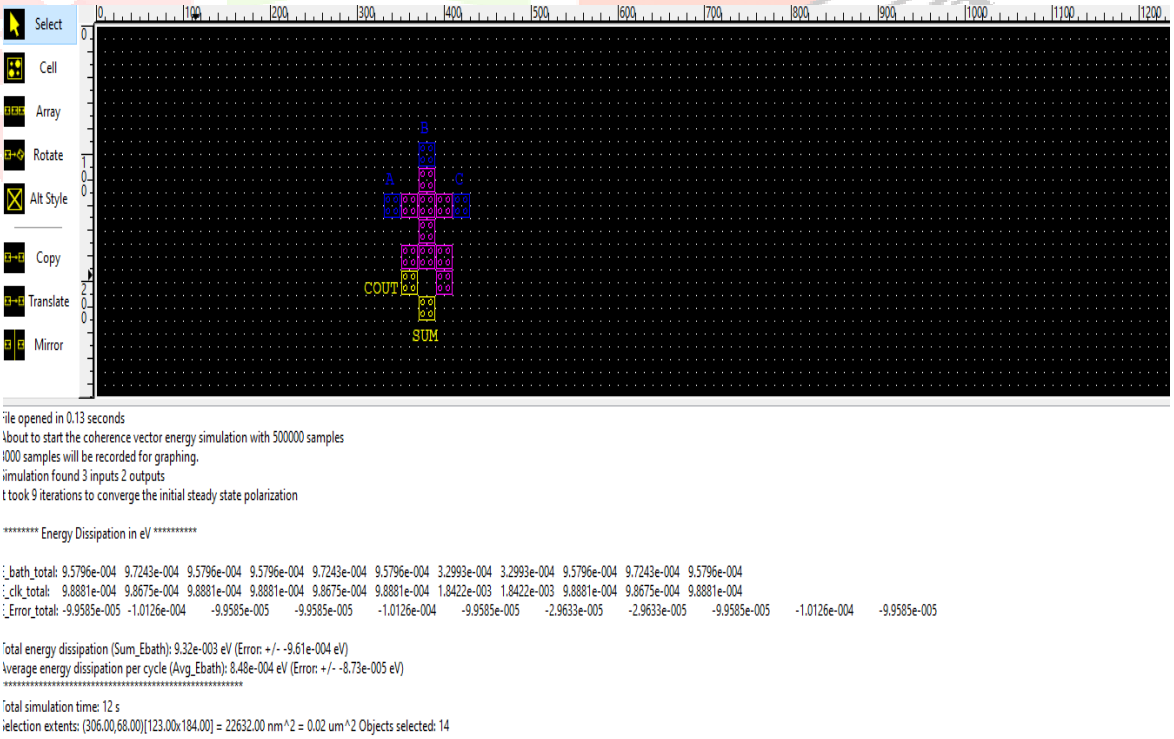

Figure.12: Approximate full adder circuit-1 simulation result in QCAD-E

Table.4: Approximate full adder circuit-1 simulation result values

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_ Ebath)	Average energy dissipation (Avg_ Ebath)	Total simulation time	Selection extends	Objects selecte d
9.5796e-004	9.8881e-004	-9.9585e-005	9.32e-003eV (Error: +/- 9.61-004 eV)	8.48e-004 eV (Error: +/- -8.73e-005 eV)	12 seconds	(306.00, 68.00) [123.00 x 184.00] = 22632.00nm^2 = 0.02um^2	14 cells
9.7243e-004	9.8675e-004	-1.0126e-004					
9.5796e-004	9.8881e-004	-9.9585e-005					
9.5796e-004	9.8881e-004	-9.9585e-005					
9.7243e-004	9.8675e-004	-1.0126e-004					
9.5796e-004	9.8881e-004	-9.9585e-005					
3.2993e-004	1.8422e-003	-2.9633e-005					
3.2933e-004	1.8422e-003	-2.9633e-005					
9.5796e-004	9.8881e-004	-9.9585e-005					
9.7243e-004	9.8675e-004	-1.0126e-004					
9.5796e-004	9.8881e-004	-9.9585e-005					

The approximation can be done at several phases of basic circuitry such as half adders, and full adders. Here, the proposed approximate full adder using the Majority gate circuitry is shown in Figure 13.

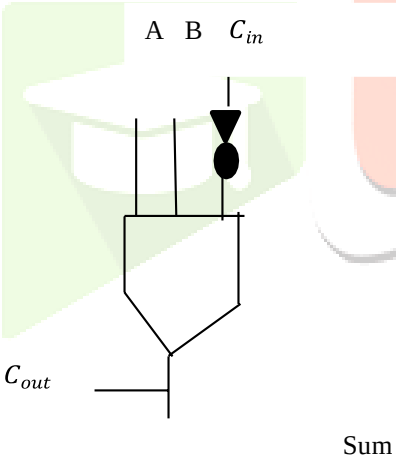

Figure.13: Approximate full adder circuit-2 logic diagram

The execution of the preceding design is based on introducing errors to the output for approximate circuit design. This circuit approximation is carried out utilizing the conventional process for probability calculation. In case:001 and case:110 for both these cases the values will be changed when compared to full adder truth table. Table 5.2 displays the truth table for the current approximate complete adder design.

Simulation result of Approximate full adder circuit-2

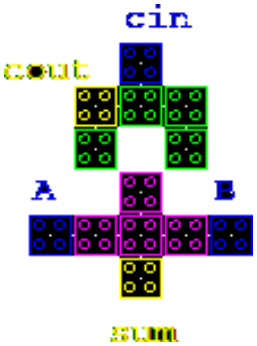

Figure.14: Approximate full adder circuit-2 implementation in QCAD

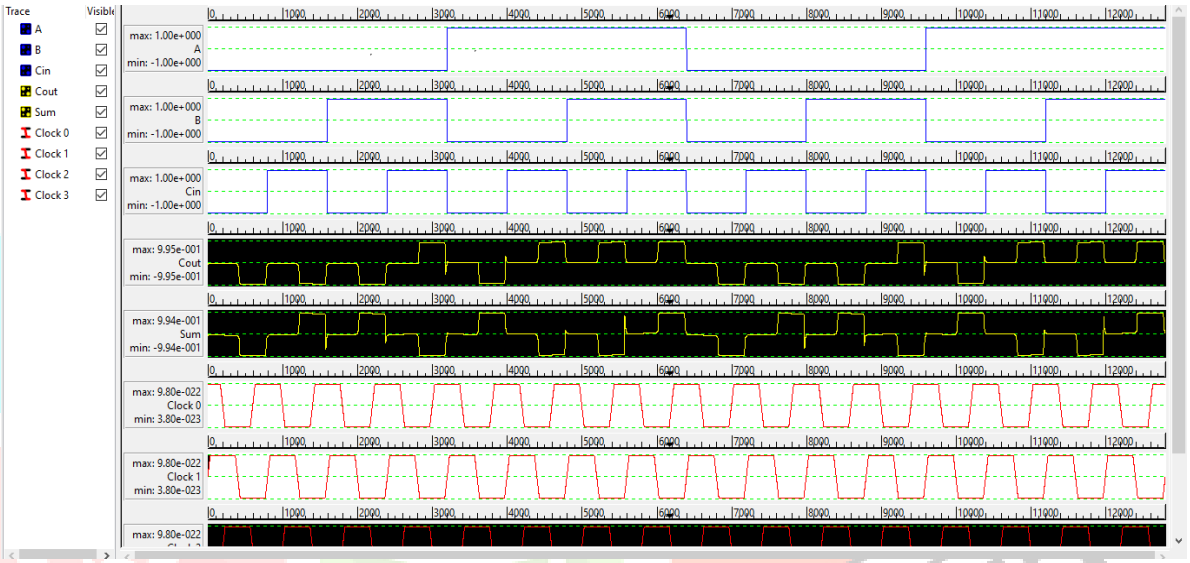

Figure.15: Approximate full adder circuit-2 implementation output in QCAD

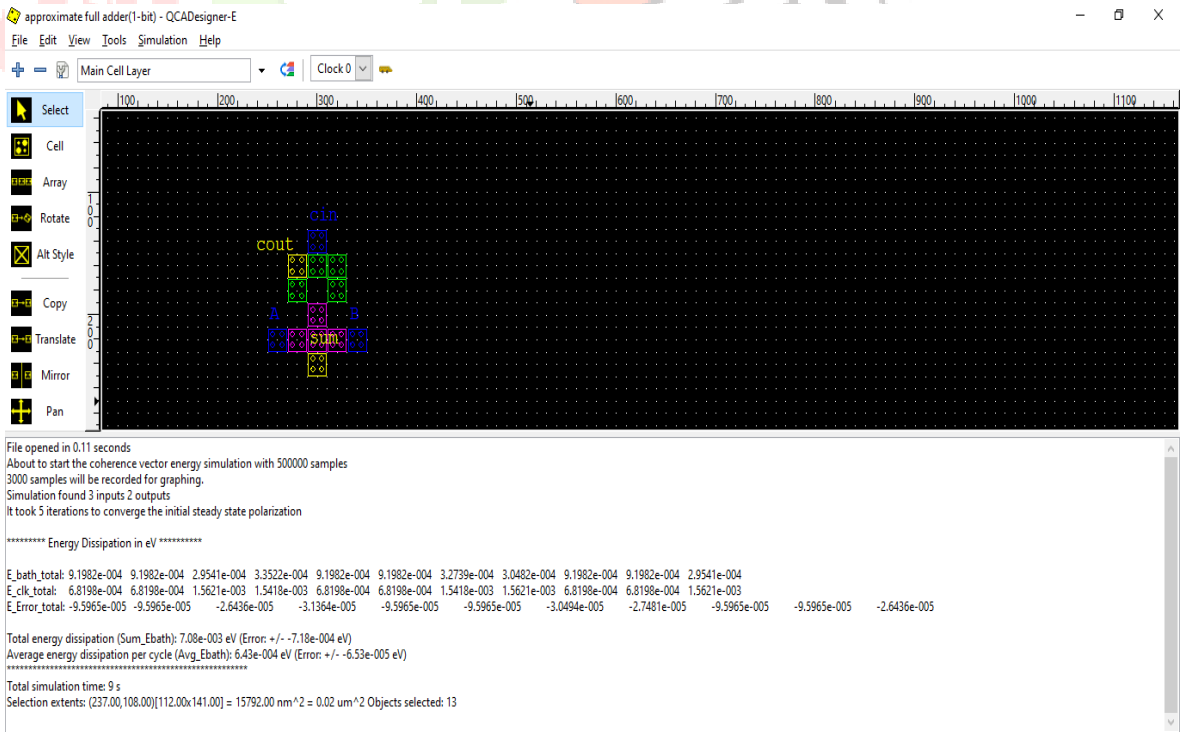

Figure.16: Approximate full adder circuit-2 simulation result in QCAD-E

Table.5: Approximate full adder circuit-2 simulation result values

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_E bath)	Average energy dissipation (Avg_E bath)	Total simulation time	Selection extends	Objects selected
9.1982e-004	6.8198e-004	-9.5965e-005	7.08e-003eV (Error: +/- 7.18-004 eV)	6.43e-004 eV (Error: +/- -6.53e-005 eV)	8 seconds	(237.00, 108.00) [112.00 x 168.00] = 18816.00nm^2 = 0.02um^2	13 cells
9.1982e-004	6.8198e-004	-9.5965e-005					
2.9541e-004	1.5621e-003	-2.6436e-005					
3.3522e-004	1.5418e-003	-3.1364e-005					
9.1982e-004	6.8198e-004	-9.5965e-005					
9.1982e-004	6.8198e-004	-9.5965e-005					
3.2739e-004	1.5418e-003	-3.0494e-005					
3.0482e-004	1.5621e-003	-2.7481e-005					
9.1982e-004	6.8198e-004	-9.5965e-005					
9.1982e-004	6.8198e-004	-9.5965e-005					
2.9541e-004	1.5621e-003	-2.6436e-005					

3.3 Optimized Circuits

Energy Efficient circuits can be built by proper arrangement of quantum cells to get desired functional output. While using QCA wire logic the electrons occur side by side repulsion will be less. In QCA inverter logic the electrons will be occurred diagonally so repulsion will be more.

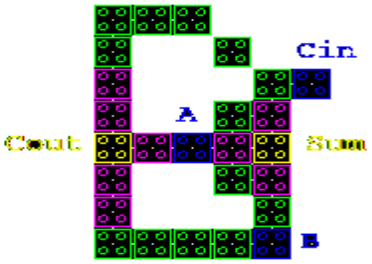

Figure.17: Optimized full adder circuit-1 implementation in QCAD

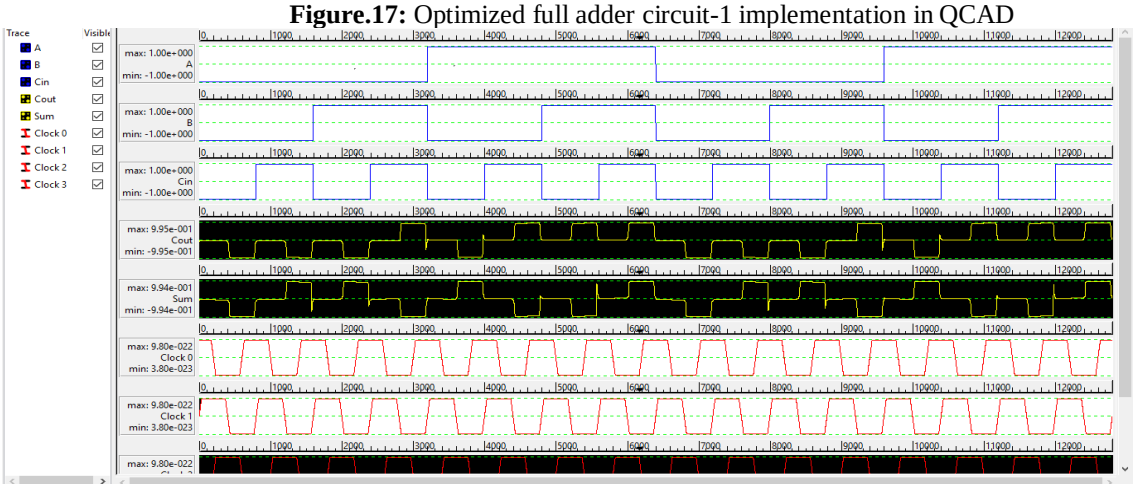

Figure.18: Optimized full adder circuit-1 implementation output in QCAD

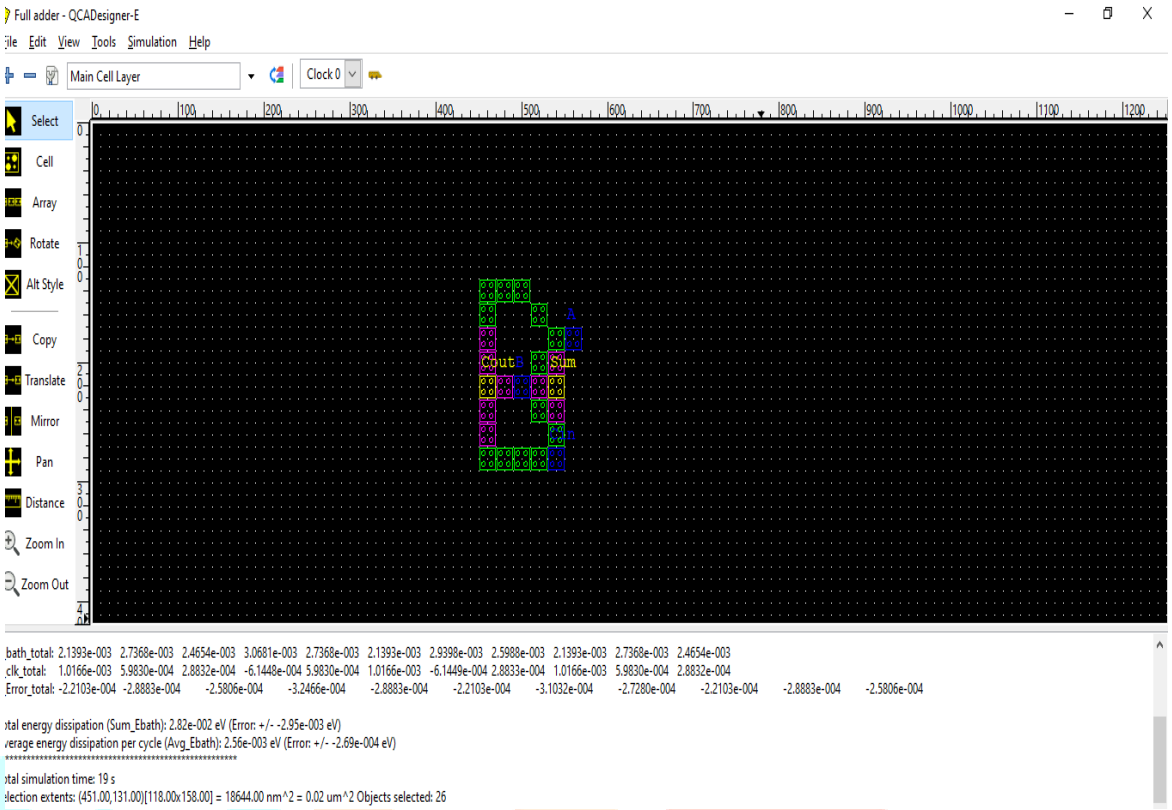

Figure.18: Optimized full adder circuit-1 simulation result in QCAD-E

Table.6: Optimized full adder circuit-1 simulation result values

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_E bath)	Average energy dissipation (Avg_E bath)	Total simulation time	Selection extends	Objects selected
2.1393e-003 2.7368e-003 2.4654e-003 3.0681e-003 2.7368e-003 2.1393e-003 2.9398e-003 2.5988e-003 2.1393e-003 2.7368e-003 2.4654e-003	1.0166e-003 5.9830e-004 2.8832e-004 -6.1448e-004 5.9830e-004 1.0166e-003 -6.1449e-004 2.8833e-003 1.0166e-003 5.9830e-004 2.8832e-004	-2.2013e-004 -2.8883e-004 -2.5806e-004 -3.2466e-004 -2.8883e-004 -2.2103e-004 -3.1032e-004 -2.7280e-004 -2.2103e-004 -2.8883e-004 -2.5806e-004	2.82e-002eV (Error: +/- 2.56-003 eV)	2.56e-003 eV (Error: +/- -2.69e-004 eV)	19 seconds	(451.00, 131.00) [118.00 x 158.00] = 18644.00nm^2 = 0.02um^2	26 cells

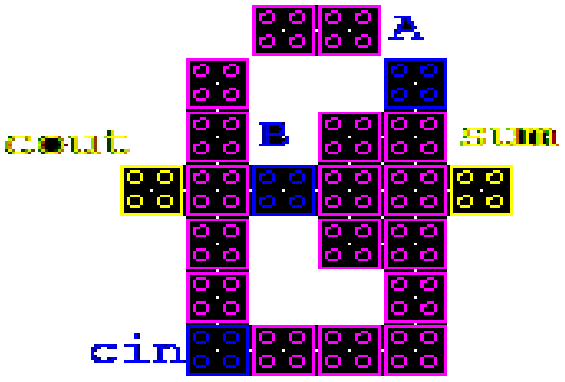

Figure.19: Optimized full adder circuit-2 implementation in QCAD

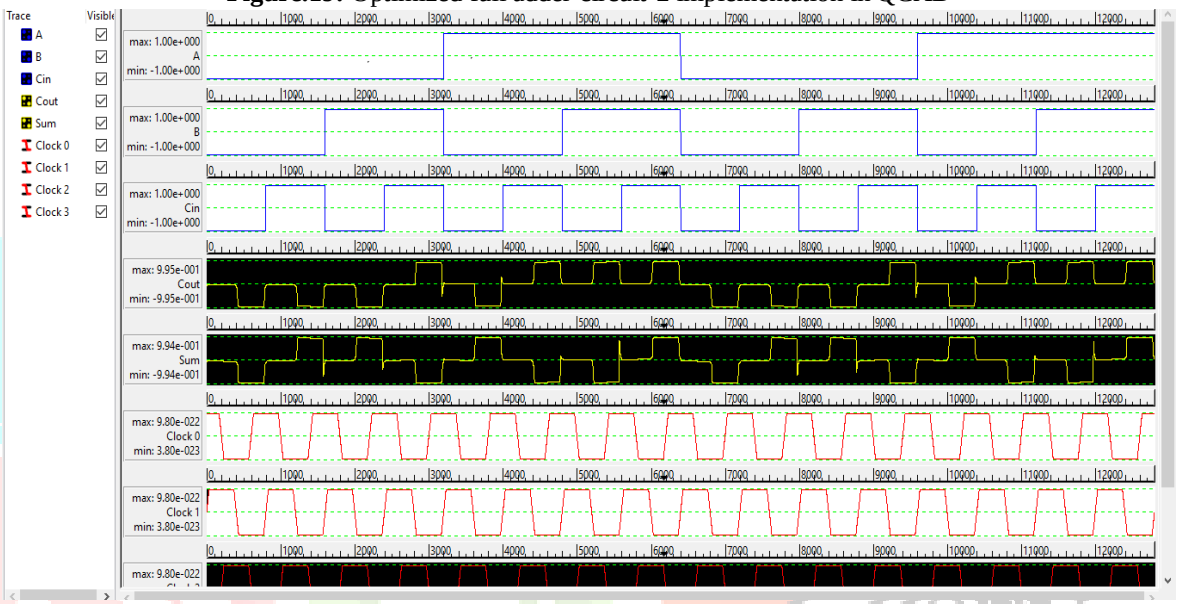

Figure.20: Optimized full adder circuit-2 implementation in QCAD

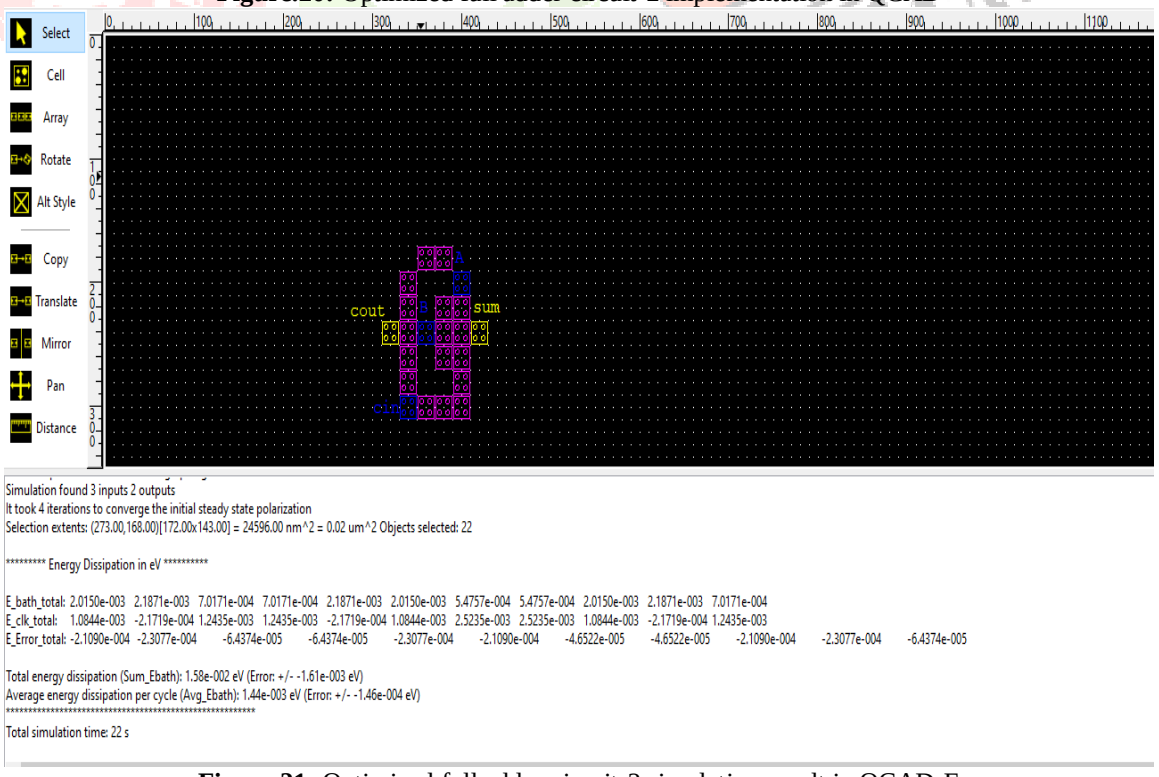

Figure.21: Optimized full adder circuit-2 simulation result in QCAD-E

Table 7: Optimized full adder circuit-2 simulation result values

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_E bath)	Average energy dissipation (Avg_E bath)	Total simulation time	Selection extends	Objects selected
2.0150e-003 2.1871e-003 7.0171e-004 7.0171e-004 2.1871e-003 2.0150e-003 5.4757e-004 5.4757e-004 2.0150e-003 2.1871e-003 7.0171e-004	1.0644e-003 -2.1719e-004 1.2435e-003 1.2435e-003 -2.1719e-004 1.0844e-003 2.5235e-003 2.5235e-003 1.0844e-003 -2.1719e-004 1.2435e-003	-2.1090e-004 -2.3077e-004 -6.4374e-005 -6.4374e-005 -2.3077e-004 -2.1086e-004 -4.6522e-005 -4.6522e-005 -2.1090e-004 -2.3077e-004 -6.4374e-005	1.59e-002eV (Error: +/- 1.61-003 eV)	1.44e-003 eV (Error: +/- -1.46e-004 eV)	22 seconds	(451.00, 131.00) [118.00 x 158.00] = 18644.00nm^2 = 0.02um^2	22 cells

IV. MULTIPLEXER IN QCA

4.1 Conventional multiplexer

Multiplexing is the generic term used to describe the operation of sending one (or) more analog or digital signals over a common transmission line at different times or speeds and as such, the device we use to do just that is called the multiplexer [12].

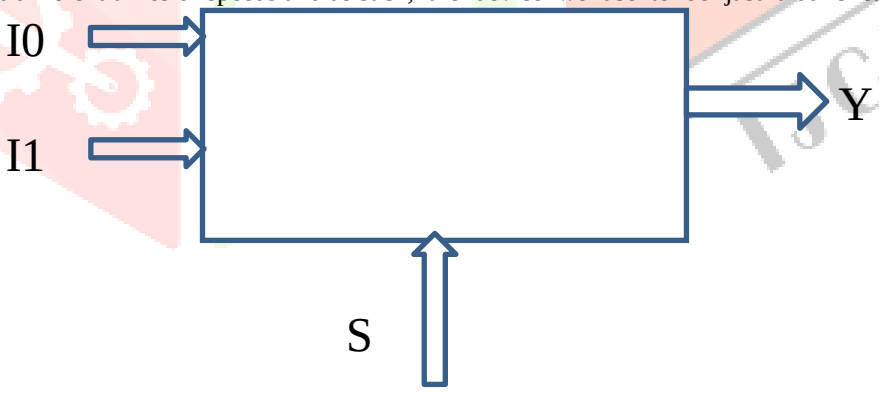

Figure.22: Block diagram of Multiplexer

Figure 23. logic diagram of full adder. we connected two and gate logic, or gate logic, not gate logic. We have three inputs (I0, I1,S), and one output (C_{out}).

$$Y = I_0\bar{s} + I_1 s \quad \text{..... (2)}$$

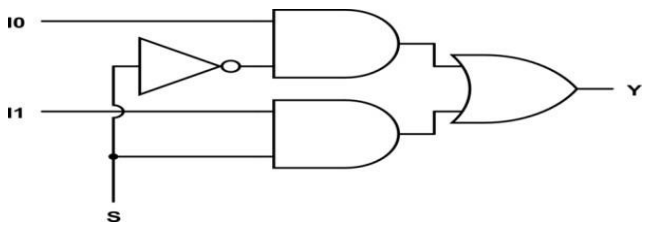

Figure.23: Logic diagram of Multiplexer

'S' and 'I0' and 'I1' are the input variables. These variables represent the two significant bits that are going to combinations of '0'or '1'.'Y' are the output variable. These variables represent the two significant bits that are going to combinations of '0' or '1'.

Table.8: Truth table of multiplexer

Input			Output
S	I0	I1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Simulation results of Multiplexer

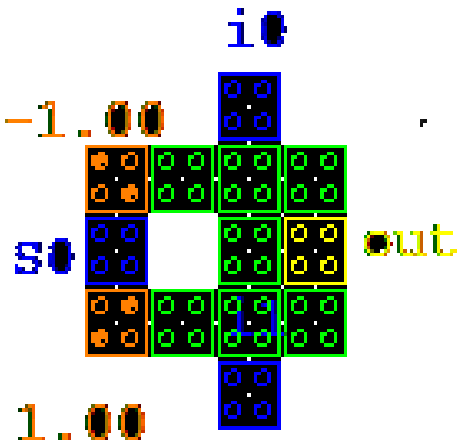

Figure.28: Multiplexer implementation in QCAD

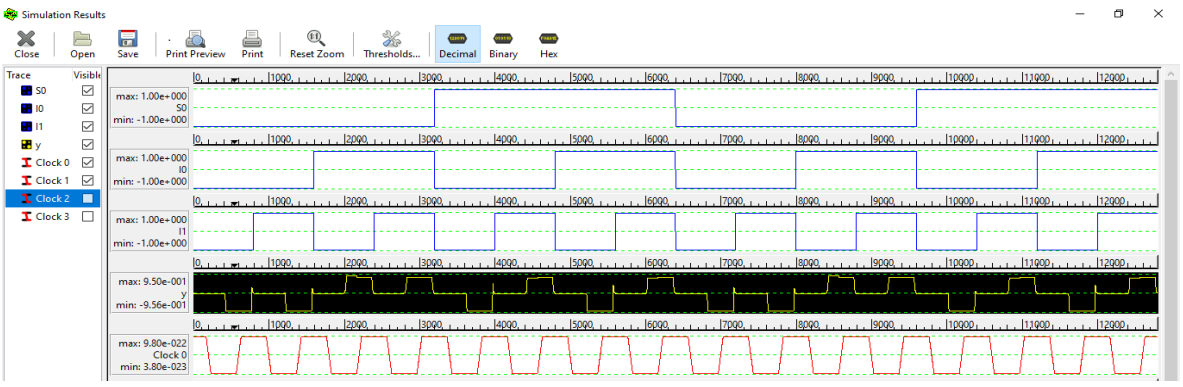

Figure.29: Multiplexer implementation output in QCAD

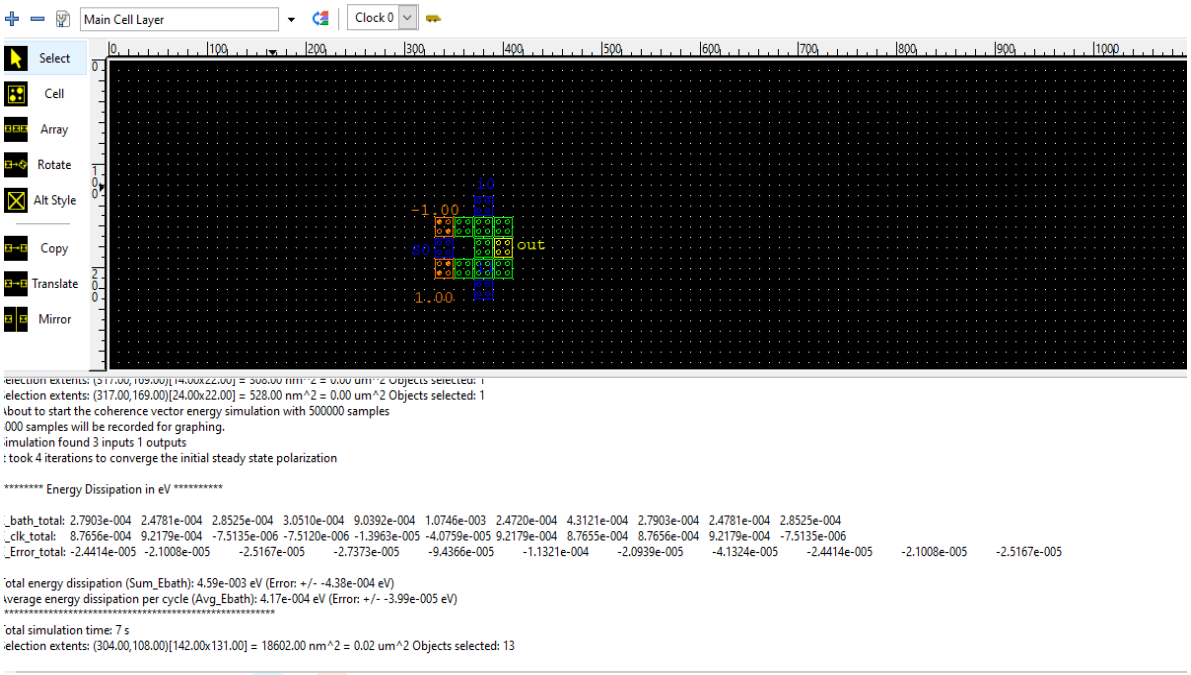

Figure.30: Multiplexer simulation result in QCAD-E

Table.9: Multiplexer simulation result values

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_E bath)	Average energy dissipation (Avg_E bath)	Total simulation time	Selection extends	Objects selected
2.7903e-004	8.7656e-004	-2.4414e-005	4.59e-003eV (Error: +/- 4.38e-004 eV)	4.17e-004 eV (Error: +/- 3.99e-005 eV)	7 seconds	(237.00, 108.00) [112.00 x 168.00] = 18816.00nm^2 = 0.02um^2	13 cells
2.4781e-004	9.2179e-004	-2.1008e-005					
2.8525e-004	-7.5135e-006	-2.5167e-005					
3.0510e-004	-7.5135e-006	-2.7373e-005					
9.0392e-004	-1.3963e-005	-9.4366e-005					
1.0746e-004	-4.0759e-005	-1.1321e-004					
2.4720e-004	9.2179e-004	2.0939e-005					
4.3121e-004	8.7655e-004	-4.1324e-005					
2.7903e-004	8.7656e-004	-2.4414e-005					
2.4781e-004	9.2179e-004	-2.1008e-005					
2.8525e-004	7.5135e-006	-2.5167e-005					

4.2 Optimized Multiplexers

By strategically placing quantum cells, it is possible to create circuits that are both functionally and energy-efficient. The electrons' repulsion will be smaller when they are side by side when employing QCA wire logic. The electrons will be arranged diagonally in QCA inverter logic, increasing the amount of repulsion.

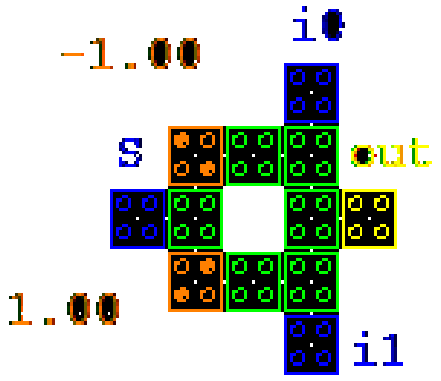

Figure.31: Optimized Multiplexer circuit-1 implementation in QCAD

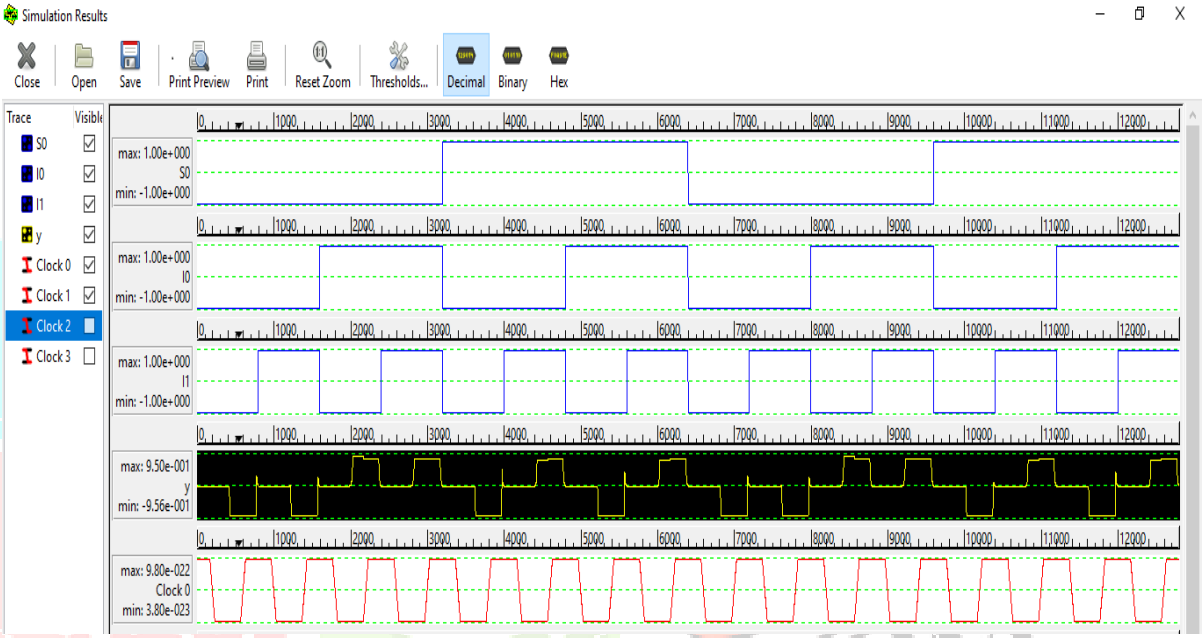

Figure.32: Optimized Multiplexer circuit-1 implementation output in QCAD

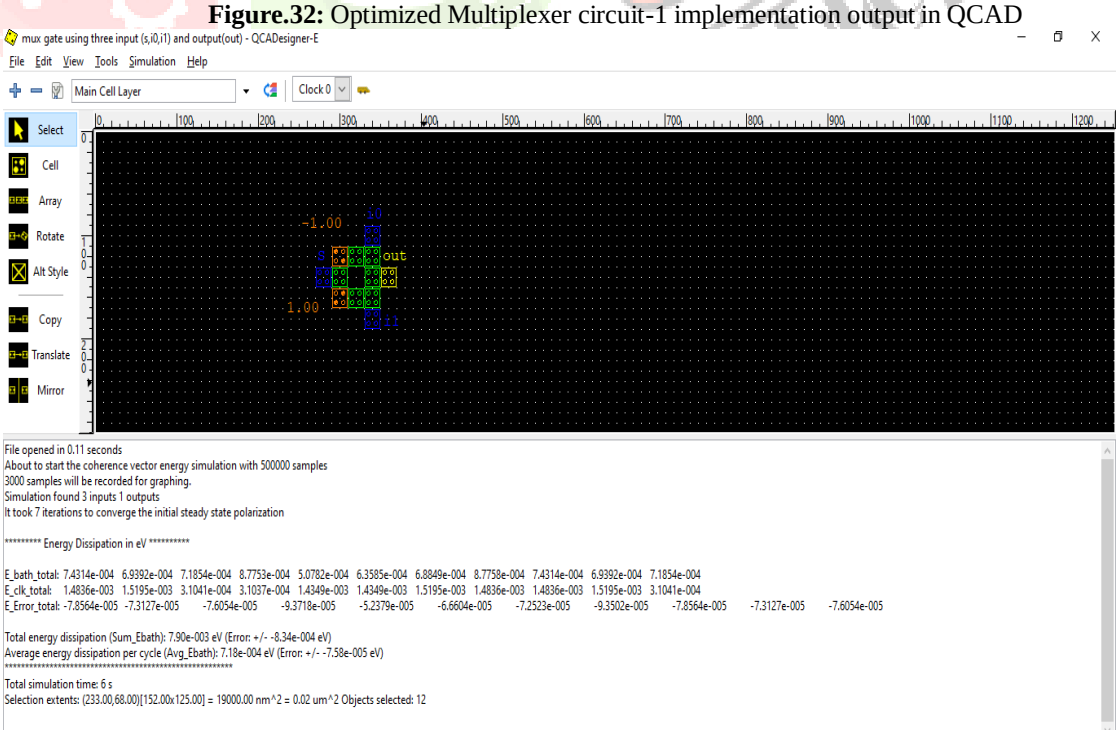

Figure.33: Optimized Multiplexer circuit-1 simulation result in QCAD-E

Table.10: Optimized Multiplexer circuit-1 simulation result values

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_E bath)	Average energy dissipation (Avg_E bath)	Total simulation time	Selection extends	Objects selected
7.4314e-004 6.9392e-004 7.1854e-004 8.7758e-004 5.0782e-004 6.1985e-004 6.8849e-004 8.7758e-004 7.4334e-004 6.9092e-004 71854e-004	1.4836e-004 3.5195e-003 3.3041e-004 3.5087e-004 1.4349e-003 1.4349e-003 1.5195e-003 1.4836e-003 1.4836e-003 1.5195e-003 3.1041e-004	-7.8564e-005 -7.3127e-005 -7.6054e-005 -9.3718e-005 -5.2379e-005 -6.6604e-004 -7.2523e-005 -9.3502e-005 -7.8564e-005 -7.3127e-005 -7.6054e-005	7.90e-003eV (Error: +/- 8.34e-004 eV)	7.18e-004 eV (Error: +/- 7.58e-005 eV)	6 seconds	(233.00, 66.00) [152.00 x 125.00] = 19000.00nm^2 = 0.02um^2	12 cells

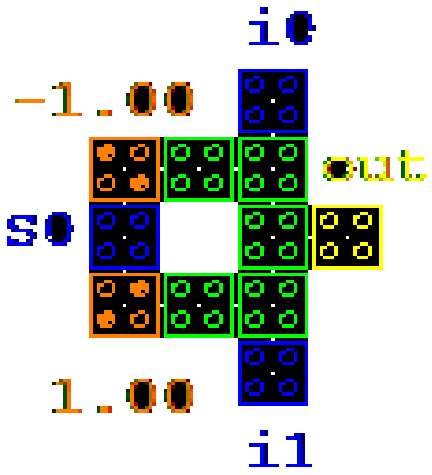

Figure.34: Optimized Multiplexer circuit-2 implementation in QCAD

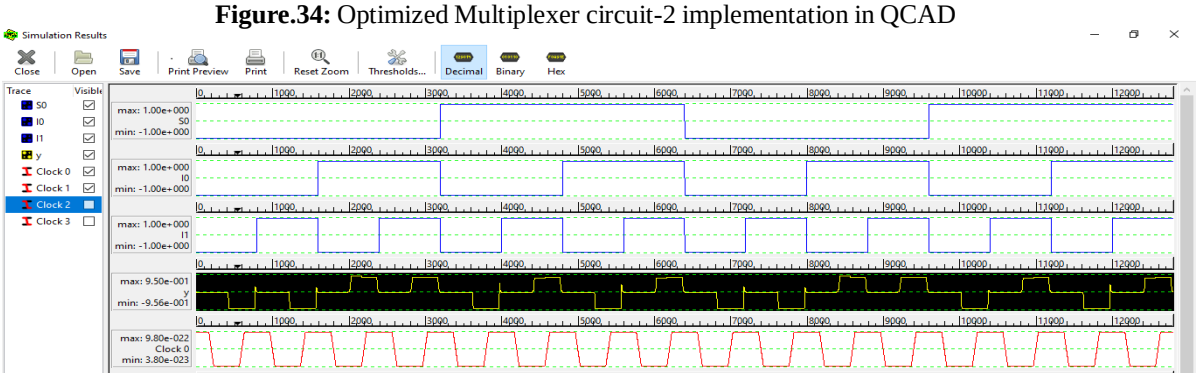

Figure.35: Optimized Multiplexer circuit-2 implementation output in QCAD

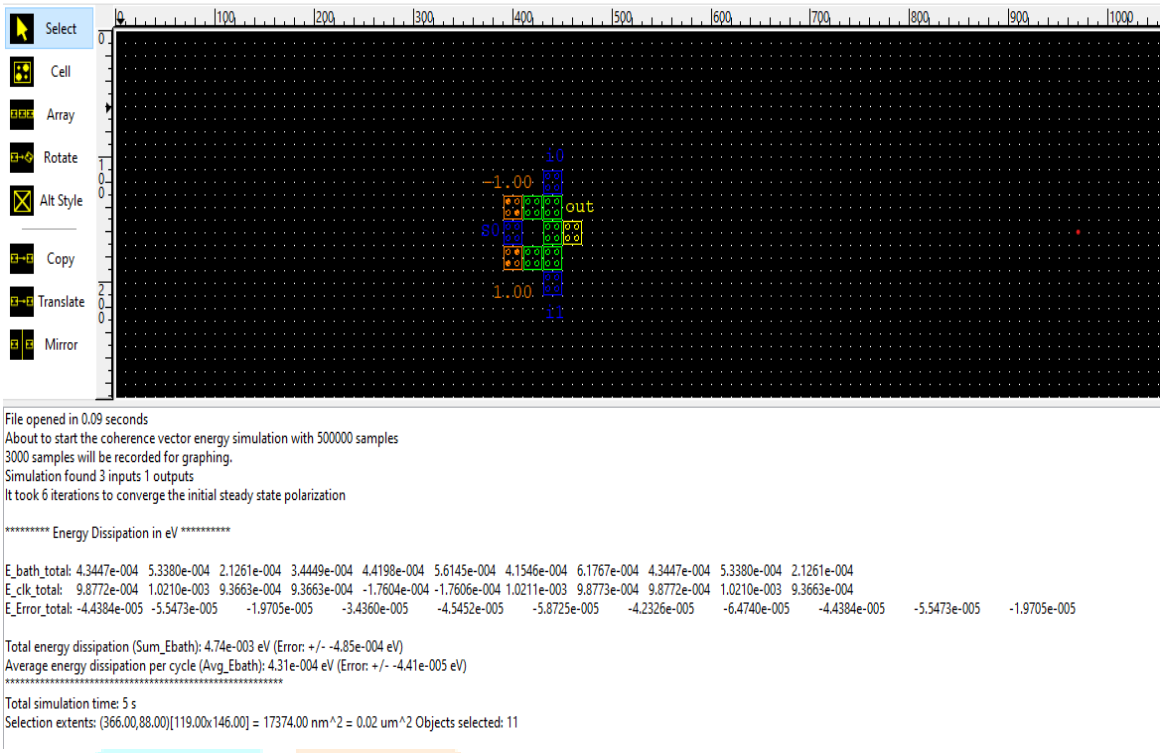

Figure.36: Optimized Multiplexer circuit-2 simulation result in QCAD-E

Table.11: Optimized Multiplexer circuit-2 simulation result values

E_bath_total	E_clk_total	E_error total	Total energy dissipation (Sum_E bath)	Average energy dissipation (Avg_E bath)	Total simulation time	Selection extends	Objects selected
4.3447e-004 5.3380e-004 2.1261e-004 3.4449e-004 4.4198e-004 5.6145e-004 4.1546e-004 6.1767e-004 4.3447e-004 5.3390e-004 2.1261e-004	9.8772e-004 1.0210e-003 9.3663e-004 9.3663e-004 -1.7604e-004 -1.7604e-004 1.0211e-003 9.8773e-003 9.8772e-003 1.0210e-003 9..3663e-004	-4.4384e-005 -5.5479e-005 -1.9705e-005 -3.4360e-005 -4.5452e-005 -5.8725e-005 -4.2326e-005 -6.4740e-005 -4.4384e-005 -5.5473e-005 -1.9705e-005	4.74e-003eV (Error: +/- 4.85e-004 eV)	4.31e-004 eV (Error: +/- 4.41e-005 eV)	5 seconds	(366.00, 88.00) [119.00 x 146.00] = 17374.00nm^2 = 0.02um^2	11 cells

V. Comparison table

Table.12: Comparison table between Full adder and Approximate full adder

Full adder circuit with logic gates	**Approximate full adder circuit-1 with majority gate function**	**Approximate full adder circuit-2 with majority gate function**
No of cells:28	No of cells:14	No of cells:13
Total energy dissipation: 2.19e-002eV	Total energy dissipation: 9.32e-003eV	Total energy dissipation: 7.08e-003eV
Average energy dissipation: 1.99e-003eV	Average energy dissipation: 8.48e-003eV	Average energy dissipation: 6.43e-003eV
Area occupancy: 28512.00 nm^2	Area occupancy: 22632.00 nm^2	Area occupancy: 15792.00 nm^2
Total simulation:28 seconds	Total simulation:26 seconds	Total simulation:22 seconds

Table.13: Comparison table between Full adder and Optimized full adder

Full adder circuit with logic gates	**Optimized full adder circuit-1 without gates**	**Optimized full adder circuit-2 without gates**
No of cells:28	No of cells:26	No of cells:22
Total energy dissipation: 2.19e-002eV	Total energy dissipation: 2.82e-002eV	Total energy dissipation: 1.58e-002eV
Average energy dissipation: 1.99e-003eV	Average energy dissipation: 2.56e-003eV	Average energy dissipation: 1.44e-003eV
Area occupancy: 28512.00 nm^2	Area occupancy: 18644.00 nm^2	Area occupancy: 24596.00 nm^2
Total simulation:28 seconds	Total simulation:26 seconds	Total simulation:22 seconds

Table.14: Comparison table between Multiplexer and Optimized multiplexer

Multiplexer circuit with logic gates	**Optimized multiplexer circuit-1 without gates**	**Optimized multiplexer circuit-2 without gates**
No of cells:13	No of cells:12	No of cells:11
Total energy dissipation: 4.59e-003eV	Total energy dissipation: 7.90e-003eV	Total energy dissipation: 4.74e-003eV
Average energy dissipation: 4.17e-004eV	Average energy dissipation: 7.18e-004eV	Average energy dissipation: 4.37e-004eV
Area occupancy: 18602.00 nm^2	Area occupancy: 19000.00 nm^2	Area occupancy: 17374.00 nm^2
Total simulation:9 seconds	Total simulation:6 seconds	Total simulation:5 seconds

CONCLUSION

When compared to other conventional full adder circuit types, the optimized full adder circuit-1 with different patterns of placing QCA cells has used less no of cells, area occupancy values have been reduced. Optimized full adder circuit-2 has less no of cells, total energy dissipation, average energy dissipation.

Two different types of approximation adders are designed in this thesis (majority gate-based approximate full adder). When compared to the actual full adder, the suggested majority gate-based approximation adder exhibits dramatic reductions in terms ofpower consumption, cell count and timing, and delay.

1) The first existing approximate full adder has a different technique in two cases they are case (a):000 and case (b):111. In these two cases, the output values of sum(s) and carry out (C_{out}) values will be changed. Here error metrics can also be used.

2) The second existing approximate full adder has different techniques in two cases they are case (a):001 and case (b): 110. In

these two cases the output values of sum(s) and carry out (C_{out}) values will be changed. Here error metrics can also be used.

Approximate full adder circuit-1 are used to reduce No of cells, Area occupancy. Approximate full adder circuit-2 is used to reduce no of cells, total energy dissipation, average energy dissipation, area occupancy.

When compared to other conventional multiplexers circuits the optimized multiplexer circuit-1 has less No of cells.

Optimized multiplexer circuit-2 has reduces no of cells, area occupancy.

FUTURE SCOPE

The future scope is to design the Multi bit layer circuits and Arithmetic logic unit (ALU) circuits.

REFERENCES

1. Aproov Khurasia, Pulkit Gambhir, "Quantum Cellular Automata", May 2006
2. Bilal, Bisma, Suhaib, Ahmed, Vipan Kakkar, "Quantum Dot Cellular Automata: A New Paradigm for Digital Design",International Journal of Nano Electronics and Materials, vol.11, no.1, pp.87-98, Jan 2018.
3. Kavitha S.S., Kaulgud N., "Quantum Dot Cellular Automata: Design for the Realization of Basic Logic Gates", International Conference on Electrical, Electronics, Communication, Computer and Optimization Techniques, pp.314-317, Dec 2017.
4. Abdullah M.D., Shariful M.D., Ali Newaz, "Five Input Majority Gate Based Optimized Full Adder", International Nano Letters, vol.10, no.3, pp.177-195, Sep 2020.
5. Mehta, Usha, Vaishali Dhare, "Quantum dot cellular Automata: A Survey", Arxiv preprint: 1711.08153, Nov 2017.
6. Pareek, Vishal, "A New Gate for Optimal Fault Tolerant and Testable Reversible Sequential Circuit Design", Arxiv preprint: 1410.2373, Oct 2014.
7. Ganesh E.N., "Power Analysis of Quantum Cellular Automata Circuits", Procedia Materials Science, vol.10, pp.381-384, Jan 2015.
8. Amrutha M., Kavitha K.R., "Hardware Security Based Quantum Dot Cellular Automata Circuit Design Review and Outlook", Annuals of the Romanian Society for Cell Biology, pp.1934-1939, Sep 2021.
9. Safavi A., Moslesh M., "An Overview of Full Adders in QCA Technology", International Journal of Computer Science and Network Solutions, vol.1, no.4, pp.12-35, Jan 2013.
10. Zhang, Tingting, Weiqiang Liu, Emma Mclamon, Maire O'neli, Farizio Lombardi, "Design of Majority Logic (ML) Based Approximate Full Adders", IEEE International Symposium on Circuits and Systems (ISCAS), vol.4, pp.1-5, May 2017.
11. Gupta, Vaibhav, Mohapatra, Raghunathan, Roy, "Low Power Digital Signal Processing Using Approximate Adders," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.32, no.1, pp.124-137, Dec 2012.
12. Ahmad, Firdous, "An Optimal Design of QCA Based 2n:1/1:2n Multiplexer/De multiplexer and its Efficient Digital Logic Realization," Microprocessors and Microsystems, vol.56, pp.64-75, Feb 2018.
13. Heikalabad, Saeed Rasouli, Mahya Rahimpour Gadim, "Design of Improved Arithmetic Logic Unit in Quantum Dot Cellular Automata", International Journal of Theoretical Physics, vol.57, no.6, pp.1733-1747, Jun 2018.