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A SEVENTEEN-LEVEL INVERTER FORMED BY CASCADING FLYING CAPACITOR AND FLOATING CAPACITOR H-BRIDGES

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ABSTRACT

A multilayer inverter that can generate 17 distinct voltage levels has recently become available for purchase. This inverter makes use of cascaded Hbridge modules that have floating capacitors and a three-level flying capacitor inverter. In this study, a number of aspects of the inverter that has been suggested are described. One of these aspects is the inverter's capacity to maintain a voltage balance across its capacitors. The findings of the experiments are used to investigate the efficiency of the suggested converter. The algorithm that is used to balance capacitors has been evaluated to ensure that it is stable in both transient and steady-state situations. Instantaneous balancing of all of the capacitors in this circuit is possible by utilising any one of the pole voltage combination options. This architecture has a number of advantages, one of which is that it makes it possible to operate the converter in back-to-back mode, with all of the voltages being generated by a single DC link power supply. The inverter that is now being demonstrated has the capacity to support a full range of load power factors in addition to modulation indices. Even if one of the H-bridges fails, the inverter can still be used at full load; the only difference is that it will be able to produce a lower total number of levels. In this setup, both the dv/dt and the common mode voltage variation are rather little. This is because both of these measures are dependent on time.

1. INTRODUCTION

Changes in medium and high voltage drive performance have been dramatic since the introduction of multilevel inverters [1]- [3]. According to [4] and [5], as the number of voltage levels increases, the performance of the drive sees a significant improvement. [Citation needed] The reason for this is that as the number of voltage levels grows, the output voltage begins to more closely resemble a sine wave and contains less harmonic content. Neutral point clamped inverters [6] were an early breakthrough that was introduced within the field of multilayer inverters. Alternately, [7] described a method whereby multiple isolated DC sources were used in conjunction with H-bridges to generate a wide range of voltages for the purpose of plasma stabilisation. The problems associated with the cascading multiple rectifiers scheme are examined in [8], along with a proposed solution for capacitor balancing. The investigation that is detailed in reference [9] demonstrates how many different voltage levels can be generated by adjusting the load current that is being carried via capacitors at the same time. By switching around the direction in which the load current travels through the capacitor and selecting redundant states for the same pole voltage, it is possible to keep the voltage across the capacitors stable and constant. In other words, the voltage can be held constant. The ideas in [10] are a synthesis of those in [9] and [7]. Here, H-bridges with floating capacitors are used to produce a range of output voltages. Switching between redundant states for the same

voltage level keeps the capacitor voltages where they should be. Cascaded H-bridges are discussed in detail, and a variety of effective control algorithms are proposed, in the published works [11]–[15]. In accordance with the data presented in [16]–[18], modular multilevel converters are yet another variety of multilevel converter that are capable of being utilised in motor driving applications. These converters are typically utilised in high-voltage direct current (HVDC) settings. In [19], the author introduces the idea of a neutral-point clamped inverter that works in tandem with a cascading flying-capacitor inverter. The ABB ACS 2000 commercial version of this idea is available now. Capacitors that are cross-connected in the manner described in [20] can be used to extend the voltage range of an inverter that uses flying capacitors. A unique configuration for generating 17 separate voltage levels from a string of capacitors is described in reference [21], which presents the method. However, the voltages of the capacitors cannot be quickly balanced in [20] and [21]. They will not be in perfect harmony with one another until they reach the fundamental frequency. In reference number 22, a floating load, a single-phase inverter with a total of seventeen levels, and a significant number of power supplies are described. As such, it is better suited for use in STATCOM contexts. In [23], a compelling algorithm for controlling an inverter with seventeen levels is described.

We propose a brand new 17-level inverter that derives all of its power from a single DC source. This inverter would be constructed using cascading 3-level flying capacitor inverters with H-bridges that use floating capacitors. The findings of the experiments that were done to validate the steady-state and transient performances of the suggested configuration are presented here after those experiments were carried out.

2. LITERATURE REVIEW

An inverter is a form of power electronic equipment that can change direct current (dc) power into alternating current (ac) power at the output voltage and frequency that the user specifies. Direct current (dc) electricity is also known as battery power. Inverters that create a voltage or current at the output with two distinct levels of +or-V are referred to as 2 level inverters. "2 level" is the name given to certain types of inverters. This two-level conventional inverter operates at a high switching frequency, which causes significant switching losses and places rating constraints on its ability to serve applications that require high power and voltage. Additional obstacles for it include harmonic distortion, electromagnetic interference (EMI), and high dv/dt stress. Another problem is that there is an excessively high level of overall harmonic distortion. As a result of these issues, it is challenging to interface power electronic switches directly to high and medium voltage grids. At this point in time, it is abundantly evident that a different architecture for the multi-level inverter is required [1].

There has been a reduction in both electromagnetic interference (EMI) and core losses, while at the same time there has been a rise in the efficiency of solar applications with multilevel topologies. Both of these are areas that have seen improvements in recent times. However, research efforts are expanding to low-voltage applications in order to take use of the benefits that were previously emphasised. The multi-level converter has been used mostly in renewable energy systems that utilise high voltages of more than kV. A photovoltaic (PV) generation system with the cascaded H-bridge multilevel inverter architecture has been explored, which is just one of the many research that have been conducted. This is because isolated direct current (DC) sources can be naturally obtained from photovoltaic (PV) arrays, and in comparison to other multilevel converters, they can be simply modularized. Another reason for this is that DC sources can be produced from PV arrays. Reference presented a study on the reactive power compensation for the single-phase grid-connected cascaded H-bridge multilevel inverter; however, they did not fully describe the approach for designing the controller [2].

The three basic categories of multi-level inverters are called diode clamped multi-level inverters, flying capacitor inverter multi-level inverters, and cascaded multi-level inverters. When compared to other varieties of multilevel inverters, the cascaded multilevel control method is a lot easier to understand and use. This is owing to the fact that it does not require the use of a clamping diode or flying capacitor in order for it to function properly. The control method of multilevel inverters typically makes use of one of two major PWM approaches. [Case in point:] [Case in point:] The first one is called the fundamental switching frequency, while the second one is called the high switching frequency. Both of these terms refer to the frequency at which the switch is made. For high switching frequencies, the classifications PWM with space vectors, PWM with selective harmonic removal, and SPWM are utilised [3]. Switched control has recently attracted a lot of attention since it can be easily applied, particularly in the field of power converters.

3. POWER CIRCUIT TOPOLOGY

The converter that has been suggested is an illustration of a hybrid multilevel topology. It makes use of a three-level flying capacitor inverter in conjunction with three cascade floating capacitor H-bridges. A graphical representation of a power supply that operates in three phases. In this configuration, capacitors AC1, BC1, and CC1 all have their voltages held at Vdc/2. The voltage across capacitors AC2, BC2, and CC2 is held constant at Vdc/4. The voltage across capacitors AC3, BC3, and CC3 is kept at 8 volts direct current (Vdc), while the voltage across capacitors AC4, BC4, and CC4 is kept at 16 volts direct current (Vdc). Each subsequent H-bridge in the cascade can either add to or subtract from the voltage produced by the stage before it. The CHBs can also be avoided. When all of the stages' voltages are added together, we get the voltage at the inverter's poles. Figure 1, which is a schematic, illustrates a diagram of a single phase of the proposed converter. When there is sufficient dead time, the complimentary switch pairs (AS1, AS1'), (AS2, AS2'), (AS3, AS3'), (AS4, AS4'), (AS5, AS5'), (AS6, AS6'), (AS7, AS7'), and (AS8, AS8') are toggled. Each switch pair can be in one of two logic states: either 1 (indicating that the device on top is active) or 0 (indicating that the device on the bottom is active) (denoted by 0).

As a direct consequence of this, there are 256 (28), distinct combinations of the switches that are feasible. One or more switching states can be used to produce any desired voltage (pole voltage redundancies). By inverting the direction of the current that is flowing through a capacitor and repeatedly cycling through the various redundant switching combinations, the voltage of the capacitor can be set to the desired level (for the same pole voltage). This approach has been seen to quickly balance capacitor voltages across all load currents and power factors for voltages spanning 17 poles. This is true regardless of the load current. They are 0 Vdc, 16 Vdc, 8 Vdc, 3 Vdc, 16 Vdc, 4 Vdc, 5 Vdc, 16 Vdc, 3 Vdc, 16 Vdc, 2 Vdc, 9 Vdc, 5 Vdc, 8 Vdc, 11 Vdc, 3 Vdc, 4 Vdc, 13 Vdc, 7 Vdc, 16 Vdc, and 15 Vdc. However, by cycling through all of the different switching combinations that are feasible for the pole voltage, the suggested topology is able to generate 31 distinct pole voltage levels. Only within a primary cycle can the voltages of capacitors over the subsequent 14 levels be brought into balance. One of the 82 possible switching combinations can be used to provide the 17-pole voltage levels that were previously described, which make it possible to achieve instantaneous capacitor voltage balancing (Table. I). The results that were obtained from 82 different switch designs are presented in Table I. These results concern the charge state (charge or discharge) of each capacitor when the current was flowing in the positive direction (i.e. when the pole is sourcing current, as indicated in Fig. 2). When the current flows in the opposite direction, which is negative, the capacitor will be charged rather than discharged because this is the case when the current is moving in the opposite way. For example, if the controller requires a pole voltage of Vdc/16, there are five distinct switching configurations that can be used to achieve that voltage level. These configurations can be selected from the available options. The myriad of different switching configurations that are available each bring their own unique set of changes to the capacitors' charge states. When the switching state (0,0,0,0,0,1) from Table I is applied, the capacitor C4 will discharge

It is evident that the voltages on all of the capacitors can be kept at their designated levels while cycling through the various pole voltage combination redundancies in order to generate a pole voltage of Vdc/16 for the positive direction of current. This can be accomplished without affecting the voltages on any of the capacitors. Cycling through the various pole voltage combination redundancies is one way to achieve this goal. If it is necessary to empty all of the capacitors, then C4 is emptied first, and then the other capacitors can be emptied during subsequent switching cycles while C4 is being charged. If it is not necessary to empty all of the capacitors, then C4 is charged while the other capacitors are being emptied. In the event that it is essential to discharge each of the capacitors, C4 is discharged first. When the current is flowing in the other direction, the effect that the voltages have on the capacitor is altered such that it has an effect that is opposite of what it had before. Figure 4 provides a visual representation of the full process of balancing the voltage of the capacitor for the Vdc/16 pole voltage. In this particular illustration, the current is moving in a positive direction, and we demonstrate how the voltage on the capacitor adjusts in response to the application of various redundant states to it. Vdc/16 is the voltage that is specified for the pole. Equalizing the capacitor voltages for the other pole voltages, such as Vdc/8, 3Vdc/16, Vdc/4, 5Vdc/16, 3Vdc/8, 7Vdc/16, Vdc/2, 9Vdc/16, 5Vdc/8, 11Vdc/16, 3Vdc/4, 13Vdc/16, 7Vdc/8, 15Vdc/16, and Vdc, can be performed with a method that is comparable to V It is important to note that the maximum switching frequency of each CHB module and the PWM switching frequency of the converter are identical. This is because the switching state is applied simultaneously with each change in PWM, which is the reason for this phenomenon (the switching state is latched till the next PWM transition). In addition, switching occurs only on the output

capacitors for those capacitors that contribute to the pole voltages. This is the only case in which switching occurs on output capacitors.

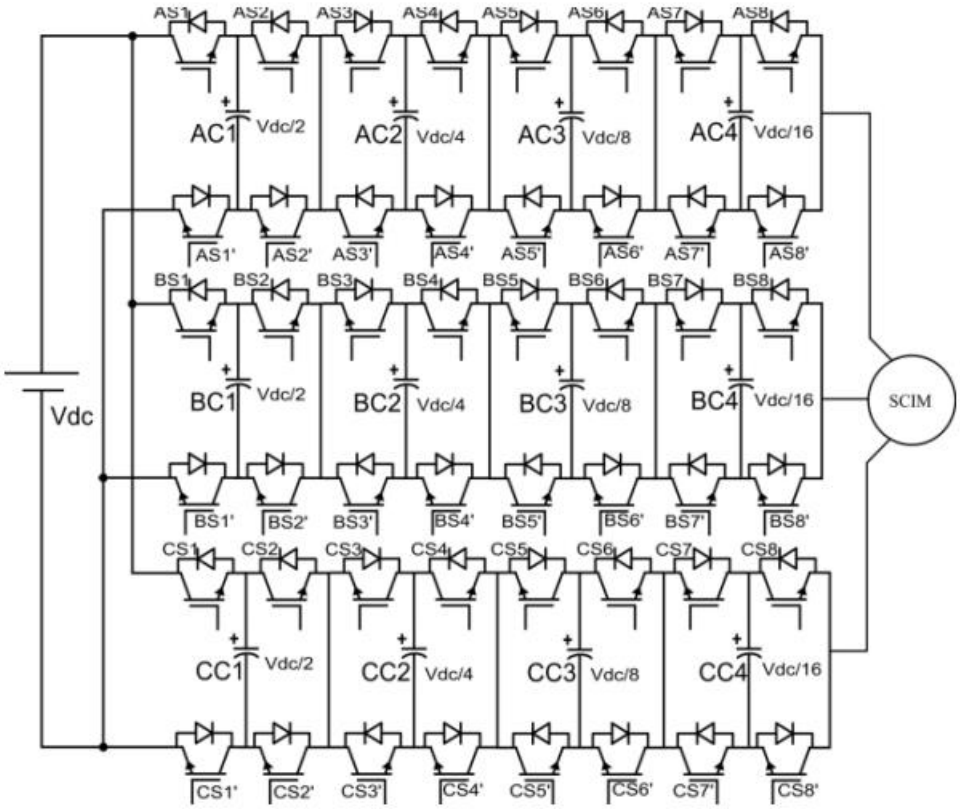


Fig. 1. Cascading three-level flying capacitor inverters with three H-bridges while utilising a single DC connection is how the planned configuration for a seventeen-lever inverter will be built. This arrangement is depicted in the form of a three-phase power schematic.

TABLE I POLE VOLTAGE REDUNDANCIES AND CAPACITOR STATES FOR VARIOUS SWITCHING COMBINATIONS WHEN POLE SOURCES CURRENT

S.No	Pole Voltage	Switch State (S1,S2,S3,S4,S5, S6,S7,S8)	C1 [a]	C2 [a]	C3 [a]	C4 [a]
1	0	(0,0,0,0,0,0,0,0)	0	0	0	0
2	Vdc/16	(0,0,0,0,0,0,0,1)	0	0	0	-
3		(0,0,0,0,0,1,1,0)	0	0	-	+
4		(0,0,0,1,1,0,1,0)	0	-	+	+
5		(0,1,1,0,1,0,1,0)	-	+	+	+
6		(1,0,1,0,1,0,1,0)	+	+	+	+
7	Vdc/8	(0,0,0,0,0,1,0,0)	0	0	-	0
8		(0,0,0,1,1,0,0,0)	0	-	+	0
9		(0,1,1,0,1,0,0,0)	-	+	+	0
10		(1,0,1,0,1,0,0,0)	+	+	+	0
11	3Vdc/16	(0,0,0,0,0,1,0,1)	0	0	-	-
12		(0,0,0,1,0,0,1,0)	0	-	0	+
13		(0,0,0,1,1,0,0,1)	0	-	+	-
14		(0,1,1,0,0,0,1,0)	-	+	0	+
15		(0,1,1,0,1,0,0,1)	-	+	+	-
16		(1,0,1,0,0,0,1,0)	+	+	0	+
17		(1,0,1,0,1,0,0,1)	+	+	+	-
18	Vdc/4	(0,0,0,1,0,0,0,0)	0	-	0	0
19		(0,1,1,0,0,0,0,0)	-	+	0	0
20		(1,0,1,0,0,0,0,0)	+	+	0	0
21	5Vdc/16	(0,0,0,1,0,0,0,1)	0	-	0	-
22		(0,0,0,1,0,1,1,0)	0	-	-	+
23		(0,1,0,0,1,0,1,0)	-	0	+	+
24		(0,1,1,0,0,0,0,1)	-	+	0	-
25		(0,1,1,0,0,1,1,0)	-	+	-	+
26		(1,0,0,0,1,0,1,0)	+	0	+	+
27		(1,0,1,0,0,0,0,1)	+	+	0	-
28		(1,0,1,0,0,1,1,0)	+	+	-	+
29	3 Vdc/8	(0,0,0,1,0,1,0,0)	0	-	-	0
30		(0,1,0,0,1,0,0,0)	-	0	+	0
31		(0,1,1,0,0,1,0,0)	-	+	-	0
32		(1,0,0,0,1,0,0,0)	+	0	+	0
33		(1,0,1,0,0,1,0,0)	+	+	-	0
34	7 Vdc/16	(0,0,0,1,0,1,0,1)	0	-	-	-
35		(0,1,0,0,0,0,1,0)	-	0	0	+
36		(0,1,0,0,1,0,0,1)	-	0	+	-
37		(0,1,1,0,0,1,0,1)	-	+	-	-
38		(1,0,0,0,0,0,1,0)	+	0	0	+
39		(1,0,0,0,1,0,0,1)	+	0	+	-
40		(1,0,1,0,0,1,0,1)	+	+	-	-
41	Vdc/2	(0,1,0,0,0,0,0,0)	-	0	0	0

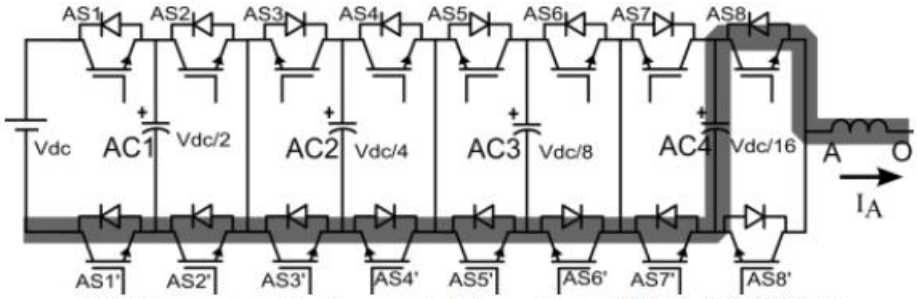
S.No	Pole Voltage	Switch State (S1,S2,S3,S4,S5,S 6,S7,S8)	C1 [a]	C2 [a]	C3 [a]	C4 [a]
42	Vdc/2	(1,0,0,0,0,0,0,0)	+	0	0	0
43	9 Vdc/16	(0,1,0,0,0,0,0,1)	-	0	0	-
44		(0,1,0,0,0,1,1,0)	-	0	-	+
45		(0,1,0,1,1,0,1,0)	-	-	+	+
46		(1,0,0,0,0,0,0,1)	+	0	0	-
47		(1,0,0,0,0,1,1,0)	+	0	-	+
48		(1,0,0,1,1,0,1,0)	+	-	+	+
49		(1,1,1,0,1,0,1,0)	0	+	+	+
50	5 Vdc/8	(0,1,0,0,0,1,0,0)	-	0	-	0
51		(0,1,0,1,1,0,0,0)	-	-	+	0
52		(1,0,0,0,0,1,0,0)	+	0	-	0
53		(1,0,0,1,1,0,0,0)	+	-	+	0
54		(1,1,1,0,1,0,0,0)	0	+	+	0
55	11 Vdc/16	(0,1,0,0,0,1,0,1)	-	0	-	-
56		(0,1,0,1,0,0,1,0)	-	-	0	+
57		(0,1,0,1,1,0,0,1)	-	-	+	-
58		(1,0,0,0,0,1,0,1)	+	0	-	-
59		(1,0,0,1,0,0,1,0)	+	-	0	+
60		(1,0,0,1,1,0,0,1)	+	-	+	-
61		(1,1,1,0,0,0,1,0)	0	+	0	+
62		(1,1,1,0,1,0,0,1)	0	+	+	-
63	3 Vdc/4	(0,1,0,1,0,0,0,0)	-	-	0	0
64		(1,0,0,1,0,0,0,0)	+	-	0	0
65		(1,1,1,0,0,0,0,0)	0	+	0	0
66	13 Vdc/16	(0,1,0,1,0,0,0,1)	-	-	0	-
67		(0,1,0,1,0,1,1,0)	-	-	-	+
68		(1,0,0,1,0,0,0,1)	+	-	0	-
69		(1,0,0,1,0,1,1,0)	+	-	-	+
70		(1,1,0,0,1,0,1,0)	0	0	+	+
71		(1,1,1,0,0,0,0,1)	0	+	0	-
72		(1,1,1,0,0,1,1,0)	0	+	-	+
73	7 Vdc/8	(0,1,0,1,0,1,0,0)	-	-	-	0
74		(1,0,0,1,0,1,0,0)	+	-	-	0
75		(1,1,0,0,1,0,0,0)	0	0	+	0
76		(1,1,1,0,0,1,0,0)	0	+	-	0
77	15 Vdc/16	(0,1,0,1,0,1,0,1)	-	-	-	-
78		(1,0,0,1,0,1,0,1)	+	-	-	-
79		(1,1,0,0,0,0,1,0)	0	0	0	+
80		(1,1,0,0,1,0,0,1)	0	0	+	-
81		(1,1,1,0,0,1,0,1)	0	+	-	-
82	Vdc	(1,1,0,0,0,0,0,0)	0	0	0	0

4. SPACE VECTOR CONTROL REGION

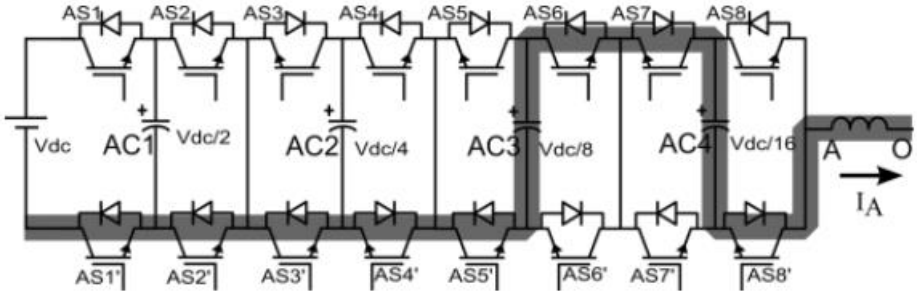
An inverter that operates with three phases is capable of producing any one of 17 different discrete pole voltage levels. These tiers are broken out as follows: 0 Vdc/16, 3 Vdc/8, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. There are 4913 possible permutations of pole voltage for the three-phase inverter that is being suggested. With the equation in hand, a voltage space vector, abbreviated as VSV, is generated for every conceivable combination of voltage at the poles (1).

$$V_{SV} = V_{AN} + V_{BN}\angle 120^{o} + V_{CN}\angle 240^{o} \qquad (1)$$

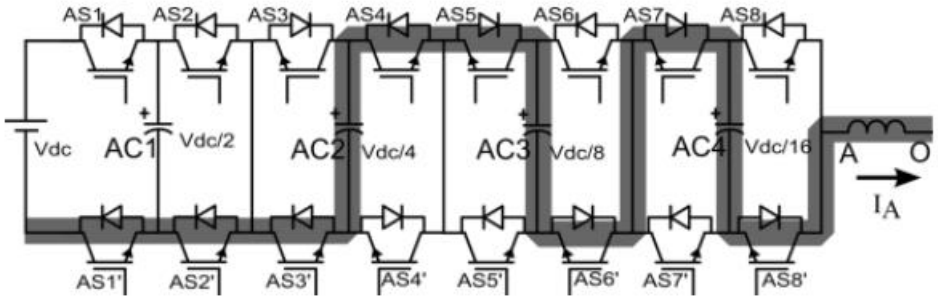
where the three phase voltages are indicated by VAN, VBN, and VCN. When plotted on a space vector plane, these 4193 voltage combinations are dispersed among 817 distinct points. There is the potential for multiple pole voltage combinations (phase voltage redundancy) at each of the 817 space vector locations, each of which can use a unique common mode voltage. In addition, as was mentioned before, the capacitor voltages of any given phase can be balanced by employing any one of multiple redundant switching combinations (pole voltage redundancy). In Fig. 5, we see a representation of the space vector polygon made up of these 817 points. The proposed seventeen-level inverter has a space vector control region comprised of 16 concentric hexagons. Unlike the inner hexagon's space vectors, the outer six have no backup phase voltage sources. As a consequence of this, it is possible to construct the positions on the second largest hexagon by making use of two independent sets of pole voltages that each have their own distinct common mode voltages. Because of this, the sites would become completely unnecessary. As one moves closer to the smaller inner hexagons, the number of pole voltage combinations that are used to produce space vector positions rapidly increases. This is because more combinations are required to build space vector positions. There are sixteen different redundant pole voltage combinations that are conceivable for any common mode voltage.



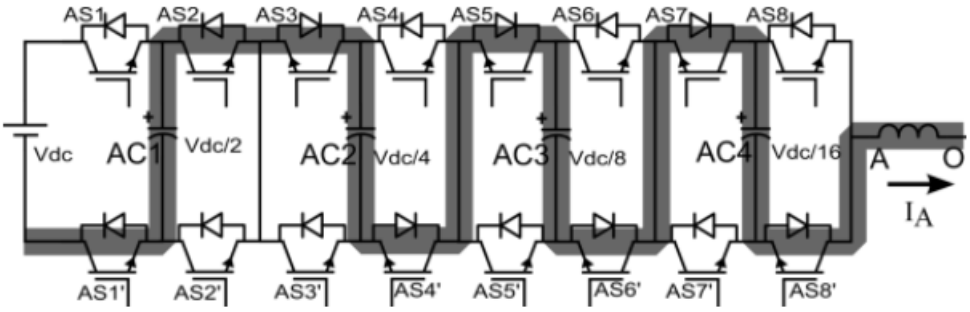
(a) Current path for switching state (0,0,0,0,0,0,0,1)



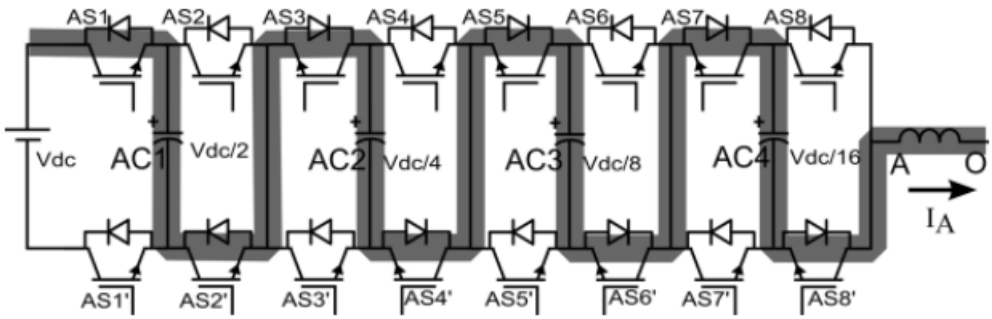
(b)Current path for switching state (0,0,0,0,0,1,1,0)



(c)Current path for switching state (0,0,0,1,1,0,1,0)



(d) Current path for switching state (0,1,1,0,1,0,1,0)



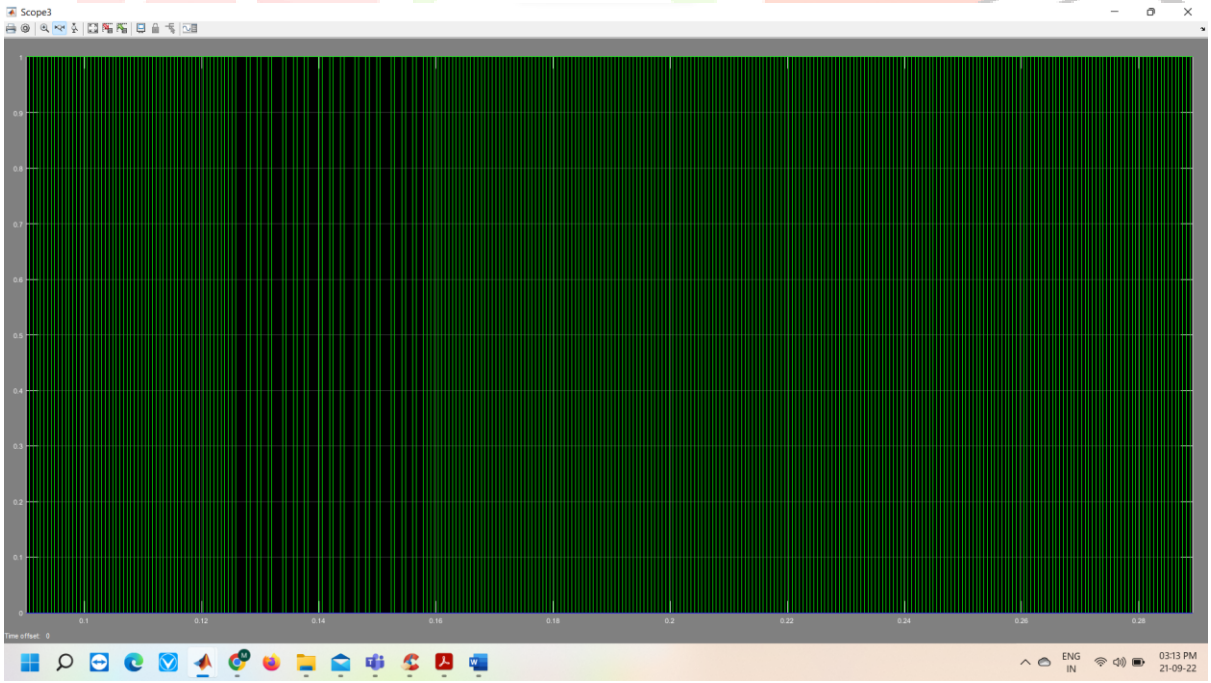
(e)Current path for switching state (1,0,1,0,1,0,1,0)

Fig 2.Switching Redundancies for pole voltage of Vdc/16

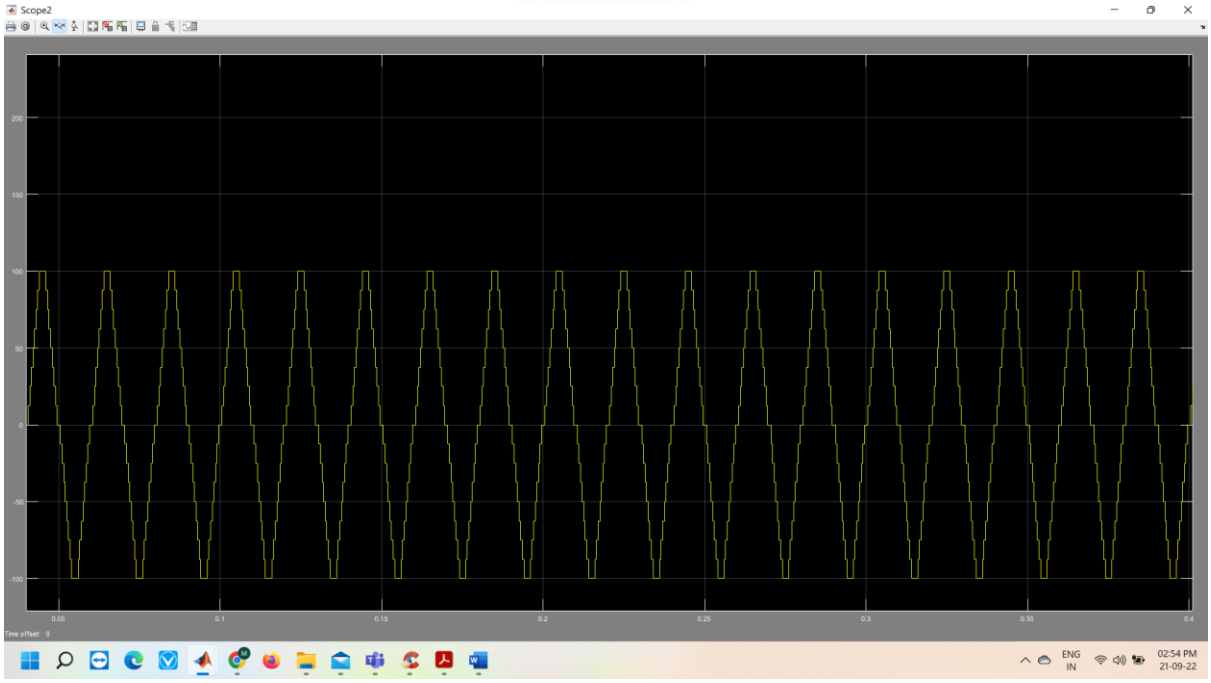
In other words, there are seventeen possible combinations of pole voltages at the zero state in the centre, and they all result in a differential mode voltage of zero.

5. SIMULATION RESULTS

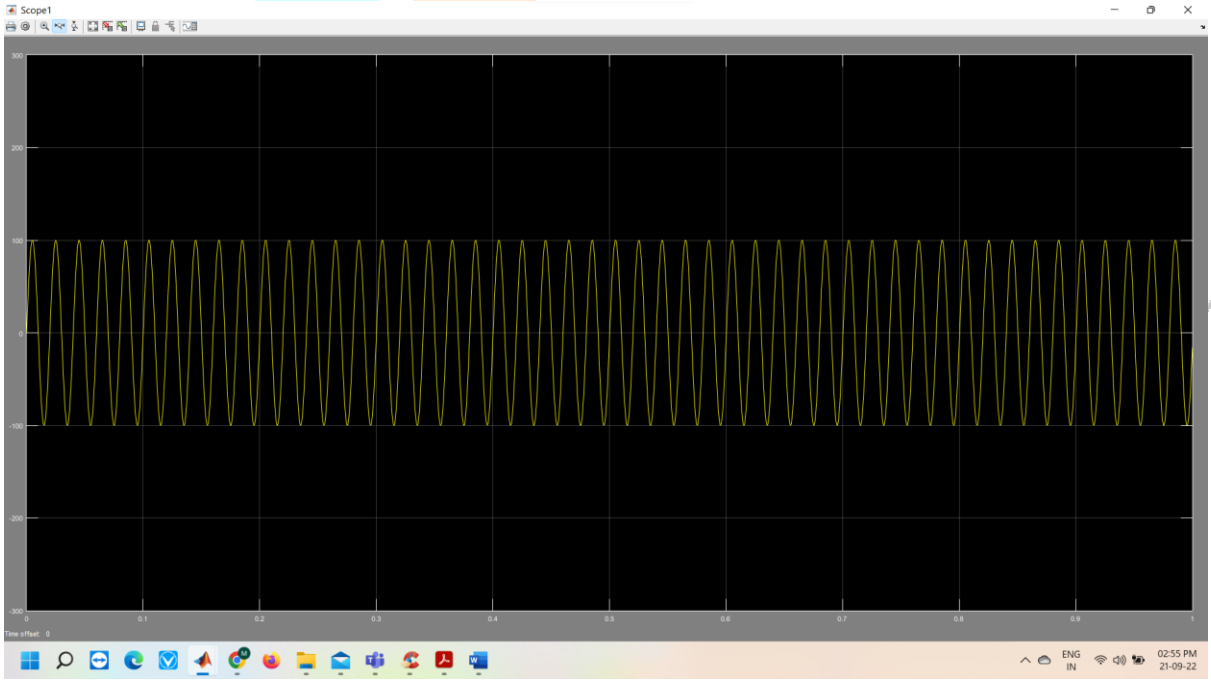
GATING PULSES



VOUT


Scope2
200
150
100
50
0
-50
-100
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
Time offset: 0
ENG
IN
02:54 PM
21-09-22

IOUT


Scope1
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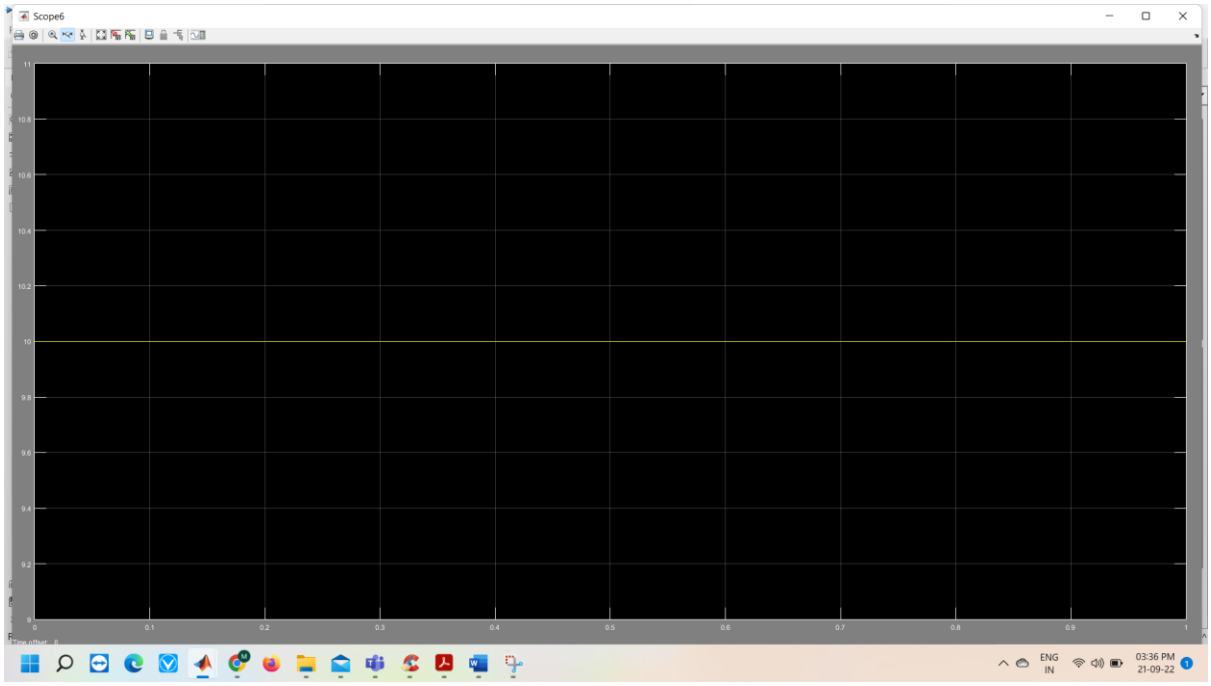
100
0
-100
-200
-300
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Time offset: 0
ENG
IN
02:55 PM
21-09-22

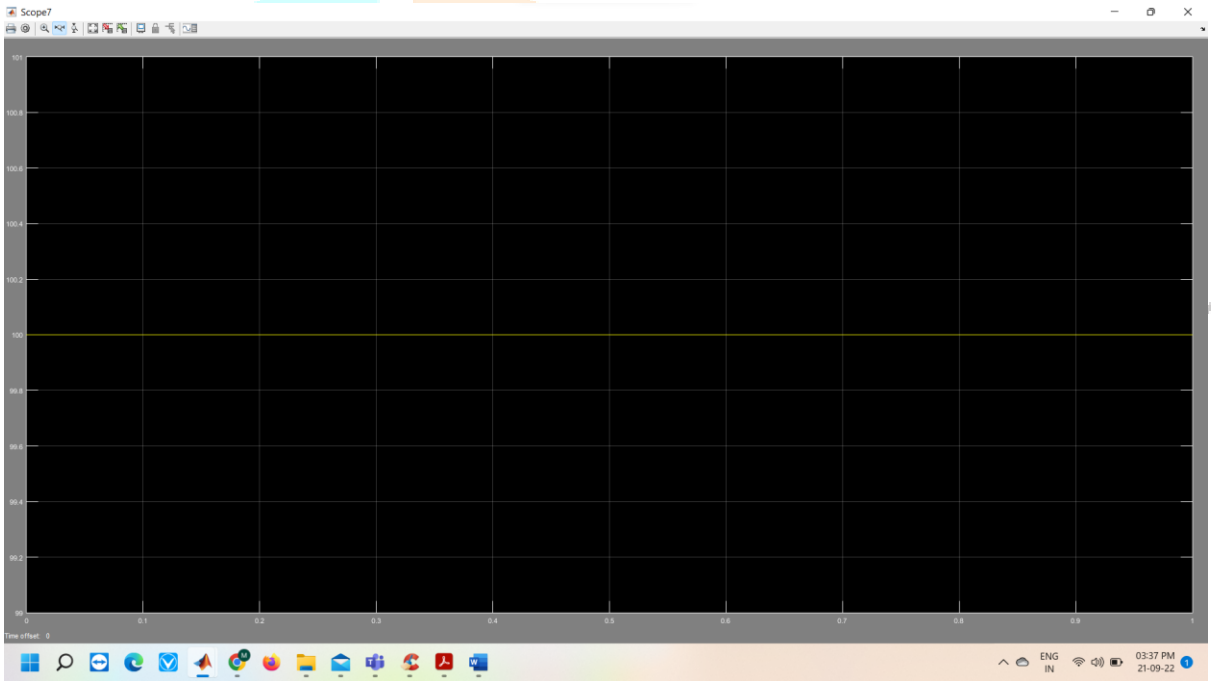
VAC1

VAC 2

VAC 3



VAC4



CONCLUSION

Cascading three H-bridges with flying capacitors on the third level and three with floating capacitors on the sixth level creates a new seventeen-level inverter configuration. In order to obtain high performance output voltages and currents, the voltages of each capacitor are instantaneously altered in a short number of switching cycles across all loads and power factors. This is done in an effort to reduce the number of switching cycles required. This is done in order to reduce the necessary amount of switching cycles as much as possible. The proposed configuration is based on a solitary DC link, which serves as the point of origin from which all other voltages are generated. Back-to-back converter functionality can be achieved by simultaneously drawing power from the grid and supplying that power to it at a predetermined power factor. The inverter with seventeen levels that was suggested is additionally more reliable. The inverter can continue to supply full power to the load even if one of the H-bridges fails, as long as the number of levels is reduced. This allows its use in highly important fields like marine propulsion and traction, where dependability is of the utmost importance. Because of its modular and symmetrical design, the proposed configuration can easily be scaled up to support higher phase counts, such as 5 and 6 phase configurations, while still using the same control logic. In this particular experiment, a three-phase 3 kilowatt (kW) squirrel cage induction motor is used in order to investigate and validate the efficacy of the inverter across a variety of modulation indices and load currents. The goal of this

particular experiment is to investigate and validate the efficacy of the inverter in a variety of applications. We were able to evaluate the resilience of the capacitor balancing method in an experimental setting by suddenly accelerating the motor while it was not under any load and measuring the capacitor voltages at various load currents. This allowed us to determine whether or not the method was effective.

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