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Ternary D-Latch Logic Implementation using Graphene Nano Ribbon Field Effect Transistor

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Abstract: Multi Valued Logic (MVL) presents a better information density as compared to a Boolean system. MVL is subdivided into ternary, quaternary, quinary etc. The ternary logical system is the maximum possible MVL system and may be utilized by the studies network because of its simplicity and difference among distinctive logical stages. More discrete voltage stages are required to pick out distinctive logic values over the range i.e., 0 to 1.2V. Ternary logic became initially applied in Complementary Metal Oxide Semiconductor CMOS (Complementary Metal Oxide Semiconductor) era however this introduces short channel effects, scaling limitations, Drain-induced barrier lowering DIBL (Drain Induced Barrier Lowering), and power consumption. So, a brand-new era has appeared specifically carbon-based field effect transistors. CNTFET (Carbon Nanotube Field Effect Transistor) and GNRFET (Graphene Nano Ribbon Field Effect Transistor) are kinds of carbon transistors. In this paper we are using the GNRFET in place of CMOS technology. We can design the proposed logic with using the one NTI (Negative Ternary Inverter), and Four NAND gates. To achieve the calculation of performance parameters we use the HSPICE 16 nm technology

Index Terms **- GNRFET, NTI, Ternary, D-Latch.**

I. INTRODUCTION

The three-valued logic called with different terms those are the trinary logic, trivalent, ternary, trilean, and 3VL. Truth values with inside the idea of ternary logic judgment may be described mathematically the use of numerous representations, such as -, 0, + or 0, 1, 2 or 0, 1/2, 1 or respectively false, indeterminate, true. In the ternary variety system, the radix or base is 3. Finding and correcting mistakes in ternary logic judgment isn't difficult. Three-valued 3VL logic judgment that has three reality values: true, false, and determined third value.

A latch is a digital circuit, which adjustments its output primarily based totally at the carried-out input. Here the set condition is placed for one input then the opposite condition always be in Reset. It is a bi-stable circuit whose states are represented as 0 and 1. Generally, latches are made of gates. The main difference between the latch and flip flop is latch requires enable signal to send information to output it doesn't require clock signal whereas the flip flops are triggered based on clock. Latches are also the memory elements same as the flip-flops but the main difference between these two are the latch operate with the enable value, but in case of flip flop it operates with the clock signal. The latches are used mainly in the onetime propagation circuits.

The overall performance of 3 valued D-Latch logic operations measured with help of parameters like power and delay. It concluded that circuit reduces power and delay discussed [1]. D-latch the use of GNRFET turned into proposed with the aid of using Badug Madhuri in 2019. This article indicates the development of a ternary D-latch the use of a Graphene Nanoribbon FET. The overall performance of a GNRFET may be improved with the aid of using setting extra GNRs. Ternary logic primarily based totally on multi threshold GNRFETs. The number of ribbons is increased in GNRFET results in the higher performance and lower power consumption [2]. Performance is progressed with a Power-gated transistor in phrases of parameters which are the delay, and power consumption. In this proposed design is TSPC D flip flop using power gated GNRFET. It improves energy dissipation and delay [3]. In this paper enhance the area and circuit performance. Here the GNRFET properties are mentioned and calculated. It is new design for D-latch using master slave flip flop. This discusses properties of GNRFET and results in better than other comparative analysis of power and delay [4]. In modified circuit adding transistor i.e., removed the glitches present in the circuit. The performance parameters compared with previous GNRFET based circuit's measure consumption and dissipation [5]. GNRFET circuits are classified into Metal Oxide Semiconductor (MOS) - GNRFET and Schottky Barrier (SB) - GNRFET. MOS-type GNRFETs were observed to be greater appropriate for designing logic gates due to the fact they act like semiconductors. The traits of the MOS-type GNRFET are higher than the ones of the SB-type GNRFET in phrases of parameters. This paper performance for both types is discussed [6]. The use of Graphene Nanoribbon is just like that of CNTs. GNRs narrow than CNTs and current fluctuation measured with the help of frequencies which is a disadvantage in CNTFET. While changing the ribbon width the electrical properties also changed that discussed in [7]. In this paper GNRFET based basic logic circuits and gates are compared with the previous technology which are CNTFET and CMOS. So, the performance parameters of each and one compared and analysis of three technologies are discussed. This article is a comparative evaluation of GNRFET primarily based totally ternary common-sense gates and CMOS and CNTFET primarily based totally circuits the usage of strength. Different implementations are primarily based totally on ternary common-sense gates the usage of GNRFET. Design of basic logic gates and arithmetic circuits discussed and compared their properties [8]. The fundamentals of shift registers and flip flops are explained in this paper. This article tries to triumph over the troubles in VLSI. The supply voltage directly proportional to the circuit speed if voltage decreases then speed also decreased [9].

CNTs can be used to enhance the stableness of the GSRAM cell. This indicates that the stableness is higher in CNT and GNR than in CMOS [10]. GNR based 6T SRAM is compared with FinFET based SRAM and noted the results. While comparing the both the FinFET based SRAM is better than GNR based SRAM [11]. 1-bit SRAM has been changed with GNRFET and simulation done with 32nm technology. It concludes that power dissipation is much less in comparison to CMOS [12]. This proposed work investigates the performance of 1- input, 2-input and 3-input GNR basic Boolean gates and compared the parameters like delay, area and power consumptions [13]. The impact of converting the quantity of GNR at the running parameters of gates along with 2:1 MUX, Half Adder, has been studied. Delay, electricity and PDP were proven to enhance with GNRFET than with CMOS [14]. The universal gates performance using Graphene Nano-Ribbon Field Effect Transistor is elaborated. Performance parameters compared for both technologies i.e., Graphene Nano Ribbon and silicon-based CMOS those are shown in [15]. GNRFET is the best replacement technology of Si-CMOS because it reduces short channel effects, reduce the power consumption and power delay. The HSPICE 32 nm technology Simulation is used find the difference between the GNRFET and Si-CMOS [16]. An overall performance evaluation and implementation of a 1-bit and multi-bit ALU primarily based totally on GNRFET and traditional CMOS is shown. Graphene architecture takes advantage over conventional CMOS device [17]. It in particular makes a specialty of the fabrication of edged MLGNRs as opposed to a densely packed MWCNT bundle. MLGNR calls for much less area as compared to MWCNT [18]. The article discusses how a GNRFET works and the way threshold voltage and different tool traits relate to tape size. This is a comparative evaluation among CNTFET and GNRFET in phrases of overall performance. The article discusses how a GNRFET works and the way the brink voltage and different traits of the tool relate to the scale of the ribbon [19]. Graphene is a single carbon tight packed in 2D honeycomb lattice. GNRFET is new technology in place of CMOS and electrical properties are better in GNRFET compared to CMOS [20].

The section I defined with the introduction and previous work done in GNRFET technology. Section II mentioned with NTI (Negative Ternary Inverter) and NAND gate logic in terms of GNRFET. Section III introduced with the GNRFET characteristics. Section IV introduced with the proposed work, and final Section V introduced with the simulation results using HSPICE 16nm technology.

II. TERNARY LOGIC

Ternary logic performs faster calculations compared with binary logic and also it reduces the short channel effects. Ternary logic is the most effective logic system in Multi valued logic system (MVL). Ternary desirable logic is the extension of binary desirable logic and it having three logic states. It can be represented with three states namely logic'0' state, logic '1' state, logic '2' state. Voltage values are defined for these states can be defined with 0, Vdd/2 and Vdd respectively. Below we noted the formulas for ternary logic gates, by using these formulas we can write the truth tables for all basic gates and universal gates.

$$Ii+Ij = \max(Ii,Ij) \quad (1)$$

$$Ii.Ij = \max(Ii,Ij) \quad (2)$$

$$\tilde{I} = 2 - Ii \quad (3)$$

Where AND represent with '+' symbol and OR represent with '.' symbol.

2.1 Ternary Inverter

Ternary Inverter subdivided into three types those are the NTI (Negative Ternary Inverter), PTI (Positive Ternary Inverter), and STI (Standard Ternary Inverter). Among these we require only NTI inverter for designing the proposed logic circuit.

Table 1: T-Inverter Truth Table

INPUT	NTI	PTI	STI
0	2	2	2
1	0	2	1
2	0	0	0

Negative Ternary Inverter designed with one PGNRFET and one NGNRFET. NTI logic circuit having the input voltagelevels are 0V , 0.45V, and 0.9V. When input voltage is equal to 0.45V or 0.9V, the output voltage should be equal to 0V.The input voltage is in logic 0 state, the ouput voltage must be logic 2 state.

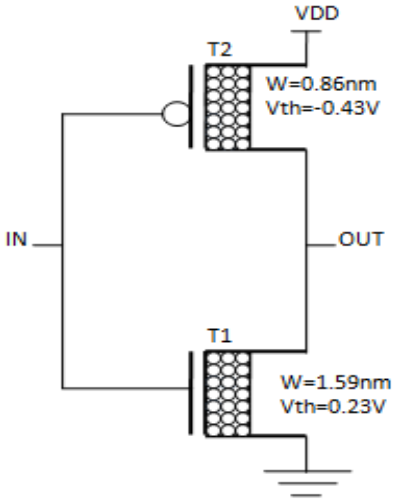

Figure 1: Schematic diagram for NTI

2.2 Ternary NAND Gate

NAND gate designed with five PGNRFETs and remaining five are NGNRFETs. The threshold voltage specifications for NAND gate defined with based on width of GNRFET transistors. When NAND gate input voltage changing from 0V to 0.9V then the NAND gate output also changed according to the ternary logic combinations.

Table 2: Ternary NAND Gate Truth Table

Input1	Input2	OUTPUT
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1
2	0	2
2	1	1
2	2	0

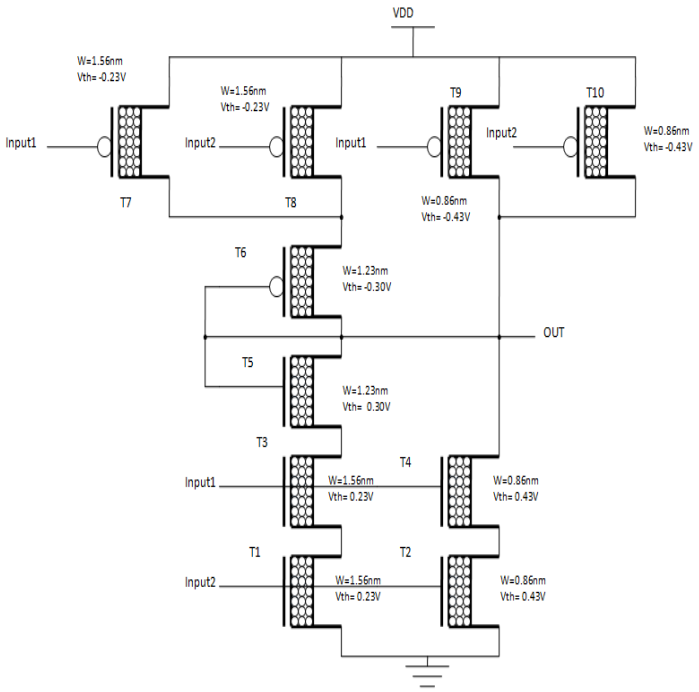

Figure 2: Circuit diagram of T-NAND gate

III. GNRFET

Nanoribbons also called nano graphene ribbons or nano graphite ribbons, often abbreviated GNRs, are strips of graphene with ultra-thin width (< 50nm). Graphene ribbons were introduced as a theoretical model by Misutaka Fujitha and coauthors to examine the edge and nanoscale size effect in graphene.

Graphene effectively conducts warmth and power alongside its plane. The fabric decisively absorbs mild of all considerable wavelengths, which corresponds to the darkish color of graphite; however, unmarried sheet of Graphene is almost immediately because of its excellent thinness. In addition, this fabric is numerous instances greater grounded than the maximum grounded metal of comparable thickness. Graphene has developed into an essential and beneficial Nano material because of its amazingly excessive elasticity, electric conductivity, transparency, and being the thinnest two-dimensional cloth at the planet. The worldwide Graphene marketplace became worth $nine million, with the giant majority of hobby in progressive tendencies in semiconductors, gadgets, electric powered batteries.

- Higher electron mobility
- Superb electron and heat conductivity, greater than copper.
- Stronger than diamond and steel.
- It can be used to make anti-bacterial materials as well as biodevices.
- Very less break over voltage i.e., less than 0.3V.

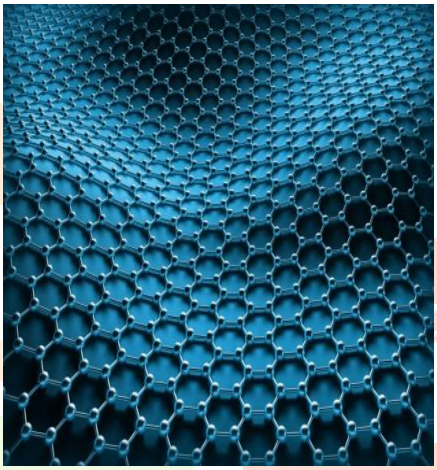

Figure 3: Graphene Structure

The Block diagram of Graphene Nano Ribbon Field Effect Transistor as shown below.

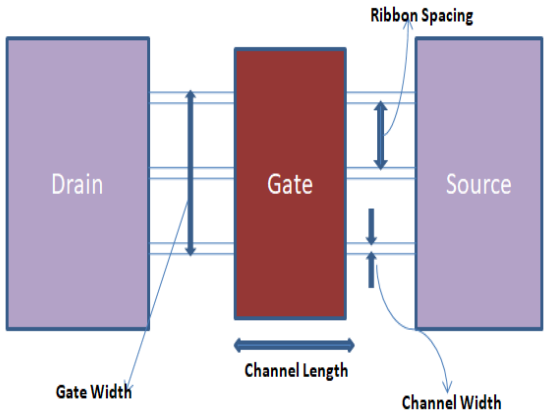

Figure 4: Block diagram of GNRFET

Three of the 4 electrons with inside the outer shell of every particle in a Graphene sheet occupy three sp2half and half of orbital's, which might be an aggregate of s, px, and py orbital's which are shared with the 3 nearest atoms, forming σ bonds. The duration of those bonds is set 0.142 nm. The extra electron of the outer shell occupies the pz orbital positioned contrary to the plane.

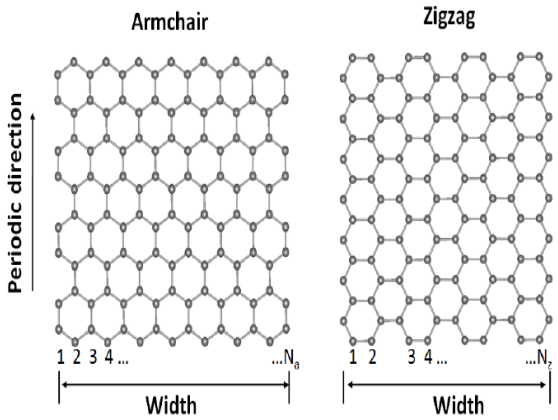

Figure 5: Different Types of GNR's

IV. PROPOSED WORK

The D-Latch is implemented the usage of one NTI, One STI, four NAND ternary gates and one OR gate. The output of D-latch i.e., Q will be identical to the input data while input enable in minimum state.

The enable in excessive state, the D – latch might be the formerly stored data. Enable is equal to 0 (low) then the D –latch sends the information data to the output here in this case the output is equal to input until the enable changes its state i.e., high. When enable moves to high (2) state the D-latch stores the previous information.

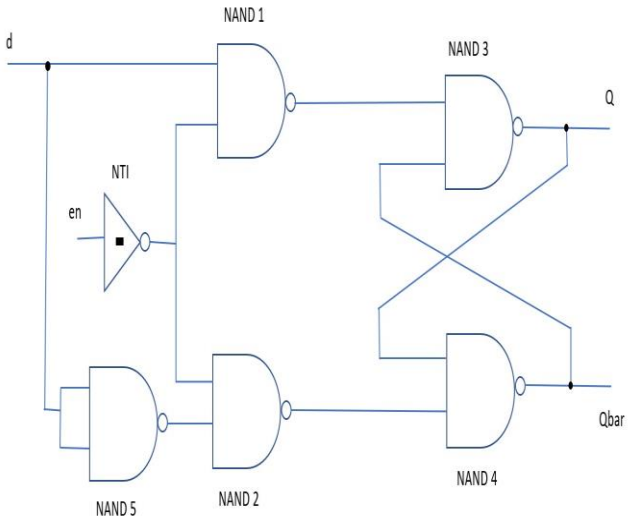

Figure 6: Block Diagram representation of Ternary D-Latch

Table 3: Ternary D-Latch Truth Table

En	din	Q	Qbar
0	0	0	2
0	1	1	1
0	2	2	0
2	X	Q_{prev}	$Qbar_{prev}$

Proposed D-Latch can be implemented with different widths and threshold voltages of GNRFETs which are mentioned in the circuit diagram. Width calculation can do with usage of Dimer lines.

The implementation of proposed work done with adding one extra OR gate. The software simulation tool used for proposed work is HSPICE. By using HSPICE 16nm technology the power and delay are analyzed. Finally, the proposed work having some good qualitative parameters.

V. RESULT

The proposed work of design of OR based D-latch using GNRFET simulation can be done with use of HSPICE 16nm technology. The D-Latch output waveforms are shown below fig.7. Finally, it is concluded that the proposed work results in higher performance, reducing power consumption and reducing power delay.

The proposed work performance parameters are compared with the existing method and tabulated the comparison parameters in terms of power consumption and delay are shown below.

Table 4: Result Comparison For D-Latch

PARAMETERS	THIS METHOD	EXISTING METHOD
Delay	5.639e-09	150.04e-09
Average Power	7.235e-08	20.60e-06
PDP (Power Delay Product)	4.079e-16	3.0908e-12

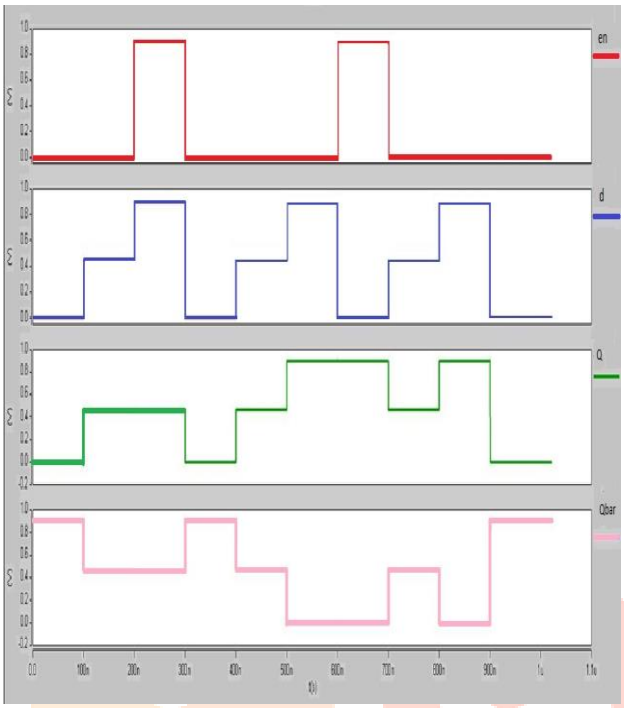

Figure 7: Waveform of Ternary D-Latch

V. CONCULSION

Based on the GNRFET transistors the ternary D-Latch operation has been explained and the performance of the circuit noted down. GNRFET transistors are the upcoming technology in place of silicon transistors so it has to be found that the replacement is better than standard MOS transistors. Here the number of ribbons placed in the GNRFET is variable which means we can change the threshold voltage levels by changing the Dimer lines. This paper concluded that the reducing the power consumption in D-latch with 16nm HSPICE Technology.

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