IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Design and Analysis of T-Slot Micro strip Patch Antenna

[1]Raju Verma, [2]Sudhir Singh

[1]Research Scholar, [2]Assistant Professor

[1]Department Of Electronics And Communication Engineering,

[1]Uma Nath Institute Of Engineering & Technology (V.B.S. Purvanchal University), Jaunpur, India

Abstract: Microstrip antennas are becoming very widespread within the wireless and mobile communication because of their various advantages over the conventional antennas. Microstrip antennas have many advantages over the conventional antennas because of light weight and low volume, low profile planar configuration which can be easily made conformal to host surface, low fabrication cost, capable of dual and triple frequency operations, mechanically robust when mounted on rigid surfaces. Rectangular microstrip antenna exhibits several limitations such as low bandwidth, low efficiency, low gain and directivity owing to the excitation of surface waves. There are numerous and well-known methods to increase the bandwidth of antennas, including increase of the substrate thickness, the use of a low dielectric substrate, slotted patch antenna, the use of various impedance matching and feeding techniques**.**

I. INTRODUCTION

In analog circuit designing, current conveyor (CC) is one of the basic units in current mode techniques. Normally a semiconductor ideally used for basic analog signal processing functions with the support of proper circuitry. The current conveyor also simplifies the circuit design in multiple of ways like conventional operational amplifier do. New and useful implementations can be introduced by extending an alternate manner of removing complex circuit with the help of Current conveyor. Despite an active building blocks the current conveyor having a capacity to replace classical operational amplifier in the voltage mode applications [2]. This can add extra advantages to transform typical voltage mode applications into current mode. The working of current conveyor has gained attention of many researchers and thus many group of product of basic current conveyor have been implemented in the last two decades. In voltage-mode circuits, operational amplifier acts as a building block, which is used to add, amplify, subtract, filter, attenuate, and voltage signal. In current-mode circuit, the analogous building block is the current conveyor. The current conveyor introduced first was a three- terminal block in which x and y were input terminals and z was output terminal having following properties:

1. Input terminal(x) potential is equal to the voltage applied towards the end of terminal(y).
2. An input current applied at the terminal x results in flowing equal amount of current at node y.
3. Input current which is flow between X node is conveyed to node z, which has the features of high output resistance current source.

In many analog blocks and analog circuits, differential pair [3] acts as active element as an input current or voltage source. Some years ago designers have used differential pair to work as an input stage of operational amplifier to design different types of analog circuits. After that differential pair was used in many circuits which have voltage inputs. In this project work the main focus is on VDCC block in which differential pair works as an input stage. As the development of integrated circuits is increased, use of differential pair as an input stage in bipolar and CMOS circuits is also increased due to its main advantages such that improved signal rejection property and large gain in comparison to its single ended counterpart.When the external circuit connected to the input terminals of current conveyor is decoupled then the current is transferred from the input terminals to the output terminal.

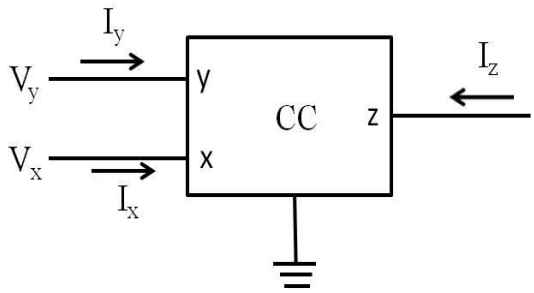

Figure 1.1: Current Conveyor Block Diagram [2]

2. LITERATURE REVIEW

In 2013 paper "Positive/negative lossy/lossless grounded inductance simulators employing single VDCC and only two passive elements" published in International Journal of Electronics and Communications, Elsevier, written by Firat Kacar, Abdullah Yesil, Shahram Minaei and Hakan Kuntman [19] designed third order Butterworth high pass ladder filter circuit using VDCC based inductance simulators. Results of this paper are as follows:

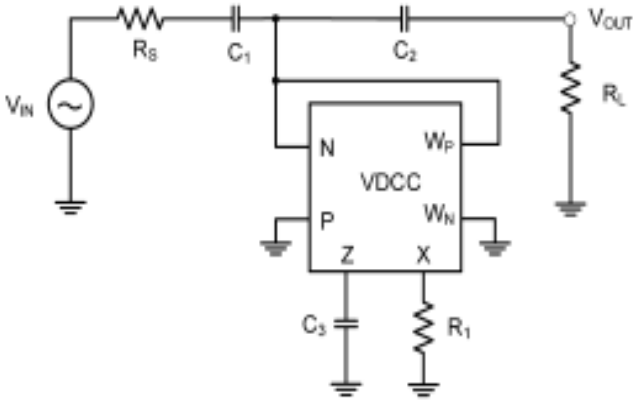

Figure 2.1: Block Diagram for High Pass Filter [19]

In 2014 paper "Z-Copy Controlled-Gain Voltage Differencing Current Conveyor: Advanced Possibilities in Direct Electronic Control of First-Order Filter" published in ELEKTRONIKA IR ELEKTROTECHNIKA, written by R. Sotner, N. Herencsar, J. Jerabek2, R. Prokop, A. Kartci, T. Dostal, K. Vrba [20] designed reconfigurable reconnection less multifunction filter in which there is no need to change input or output terminal to change the transfer function.

In 2015 paper "A Voltage mode biquad with lowpass, bandpass and notch outputs using Voltage Differencing Current Conveyor" published in International Journal of Advanced Research in Computer and Communication Engineering, written by Mayank Rawat, Dr. Malti Bansal [21] designed voltage mode multifunction biquad filter which consists of gain blocks, summer and integrators.

In 2015 paper "A Voltage mode biquad with lowpass, bandpass and notch outputs using Voltage Differencing Current Conveyor" published in International Journal of Advanced Research in Computer and Communication Engineering, written by Mayank Rawat, Dr. Malti Bansal [21] designed voltage mode multifunction biquad filter which consists of gain blocks, summer and integrators.

3. PROPOSED WORK

VDCC transfers voltage and current in its correspondent terminals and provides trans-conductance gain which is electronically tunable. Different devices like filters, multipliers, simulators etc. can be designed efficiently using the VDCC. CMOS circuits for low pass, high pass and band pass filters are designed and simulated in PSpice tool using 180nm library. All the circuits and waveforms are included in this chapter. PSpice stands for Personal Simulation Program with Integrated Circuit Emphasis. It is a circuit simulator for the simulation and verification of analog as well as mixed signal circuits. PSpice was first introduced by MicroSim in 1984. A file with code or schematic diagram also called net list is analyzed and simulated in PSpice. It also includes waveform viewer and program analyzer. There are three analyzes which can be done in PSpice. These analyzes are as follows:

1. **Transient Analysis:** This analysis is done when the circuits have time variant sources like sinusoidal sources or switched DC sources. In this analysis voltage at each node and current in each branch over a specific time interval are calculated and output is the instantaneous value.

2. **DC Analysis:** This analysis is done when the circuits have time invariant sources like steady state DC sources. In this analysis voltage at each node and current in each branch over a specific range of values are calculated. Linear Sweep and Logarithmic Sweep are some examples of this analysis.

3. **AC Analysis:** This analysis is done when the circuits have components with varying frequency for small signal. In this analysis magnitude and phase angle of voltage at each node and current in each branch over a specific range of frequencies are calculated.

3.1. VOLTAGE DIFFERENCING CURRENT CONVEYOR

Circuit_Description The circuit symbol of the proposed active element,VDCC, is shown in Fig. 4.2, where P and N are input terminals and Z, X, W_P and W_N are output terminals. Ideally, the VDCC is an active block which is the combination of OTA and MO-CCII as shown in Fig. 4.1.

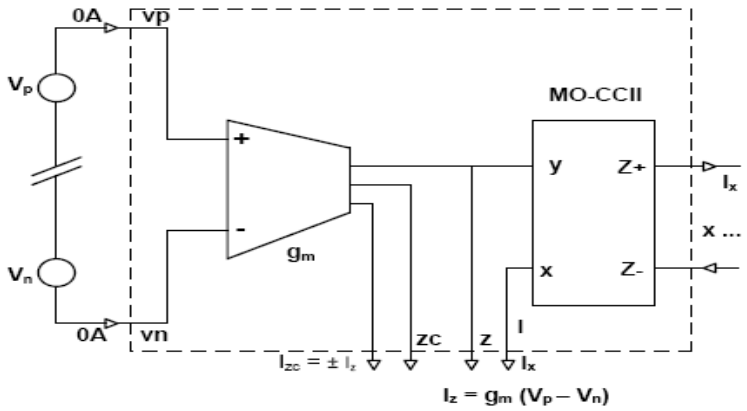

Figure 3.1.1: Internal structure of VDCC [17]

All of the terminals exhibit high impedance, except the X terminal.Using standard notation the port of an ideal VDCC.

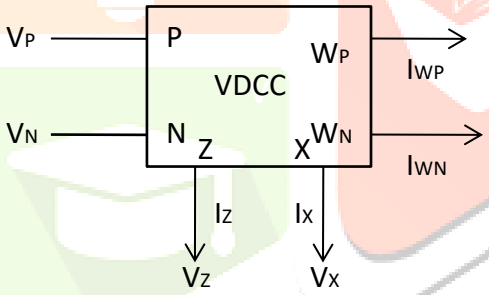

Figure 3.1.2: Voltage differencing current conveyor [17]

Using standard notation, the port relations of an ideal VDCC can be characterized by

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

According to the above matrix equation, the first stage can be realized by a balanced transconductance amplifier to convert the difference of the input voltages ($V_p - V_n$) into the output current (I_z) with transconductance gain of g_m and the second stage is a current conveyor used for transferring x-terminal current to W_p and W_n terminals. For a balanced CMOS transconductance amplifier, the parameter g_m can be given as

$$g_m = \sqrt{I_{B1}\mu_n C_{ox}\left(W/L\right)}$$

where μ_n is the mobility of the carrier for NMOS transistors, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length and I_{B1} is bias current. In the VDCC block [2] in the input stage we have a trans-conductance amplifier and in the output stage we have a second generation current conveyor.

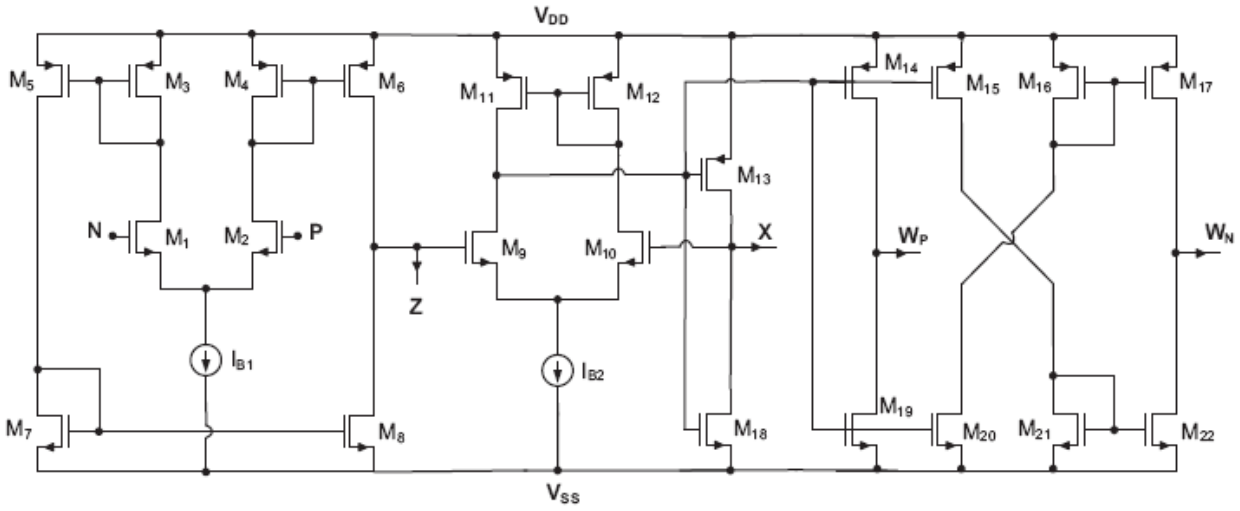

Figure 3.1.3: CMOS Realization of VDCC [18]

Table1: Transistors aspect ratios for the VDCC of Fig.4.3.

Transistors	W/L (μm)
M1–M4	3.6/1.8
M5–M6	7.2/1.8
M7–M8	2.4/1.8
M9–M10	2.4/1.8
M11–M12	9/0.72
M13–M17	14.4/0.72
M18–M22	0.72/0.72

The CMOS schematic of VDCC shown in fig.4.3 was simulated in PSpice
using TSMC CMOS 0.18µm model parameters [2]. The aspect ratios of the transistors used are given in Table 1. The supply voltages are chosen as V_{DD}=-V_{SS}= 0.9V, I_{B1} = 50µA and I_{B2} = -100µA. The following analysis has been carried out:
DC sweep (to obtain the linear voltage for various current and voltage transfers),

4. Results

Simulation was performed using a CMOS realization of VDCC given in fig 4.3. To prove the theoretical validity of single VDCC biquad filter of figure 4.10 for pole frequency (f_0) = 5MHz the filters were simulated with responses are shown in fig 4.11 to fig 4.13 respectively. The simulated center frequency of BPF was measured as 5.30 MHz. 3dB (cut-off) frequency of LPF and HPF were measured as 5MHz and 4.56MHz respectively.

To study the time-domain behavior of the proposed filter, an input sinusoidal signal of amplitude 10mV is applied. The transient response for low-pass, band-pass and high-pass are shown. To show the effectiveness of the proposed structure, sinusoidal signal of frequencies of 100 KHz, 100 MHz having amplitude of 10mV each is applied at the input of the low pass filter and high pass filter and sinusoidal signal of frequencies of 100 KHz, 5 MHz having amplitude of 10mV each is applied at the input of the band pass filter. The frequency spectrum of input and output are also given. It is clear that the 100 KHz signals is passed without attenuation and 100 MHz signal is significantly attenuated for low-pass response. There is appreciable reduction in amplitude of 100 KHz signal for both band-pass and high-pass responses. The sinusoidal signal of 5 MHz is passed through both band-pass and 100MHz through high-pass.

To study the impact of variation in resistance the Monte Carlo simulation (with 100 samples) has been carried out. The center frequency of band-pass response is taken as performance parameter. Figure 4.26 shows Monte Carlo simulations at 27◦C with 1% variations in resistance R_1. It may be noted that the variations affect the center frequency of the band-pass filter. It is found that there is 0.51% deviation in the mean value of the center frequency of band-pass response of proposed filter. Further, it is noted that the center frequency varies by a factor of 1.004 and 1.005 between the minimum and maximum values.

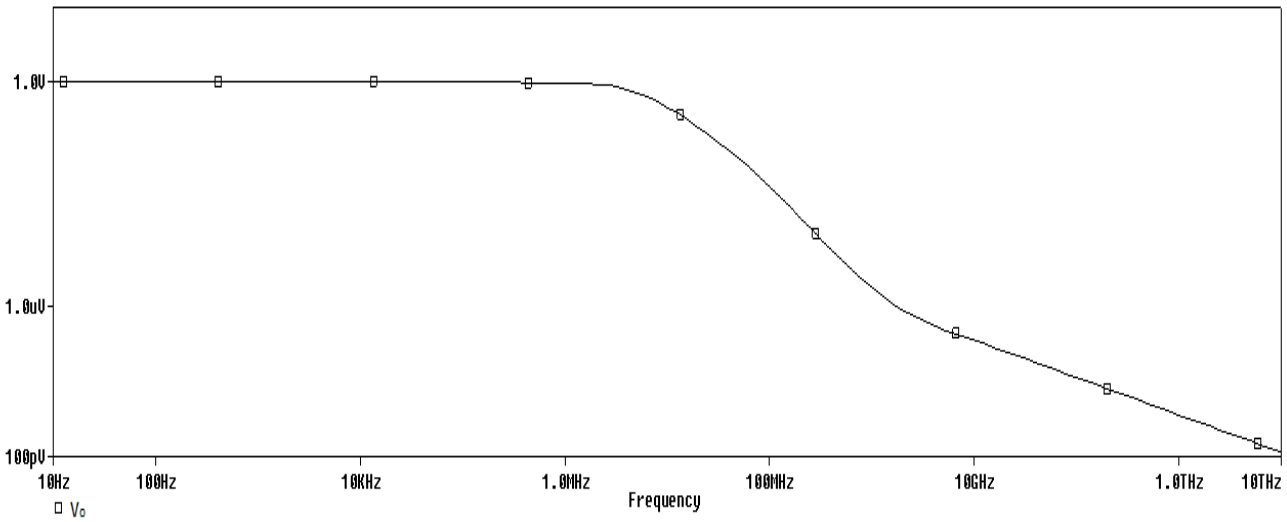

Figure 4.1: Frequency response of low pass filter

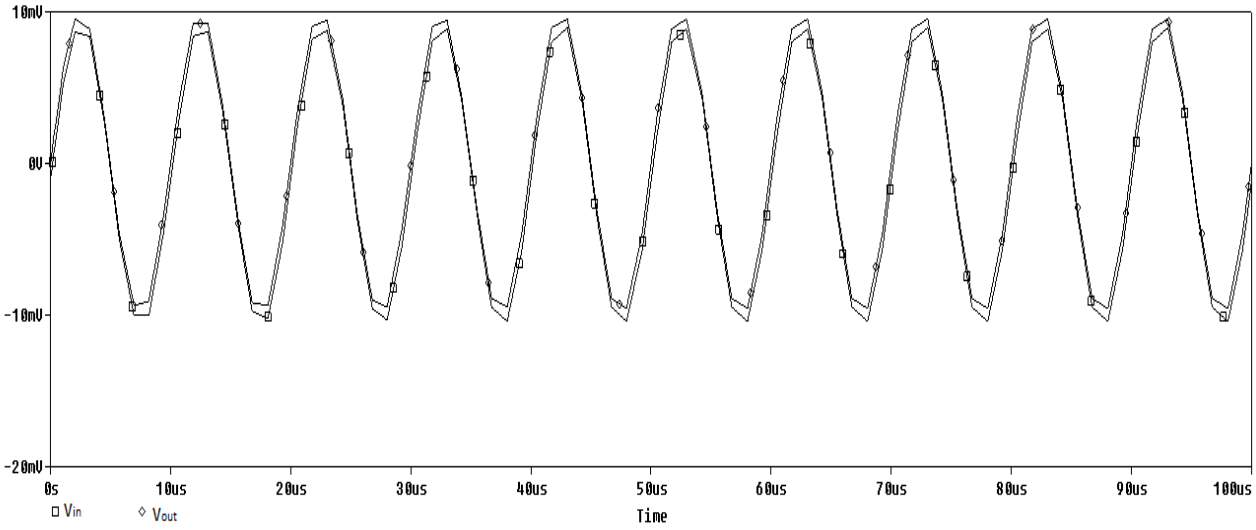

Figure 4.2: Transient response for low-pass output for frequency 100 KHz

5. CONCLUSION AND FUTURE SCOPE

In this thesis, I have designed low pass, high pass and band pass filter circuits using voltage differencing current conveyor (VDCC). Each circuit structure has been simulated in PSpice simulator. All the circuits are made from CMOS transistors and analyzed using 180nm TSMC CMOS technology. These circuits work efficiently and consume less average power compared to other designs published in previous literatures.

In future more designs can be constructed and analyzed using different types of current conveyor with less number of CMOS transistors. We know that technology is getting advanced and delay time, average power consumption & chip area are the main concerns which we have to solve in less time. Therefore not only filters but other important devices can also be designed for particular application. Cost is also an important factor so circuits should be carefully designed.

REFERENCES

[1] Adnan Kaya, E. Yesim Yuksel and Ugur Cam "Bandwidth Enhancement Technique Using Negative Inductance with Three FET for the Rectangular Microstrip Antenna," 47th IEEE International Midwest Symposium on Circuits and Systems, 2004.
[2] Jenifer T. Bernhard and Carolyn J. Tousignant "Resonant frequencies of rectangular microstrip antennas with flush and spaced dielectric superstrates," IEEE Transactions on Antennas and Propagation Volume 47, No. 2, pp. 302-308, 1999. [3] Bhatti, U. and Hanif. M. 2010. Validity of Capital Assets Pricing Model.Evidence from KSE-Pakistan.European Journal of Economics, Finance and Administrative Science, 3 (20).
[3]. C. A. Balanis, "Antenna Theory, Analysis and Design," John Wiley & Sons, New York, 1997.
[4] K. L. Wong, J.S. Kou and T. W. Chiou, "Compact Microstrip Antennas with Slots Loaded in the Ground Plane," IEE, pp. 623-626, 2001.
[5] Bahl, I.J. and Bhartia, P., "Microstrip Antennas," Artech House, Dedham, MA, 1980.
[6] Kumar, G. and Ray, K.P., "Broadband Microstrip Antennas," Artech House, Inc, 2003.
[7] Manik Gujral, "Bandwidth Enhancement of Dual Patch Microstrip antenna array using Dummy EBG Patterns on Feedline," ME thesis, National University of Singapore, 2007.
[8] Stutzman, W.L. and Thiele, G.A., "Antenna Theory and Design," John Wiley & Sons, Inc, 1998.
[9] Balanis, C.A., "Advanced Engineering Electromagnetics," John Wiley & Sons, New York, 1989.

[10] Hammerstad, E.O., "Equations for Microstrip Circuit Design," Proc. Fifth European Microwave Conf., pp. 268-272, September 1975.
[11] James, J.R. and Hall, P.S., "Handbook of Microstrip Antennas," Vols 1 and 2, Peter Peregrinus, London, UK, 1989.
[12] R. Garg, P. Bhartia, I. Bahl and A. Ittipiboon. "Microstrip Antenna Design Handbook," 2nd ed. Norwood, Massachusetts: Artech House, 2001.
[13] Richards, W.F., Microstrip Antennas, Chapter 10 in Antenna Handbook: Theory Applications and Design (Y.T. Lo and S.W. Lee, eds.), Van Nostrand Reinhold Co., New York, 1988.
[14] Newmanm E.H. and Tylyathan, P., "Analysis of Microstrip Antennas Using Moment Methods," IEEE Trans. Antennas Propag., vol. AP-29, No. 1, pp. 47-53, January 1981.
[15] Harrington. R.F., Field Computation by Moment Methods, Macmillan, New York, 1968.
[16] Kantorovich, L. and Akilov, G., "Functional Analysis in Normed Spaces," Pergamon, Oxford, pp. 586-587, 1964.
[17] D. Orban and G. J. K. Moernaut, "The Basics of Patch Antennas," Orban Microvave Products, September 2005.
[18] D. R. Jackson and J. T. Williams, "A comparison of CAD models for radiation from rectangular microstrip patches," Intl. Journal of Microwave and Millimeter-Wave Computer Aided Design, Vol. 1, No. 2, pp. 236-248, April 1991.
[19] H. Pues and A Van de Capelle, "Accurate transmission-line model for the rectangular microstrip antenna," Proc. IEEE, vol. 131, pt. H, no. 6, pp. 334-340, Dec. 1984.
[20] W. F. Richards, Y. T. Lo, and D. D. Harrison, "An improved theory of microstrip antennas with applications," IEEE Trans. Antennas and Propagation, vol. AP-29, pp, 3846, Jan. 1981.
[21] Kawei Qian and Xiaohong Tang, "Compact LTCC dual-band circularly polarized perturbed hexagonal microstrip antenna," IEEE Antennas and Wireless Propagation Letters, Vol. 10 pp. 212-1215,2011.