IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

HDL DESIGN Of EXA HERTZ PRBS GENERATOR FOR IDENTIFICATION OF PROPERTY Of PRBS PATTERNS FOR ULTRA HIGH SPEED WIRELESS COMMUNICATION PRODUCTS/APPLICATIONS

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Abstract: The Aim is to HDL Design for Exa Hertz Speed PRBS Carrier Generator ASIC for Ultra High Speed Long Distance Communication Hi-tech Smart Computing Products like Cloud & Internet Computing, LTE ASIC, WiFi, GiFi, OFDMA WCDMA, QCDMA, GPS, and WiMAX Technologies etc. Basically This Design Contains PRBS Generators of Different Tapped Sequences $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 etc. The PRBS Design by using Linear Feedback Shift register of various bit length(7,10,15,23,31). These different pattern sequences are Designated as per CCITT ITU Standards. This Soft IP Core Designed by Verilog HDL/VHDL Design flow Implemented by Xilinx ISE 9.2i IDE and FPGA Software. This PRBS Generator Mainly suit for latest coming generation New Innovative Low Power Portable Smart Computing Products like I phones, Tablets, Note Book, Pocket Multimedia SOC Computing, GPS Mobile phone Cards, GPRS, and Handheld Instruments etc.

Index Terms - LTE ASIC – Long Terminal Equipment, ASIC- Application Specific Integrated Circuit, CDMA- Code Division Multiple Access ,GPS – Global Position System, PRBS – Pseudo Random Binary Sequence , VHDL – Very High Speed Integrated Circuit Hardware Description Language.

I. INTRODUCTION

In the latest Modern Hi-tech Information Technology & Communication Engineering world, I speed is a major constraint factor for VLSI Chip Designs. Now Giga/Tera/Peta/Exa Hertz speed (Abps) based wireless & communication products came to the market. Now I Designed New Atto Hertz Speed (Abps Rate) PRBS Carrier Generator for All Latest new Innovative & future generative Hi-tech Wireless Portable Smart Computing Products & Cards. In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing ,wireless Internet Data Packets Transceivers Computing, Tablets, Pocket Mobile Multimedia Systems, Note Book Computers, Wireless Routers,NOCs,NetworkCards/Racks,WiFI,GiFi,Wimax,GPS,GSM, QCDMA Tranceivers.For that purpose ,I Designed Giga Bits Per Second ,Tera Bits Per Second & Peta Bits Per Second High Speed PRBS is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. PRBS Generators, Receivers, Transceivers Designed for HiFi Wireless Internet Data Packets Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7, 10,15,23,31 at a Clock carrier frequency speed of Gbps/Tbps/Pbps.the Length of PRBS sequence is 2^L-1. 2^L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, WiFI,GiFI,LTE, Wireless OFDMA , CDMA,QCDMA Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms Gbps,Tbps,Pbps . All these PRBS LFSR Sequences are designed by tapping different points according to ITU O.150, O.151, and O.152 Standards. This PRBS Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of Gbps/Tbps/Pbps Speed. The

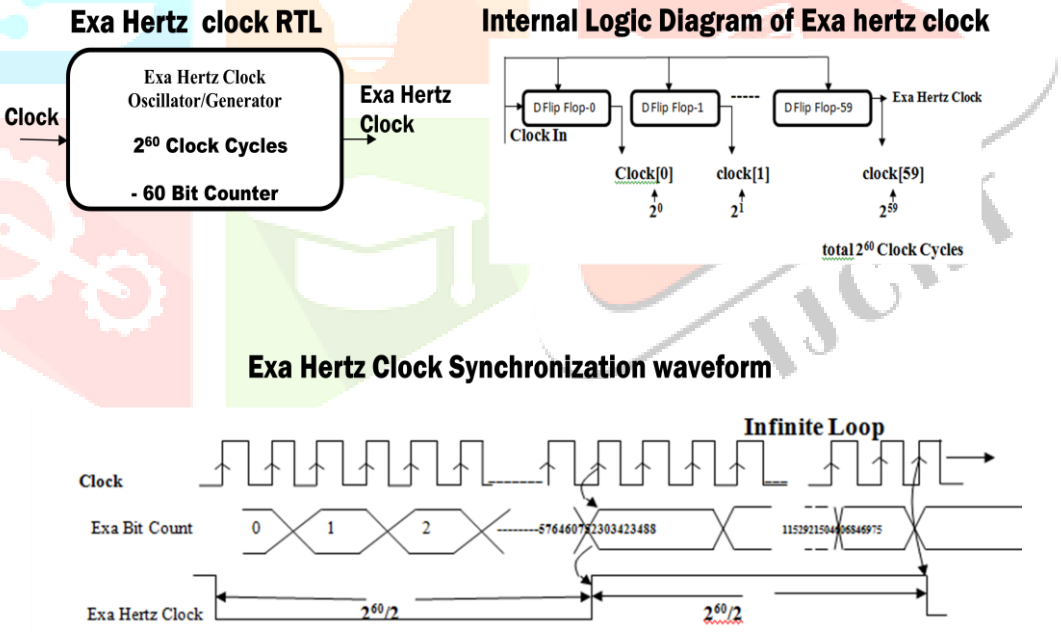
Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers. these are simply Linear Polynomial Checkers & CRC .

Table 1.1: PRBS DESIGN FREQUENCY STANDARDS

PRBS TYPE	STANDARD	SUGGESTED DATA RATE(Kilo Bits Per Second)	FEED BACK TAP
2^7-1	ITU-T O.150	14.4	7,6
2^{10}-1	ITU-T O.150	64	10,3
2^{15}-1	ITU-T O.150	1544, 2048, 6312, 8448, 32064, 44736	14,15
2^{23}-1	ITU-T O.150	34368, 44736, 139264	18,23
2^{31}-1	ITU-T O.150		28,31
2^{48}-1	ITU-T O.150/151/152		48,42
2^{52}-1	ITU-T O.150/151/152		52,47
2^{63}-1	ITU-T O.150/151/152 /153		48,63

Table(1): PRBS bit-pattern are generated in a linear feed-back shift-register. This is a shift-register with a XORed feedback of the output-values of specific flip-flops to the input of the first flip-flop.

II. EXA HERTZ CLOCK GENRATOR



2.1: Description: Exa Hertz clock generator consists of 60 bit counter generate 2^{60} Clock cycles of 1 complete Exa hertz clock cycle. Exa Hertz clock output of one full clock cycle generated at the 2^{60}th count value by increment the count value of 5.85467952E+16. if we make count = count+60'b1000_0000_00…..; on the very next clock period Exa hertz clock generated due to this we reduced number of clock cycles period for improvement of high speed and performance, access latency. The Exa Hertz Clock pulse low and high toggling happens at every 2 power 60 divided by 2 clock = 5.85467952E+16 count value. The Exa hertz positive clock edge/negative clock edge trigger happens at every count value of 5.85467952E+16.

2.2: EXA HERTZ CLOCK Generator Code

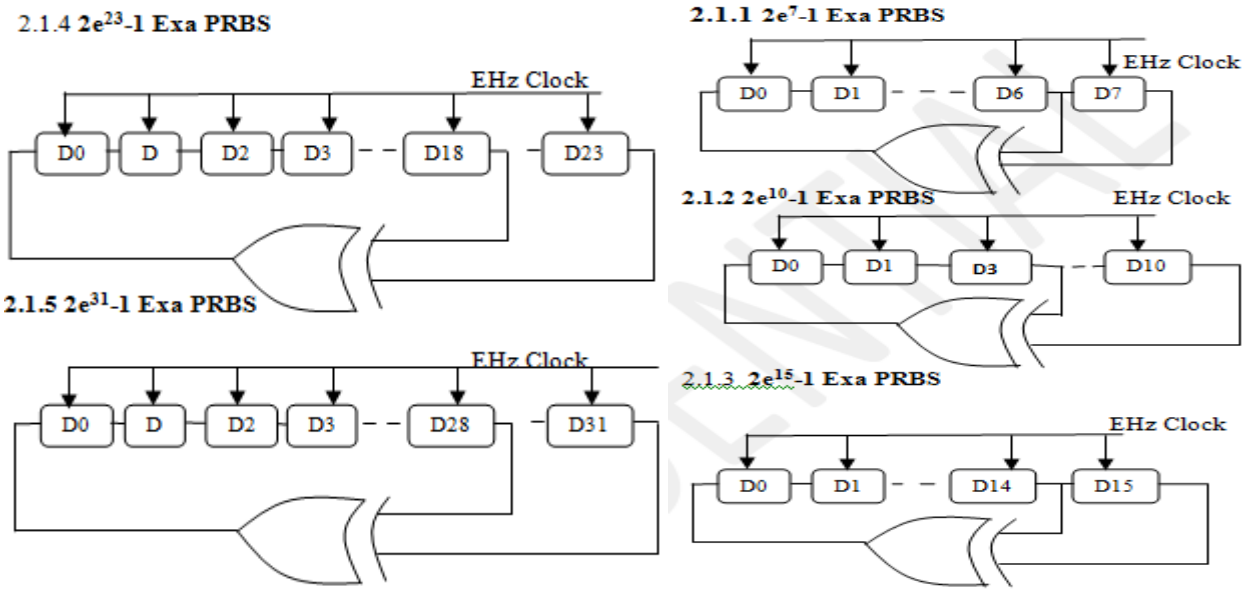
Real Time Verilog HDL- Exa hertz Clock generator RTL DUT

```
module exa_hz_clock(ref_clock, exa_hz_clock);

  //exa hz clock ios
  input ref_clock;
  output reg exa_hz_clock;

  //exa hz clock signals
  reg [59:0] exa_hz_counter = 40'b0000_0000_0000_0000_0000_0000_0000_0000_0000_0000;

  // exa hz counter generation
  always@(posedge ref_clock)
    begin
      exa_hz_counter =
exa_hz_counter+60'b1000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000;
      exa_hz_clock = exa_hz_counter[59];
    end
endmodule
```

// Exa Hertz clock generator Test Bench

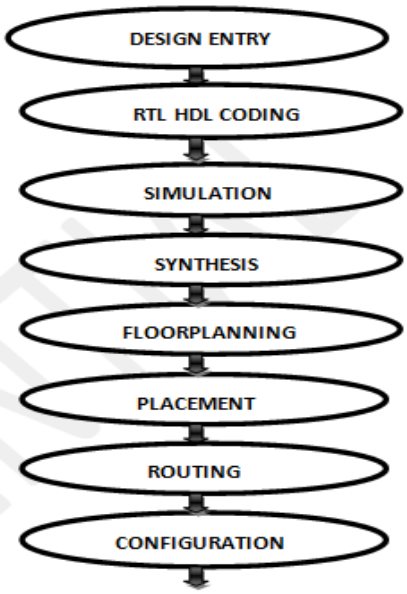
```
module exa_hz_clock_tb;
  // signal ios
  reg ref_clock;
  wire exa_hz_clock;
  // exahz clock generator RTL DUT instance
  exa_hz_clock ehz_c(ref_clock,exa_hz_clock);
  //clock toggling generator
  initial
    begin
      ref_clock = 1'b0;
      repeat(20)
        begin
          #5 ref_clock = ~ref_clock;
        end
    end
  // exahz clock generation display monitoring
  initial $monitor($time, "Exa hertz clock generation Exa_hz_clock = %b", exa_hz_clock);
  // dump signals
  initial
    begin
      $dumpvars;
      $dumpfile("dump.vcd");
    end
endmodule
```

III. EXA HERTZ PRBS DESIGN ARCHITECTURES



Description: The Above shown PRBS Generators of different Seed Word tapped element pattern sequences $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 are purely operated and synchronized with Exa Hertz Clock Frequency. These PRBS are design by using Linear Feed back shift register with different tapping elements(7,6),(10,3)(14,15)(18,23),(28,31) and these tapped elements are input the XOR gate for comparison and generate feedback output and connected to input of PRBS in looping fashion.The maximum number of seed words generates depends on the Maximum bit length of PRBS Design. Why We Designed the PRBS because it generates High Frequency Carrier waves to modulate low frequency base band signal for ultra high speed long distance wireless communication products/Applications. All these PRBS designs generate specific frequencies as per CCITT & ITU O.150/O.152 Standards.

IV. VLSI RTL DESIGN FLOW



Tape Out

4.1 Description: The Above shown VLSI RTL Design and FPGA Synthesis flow for Exa Hertz PRBS Designs. The following steps are

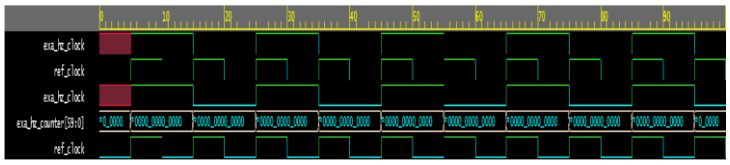
1. EXA Hertz PRBS RTL Design Entry
2. EXA Hertz PRBS HDL Coding done by Verilog HDL/VHDL
3. EXA Hertz PRBS Simulation done by Leading EDA Software Simulation tools(Synopsys VCS and Xilinx,Modelsim)
4. EXA Hertz PRBS HDL RTL Synthesis done by Xilinx FPGA Hardware Logic synthesis
5. EXA Hertz PRBS Floorplanning and Placement & Routing done by XILINX FPGA Synthesis
6. EXA Hertz PRBS CONFIGURATION by FPGA Xilinx.

I. RESEARCH METHODOLOGY

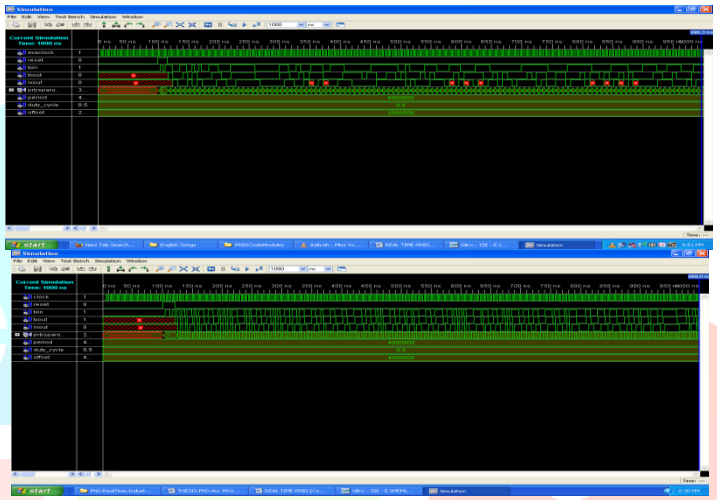
The research is based on the use of the RTL architecture for the identification of pseudo-random binary sequences. The prime benefits of using the RTL framework are the capability to provide accurate feedback on the predictions implemented on the binary sequences. The quality of the response will improve while the time of progression will be less consumed along with proper exploration of the data. RTL framework is a reliable, fast, multifaceted, and high-capacity predictive architecture that has an integrated data model having a multi-billion capacity of gates considering a full-chip hierarchical design. The progressive graphical user interface with cross-functional RTL architecture is valuable for impactful analysis (Largan et al., 2019) and
We have done Experimental Research Methodology using Leading EDA Software Automation Simulator Tools.

IV. SIMULATION AND SYNTHESIS RESULTS

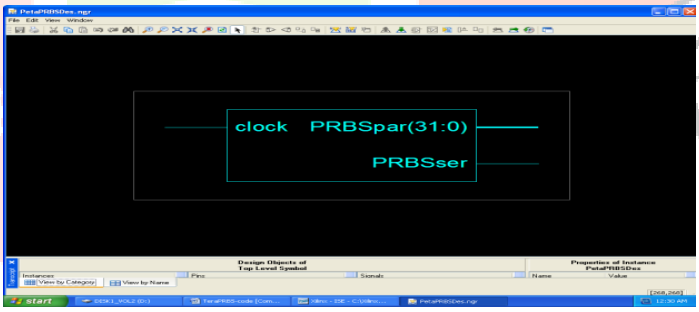
4.1 EXA HERTZ CLOCK GENERATOR



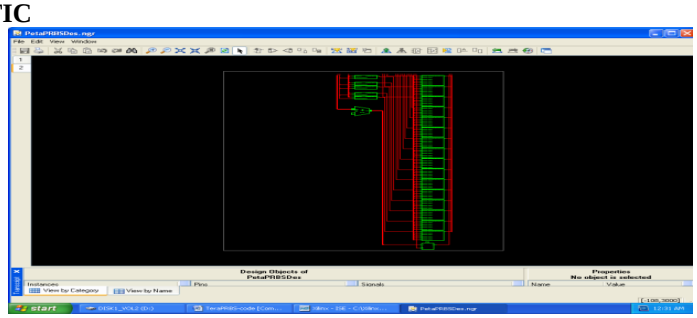
4.2. EXA HERTZ PRBS

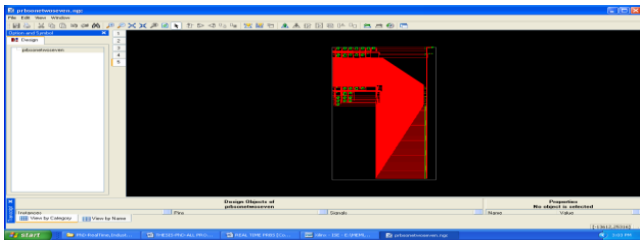


4.3 RTL DESIGN ARCHITECTURE

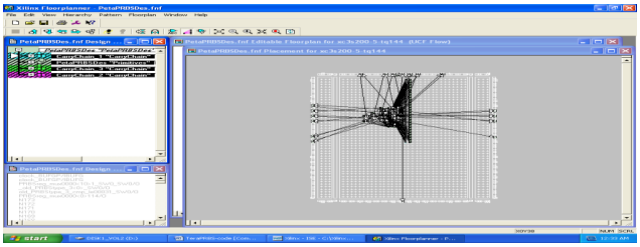


4.4 RTL-DESIGN-SCHEMATIC

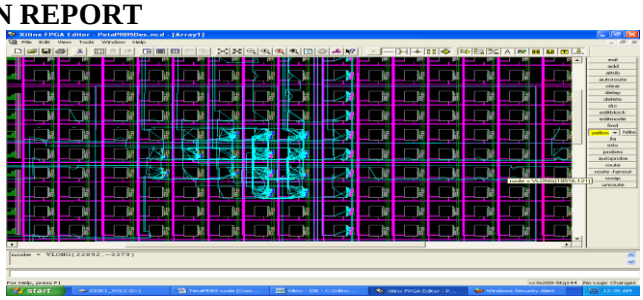




4.5: FPGA PLACED DESIGN LAYOUT



4.6: FPGA ROUTED DESIGN REPORT



4.7 EXA HERTZ CLOCK GENERATOR DISPLAY

Chronologic VCS simulator copyright 1991-2020
Contains Synopsys proprietary information.
Compiler version Q-2020.03-SP1-1; Runtime version Q-2020.03-SP1-1; Oct 23 04:37 2021
0Exa hertz clock generation Exa_hz_clock = x
5Exa hertz clock generation Exa_hz_clock = 1
15Exa hertz clock generation Exa_hz_clock = 0
25Exa hertz clock generation Exa_hz_clock = 1
35Exa hertz clock generation Exa_hz_clock = 0
45Exa hertz clock generation Exa_hz_clock = 1
55Exa hertz clock generation Exa_hz_clock = 0
65Exa hertz clock generation Exa_hz_clock = 1
75Exa hertz clock generation Exa_hz_clock = 0
85Exa hertz clock generation Exa_hz_clock = 1
95Exa hertz clock generation Exa_hz_clock = 0
V C S S i m u l a t i o n R e p o r t
Time: 100 ns

V. Acknowledgment

I Sincerely Thanks to Co-Author for Cooperation and Support of Tangible Research contribution on Software HDL based Exa Hertz PRBS Design.

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