



Load Current Ripple Reduction in Single Stage Single Switch High Power Factor Constant Current Switch Mode Power Supply

¹Ravi Sharma,²Abhishek Shrivastava

¹M.Tech Scholar, ²Assistant Professor

¹Department of Electronics and Communication Engineering

¹SRCEM, Gwalior, India

Abstract: This paper discusses the inherent problem of high ripple in load current of HPF type single stage single switch constant current SMPS. This SMPS topology widely used in modern LED control gear solution to achieve all critical parameters, like good line and load regulation, efficiency, high power factor, input current harmonics, surge immunity, EMI/EMC and we also achieve low cost of total solution. There are many advantages of this topology but on the other hand it comes with a big disadvantage of ripple in load current which causes the flicker (double line frequency) in light. In general, naked human eye cannot detect this flicker and that's why this topology is widely accepted by most of the light manufacturer.

However recent healthcare studies shows that this flicker can be detect by human brain and can cause human health problem like headache, eye strain, impaired visual performance. Camera can also detect this low frequency flicker during photography, where the images are cut with several black lines and it is not possible to properly shoot. This is the major concern from professional photographers, lighting design architect while designing a lighting design of a hotel, commercial building, monuments etc.

We will discuss a low cost solution to eliminate this low frequency flicker from load current so that we can resolve this big challenge of HPF type single stage single switch SMPS and do not increase product cost too much which make the product out of the pocket of customers.

Index Terms—LED, HPF, Flicker, EMI/EMC, Ripple, Surge.

I. INTRODUCTION

LEDs are always considered as a replacement of incandescent or fluorescent lamps since its inception but because of its low lumen output, it could not capture the light source in daily life. Many work has been done on the refinement of LEDs to make it real replacement to conventional lighting sources and today it has come true and LEDs has already taken a mass volume as a general lighting product in our routine life and gives advantages on high lumen/watt output, higher life cycle, easy to design compact and decorative lamps.

When LED product started taking place of light source that time the cost was a bigger challenge and these products were out of the pocket from consumer. Though LED products has many advantages over incandescent lamps but due to its higher cost they could not take the place of light source in our daily life. Hence there was a constant innovation was required to make the LED as a cost effective product and real replacement of light source in our daily needs.

LED products can be tearing down mainly in four components (Mechanical, Electrical, Optical and Thermal). In LED product electrical component was contributing significant cost in total product costing because of selected topologies that time to meet the different government regulations. Initially HPF two stage isolated topology were used to make the electronic control gear and then many manufacturers shifted to single stage LPF isolated topology which has the greater advantage over cost. Now a days manufacturer are using HPF type Non-isolated, HPF type isolated topology as per different product application (Indoor, Outdoor, Industrial, commercial, Residential). In general three topology are very famous Buck (Non-isolated), Buck-Boost (Non-isolated), Flyback (Isolated). All these three topology can easily meet product/government regulations like HPF, Harmonics, Lumen Efficacy, Control gear efficiency, long life cycle...etc. and have greater cost advantage on earlier used topologies.

As we know that all technology or innovation has advantages and disadvantages and the biggest disadvantage in HPF type single stage single switch topology is low frequency (double line frequency) ripple in load current. Which causes the flicker in LED of and also known as stroboscopic effect. However this flicker is acceptable because it is largely imperceptible and naked human eye cannot detect it. Recent studies shows that this flicker can be detect by human brain and can cause human health problem like Headache, Eye strain, impaired visual performance, or in extreme cases Epileptic seizure. It can also effect the LED source life cycle and other issues **during** photography or videography.

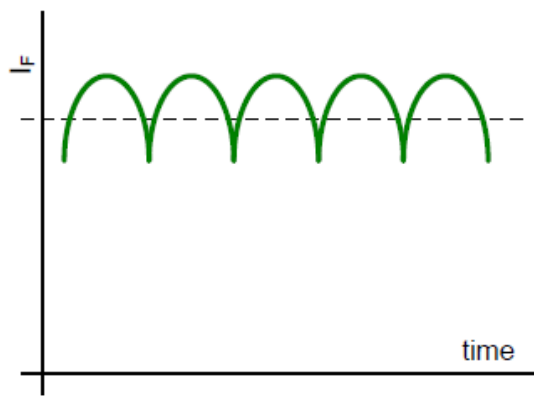


Figure 1 Ripple in Load Current

Measurement of Ripple content in load current

We have taken a HPF type single stage single switch isolated LED control gear to check the ripple content in load current at full load condition.

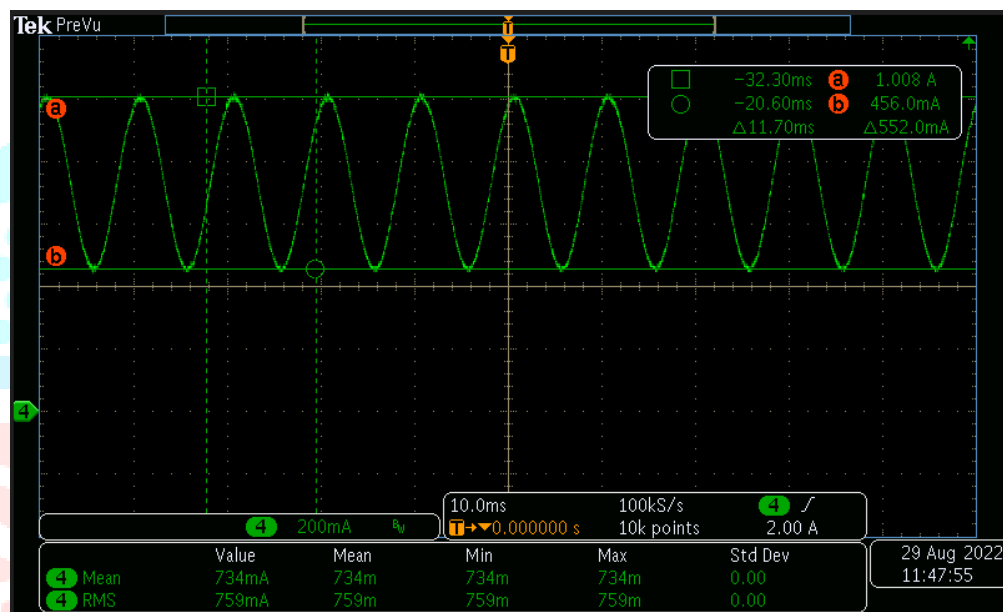


Figure 2. Ripple Measurement

We have used a digital phosphor oscilloscope to measure load current waveform in single stage single switch active power factor corrected constant current switch mode power supply. The following reading is taken from above Oscilloscope waveform.

- Mean Value of Load Current: 734mA
- RMS Value of Load Current: 759mA
- Upper Peak Value of Load Current: 1008mA
- Lower Peak Value of Load Current: 456mA
- Peak-to-Peak Value of Ripple in Load Current: 1008-456 = 552mA
- Percentage Value of Ripple in Load Current: 37.6%

$$\text{Ripple in load current (\%)} = \frac{\text{Peak to peak value of ripple in load current}}{2 \times \text{Mean value of laod current}} \times 100$$

Electrical Parameters measured of a Flyback converter

Table 1 Electrical Parameters measured of a Flyback converter

V_{IN} (VAC)	I_{IN} (A)	P_{IN} (W)	PF	I-THD	V_{OUT} (VDC)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (η)	Ripple in Load Current
100	0.345	34.5	0.992	4.7	38.2	0.768	29.4	85	39.8
230	0.139	31.8	0.990	3.3	38.0	0.734	27.9	88	37.6
300	0.107	31.5	0.976	5.4	37.9	0.721	27.3	87	38.0

We can see that the above electrical measurement table of Flyback converter (HPF single stage single switch) can meet all electrical parameters but the ripple content in load current is very high which causes the flicker in LED load.

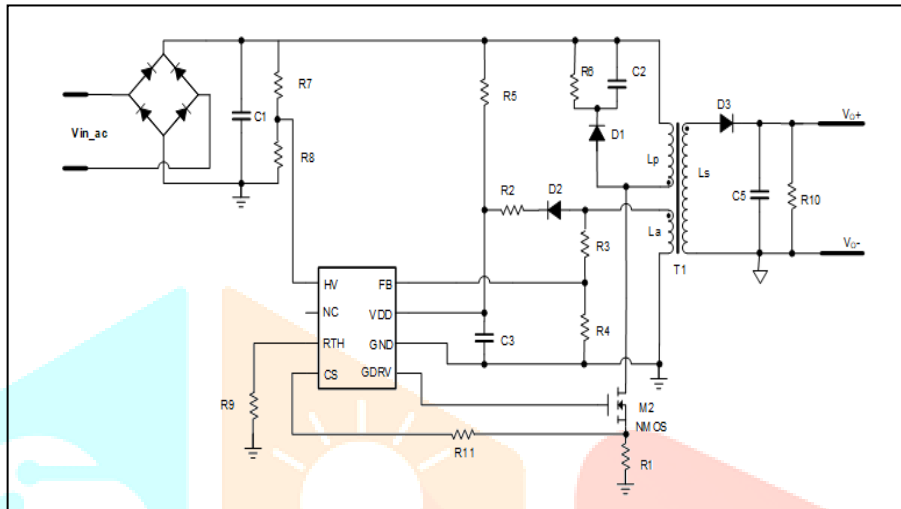


Figure 3 Typical Application of Flyback

To find the solution of the problem first we need to find the actual root cause of the issue and if we can find it then we can work to find a good solution also. We carried out few test to see the behavior of ripple content in load current.

1. We have increased the output filter capacitor value and then check the ripple current and found it has been improved (decrease). When decrease the output filter capacitor value and then check the ripple current and found it has been increased (Worse).
2. When put the different LED load which has different dynamic resistance than also found that the LEDs which has higher dynamic resistance has better ripple current behavior (Ripple current found less) and the LED load which has lower dynamic resistance has poor ripple current behavior (Ripple current found more)

To understand the behavior of more ripple current in LED load when the output filter capacitor value is less we need to understand the basic V-I characteristic of LED. As per V-I curve of LED we can see that small variation in LED forward voltage causes large variation in LED forward current. We have taken the example of V-I characteristic from Philips Lumileds Luxeon Rebel series LED datasheet which can refer in below given figure.

From the V-I characteristic of LED, it is easy to note that a slight variation in forward voltage is causing the large variation in forward current. Example: LED forward current 100mA is at forward voltage of 2.7V and forward current 1000mA is at forward voltage of 3.3V. It means around 600mV variation in forward voltage is causing large variation in forward current which is increased by 10 times of initial value.

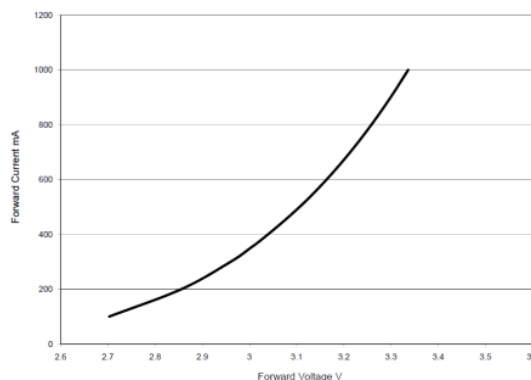


Figure 4 LED V-I Characteristic (Lumiledes)

Now we'll observe the voltage and current waveform at the output of Flyback converter. We can see that there is a small amount of AC component (sine wave) in DC output voltage and variation in LED current is in the same phase but amplitude is large comparatively to voltage. It is because of basic characteristic offered by LED.

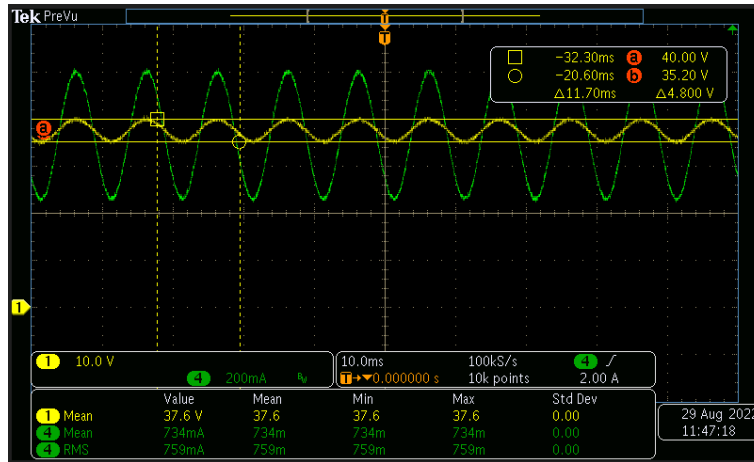


Figure 5 Actual measurement of ripple content in load voltage and load current

Yellow color waveform is showing the output voltage and green color waveform is showing output current of a Flyback converter. So, we can conclude that the variation in forward voltage of LED string is the reason of large ripple current.

II. LITERATURE SURVEY

Fang, Peng, et al. [1] in his paper had proposed a ripple cancellation technique, where resistors used for signal conditioning are within 0.5% tolerance, so that AC ripple amplitude can be set in a precise way, Op Amps used are within 120Hz frequency signal, TLV274CDR (TI) is used to reduce static power consumption and BOM cost. A method to minimize the ripple current while also maintain a small output capacitance is proposed in [2-3]. Barwar, Manish Kumar, et al. [4] had proposed RC method to remove ripple and eliminate the electrolytic capacitor. A multilevel converter topology is used to maintain UPF and reduces the voltage stress across the switches. This method decouples the output voltage control and multilevel converter, which further eliminates the impact of the load on converter and UPF. The peak efficiency of the converter has been noted as 89%.

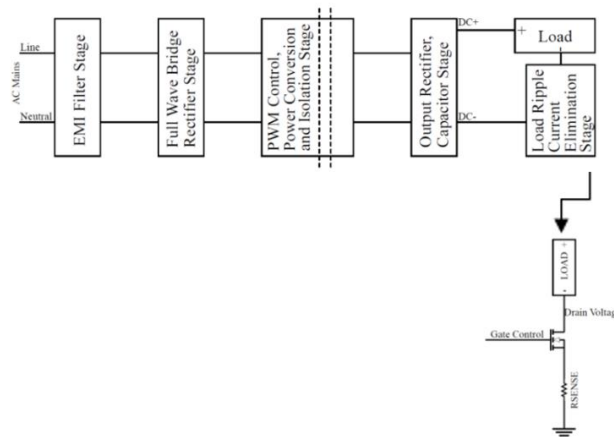
III. PROPOSED SOLUTION ARCHITECTURE/SCHEMATIC

As explained above we can say that the variation in forward voltage of LED string is causing the large variation in LED current and which can be seen as a ripple content in output current.

If we can find some way which can help to keep the string voltage constant than we will be able to control variation in LED current in a better way. There could be some way like increasing output capacitor value, Increase output bleeder resistance value, increasing dynamic resistance value. To slow down discharging of output capacitor by adding fix resistance to LED string. We can discuss the above solution disadvantages in brief.

1. Increasing output capacitance will cause large system startup time, more space, high cost
2. Increasing output bleeder resistance will cause slow discharge of capacitor which can create issue in factory processes
3. Increasing dynamic resistance of LED. Higher dynamic resistance LEDs have higher dissipation in package which creates thermal challenge and lumen depreciation and working life
4. Adding fix resistance cause direct power dissipation loss which creates thermal challenge and product life cycle

We can design a circuit which can adjust the load negative terminal in phase to the ripple content in load current (Try to maintain constant voltage across the load) which will help to reduce ripple content in LED current by a great extent. If we can bring down the LED current ripple $\leq 5\%$ than it will difficult to capture it in camera and it also reduced the human health concern by a great extent. Below figure shows the block diagram of proposed solution.



IV. WORKING PRINCIPLE

The above block diagram is showing the basic version and not showing the gate control section and will discuss the basic principle of eliminating ripple content from load current. We will discuss gate control section further in below given block diagram of our proposed solution.

Basically we are trying to replicate the same ripple voltage of load across the active switch (Between Drain and Source terminal of N-MOSFET) used in above block diagram so that load can see the constant potential difference. When we say that load is experiencing constant potential difference it means that load is seeing voltage without any ripple content in it. It means ripple content already eliminated from load voltage which is causing load current without any ripple content in it.

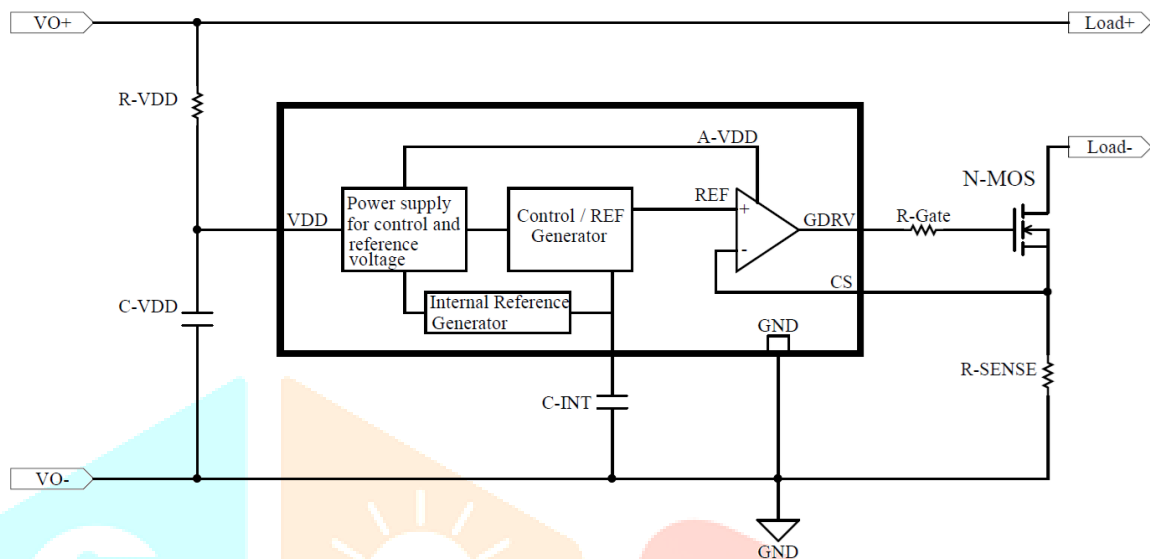


Figure 6 Block Diagram of proposed solution

Table 2 Components and their name

S.No.	Name	Function
1	R-VDD	Resistance to limit current internal power supply section (10kΩ ~ 50kΩ)
2	C-VDD	Capacitor which help to hold charge for power supply section (1μF ~ 4.7μF)
3	VDD	Internal power supply section input
4	C-INT	External Integration capacitor
5	GND	Ground
6	GDRV	External MOS Gate Drive
7	R-Gate	Current limiting resistance in gate section of external MOS (1Ω ~ 10Ω)
8	CS	Load current sense input
9	R-SENSE	Load current sense (shunt) resistance (0.1Ω ~ 5Ω)
10	N-MOS	N channel MOSFET (BVDS ≥ Open Circuit Voltage of Flyback converter)

Now we will discuss here the gate control mechanism of the proposed solution. In above block diagram of proposed solution we can see that there is a control signal block which is trying to replicate the same ripple voltage envelope across the capacitor used at C-INT location with the help of fix internal reference generator. This capacitor is working as an integrator and generating a reference voltage to the current regulator section. Current regulator is sensing the actual load current using a shunt resistance at R-SENSE location. Current regulator will control the N-MOS gate voltage in a way that it replicate the same voltage across R-SENSE location as compare to reference voltage generated by the integration capacitor located at C-INT location. So we can say that the voltage across R-SENSE is same as to internal reference voltage generated by integration capacitor at C-INT location. Since internal reference voltage which is generated by capacitor at C-INT location is similar and in same phase to the ripple voltage between terminal Load+ and GND so the voltage will also be the same and similar across R-SENSE. We can derive below equation.

$$V_{SENSE} = I_{Load} \times R_{SENSE} = V_{ref-CAP}$$

Since drain is connected to the load negative terminal hence load negative terminal potential is getting driven in similar way as drain is getting driven. It means load negative terminal is also seeing the same ripple content as load positive terminal is seeing. It means that the potential difference between load positive and load negative terminal will always remain constant, because we are able to keep potential difference constant between load positive and negative terminal it means load is not having any ripple content in load voltage and this is causing a constant current flow through the load without having any ripple content in it.

V. SIMULATION RESULT

Now we built the complete system using first stage as a flyback converter and second stage as a ripple elimination circuit and took the electrical parameters of the board than below simulation results were observed

Table 3 Electrical parameter of simulation results

V_{IN} (VAC)	I_{IN} (A)	P_{IN} (W)	PF	I-THD	V_{OUT} (VDC)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (η)	Ripple in Load Current
100	0.355	35.73	0.998	4.8	37.84	0.767	29.02	83	2.1
230	0.144	32.24	0.991	3.3	37.69	0.733	27.63	86	2.2
300	0.110	32.38	0.977	5.4	37.54	0.720	27.03	84	1.7

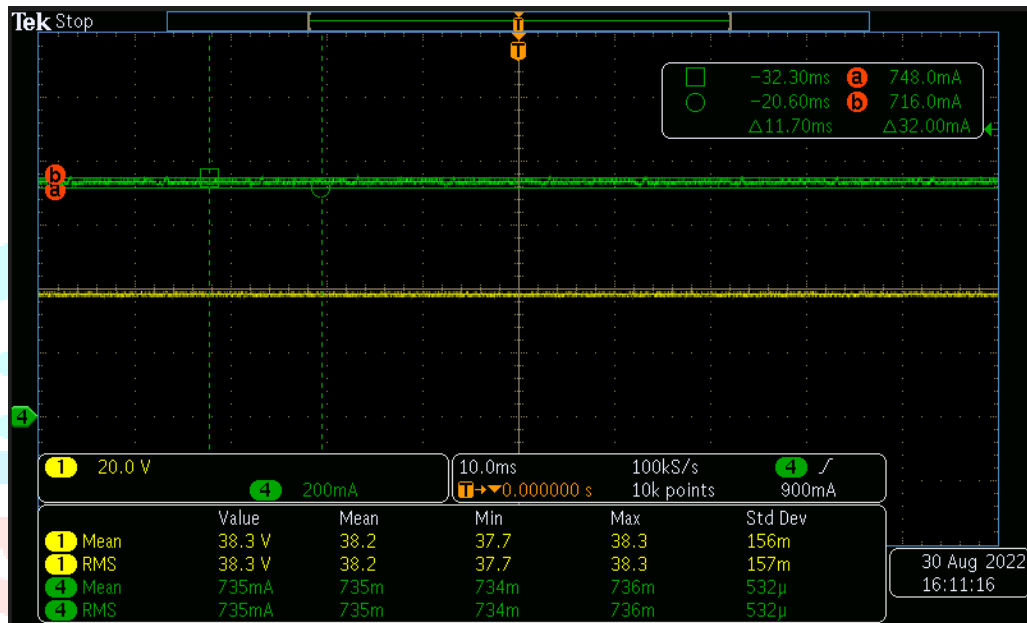


Figure 7 Simulation result

Green color waveform is showing the current in load and yellow color waveform is showing the potential different between load+ and load- terminal.

- Mean Value of Load Current: 735mA
- RMS Value of Load Current: 735mA
- Upper Peak Value of Load Current: 748mA
- Lower Peak Value of Load Current: 716mA
- Peak-to-Peak Value of Ripple in Load Current: 748-716 = 32mA
- Percentage Value of Ripple in Load Current: 2.2%

$$\text{Ripple in load current (\%)} = \frac{\text{Peak to peak value of ripple in load current}}{2 \times \text{Mean value of load current}} \times 100$$

It is clearly visible from above simulation result of complete system (Flyback converter + Ripple elimination stage) and by doing waveform analysis of load voltage and load current that the ripple content which was present earlier has been eliminated by an great extent and now we can see the output current as a pure DC current instead of earlier DC current with 100Hz AC component in it.

This new stage is helping us not only to remove ripple from load current but the total implementation cost is also very less comparatively to earlier proposed solution with two power conversion stage. Hence we can now continue to use single stage single switch flyback converter and can take all the benefit of this topology. Where low ripple load current is required we can built this small stage after the output stage of flyback converter. This circuit is very simple and easy to implement and it also required very less space and because of this it can be used as a separate module too.

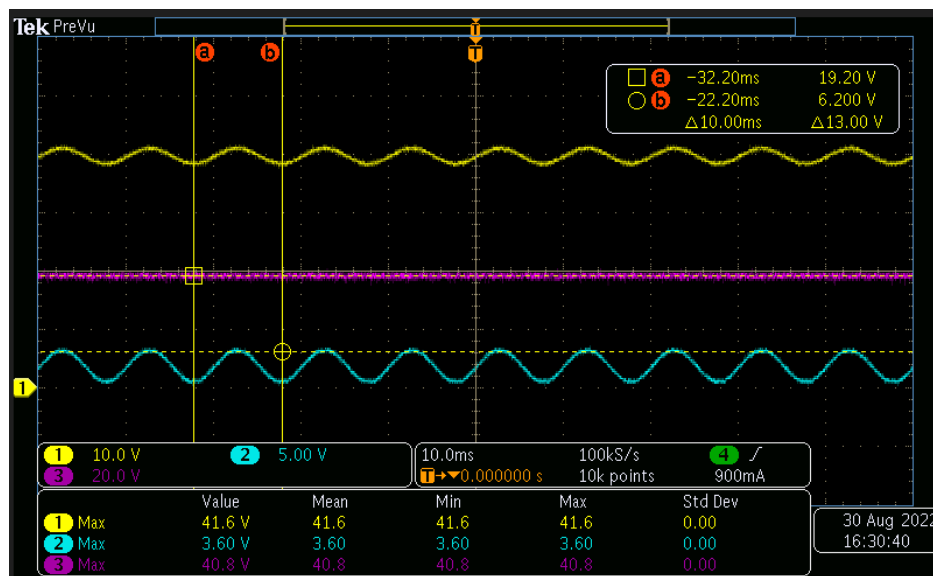
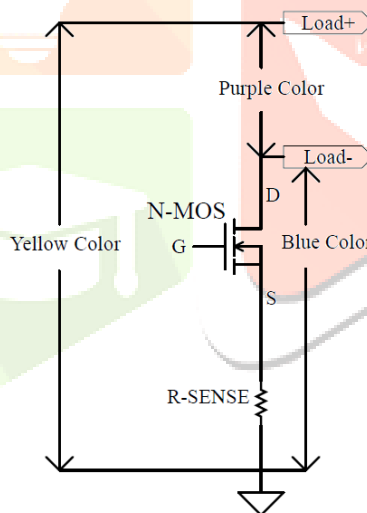


Figure 8 Simulation result

The above waveform analysis is done to find out the potential difference between load positive terminal and GND terminal, Potential difference between drain and source terminal of active switch (N-MOS), and potential difference between load positive and load negative terminal.

Please refer below given color code to see voltage between different terminals.

- Yellow Color – Showing potential difference between load positive terminal and ground terminal
- Blue Color – Showing potential difference between drain and source terminal of active switch (N-MOS)
- Purple color – Showing potential difference between load positive terminal and load negative terminal



From the waveform analysis between different terminals, it is clearly visible that the potential difference between load positive and load negative terminal is constant and load is experiencing almost negligible ripple content in voltage across it. Constant load voltage is helping to reduce ripple content in load current by a great extent.

VI. CONCLUSION

The study of our solution in this paper shows that we have achieved a very good solution for removing ripple content from load current in single stage single switch high power factor constant current switch mode power supply. From the given block/schematic diagram of our solution we can find that the cost of this complete solution is very less and negligible increase in total system cost. Which help us to easily consider single stage high power factor constant current power supply with this ripple elimination circuit. By using this system architecture we can easily achieve high power factor, good input current THD and on the other hand we can also eliminate ripple content in load current by great extent. In our test circuit of 30W power supply we have achieved good ripple current 2.2% which was earlier 37.6% (without ripple elimination circuit) and also achieve good system efficiency greater than 85% at typical input voltage. Which is a good proposition with respect to “system complexity in design Vs system cost Vs product form factor” [4].

Below given table can be referred for a comprehensive view to look at the pros and cons of different topologies of power converter. We can see that using ripple elimination circuit in conjunction with single stage high power factor (APFC) topologies gives the best result in different aspects.

Table 4Pros and cons of different topologies of power converter

Topology	Line Regulation	Load Ripple Current	I-THD	Power Factor	Efficiency	Cost Idea
Active PFC + Flyback (Two Stage)	Best	Best	Best	Best	Better	High
Active PFC + Buck (Two Stage)	Best	Best	Best	Best	Better	High
LPF Flyback + Passive PFC	Better	Poor	Poor	Good	Good	Medium
LPF Buck + Passive PFC	Better	Poor	Poor	Better	Better	Low
Active PFC Flyback (Single Stage)	Good	Poor	Better	Better	Best	Low
Active PFC Buck (Single Stage)	Good	Poor	Poor	Better	Best	Very Low
Active PFC Flyback + Ripple Elimination	Good	Better	Better	Better	Better	Medium
Active PFC Buck + Ripple Elimination	Good	Better	Poor	Better	Best	Low

The above study of our solution shows that we have achieved a very good solution for removing ripple content from load current in single stage single switch high power factor constant current switch mode power supply.

REFERENCES

- [1]Fang, P., White, B., Fiorentino, C., & Liu, Y. F. (2013, September). Zero ripple single stage AC-DC LED driver with unity power factor. In 2013 IEEE Energy Conversion Congress and Exposition (pp. 3452-3458). IEEE.
- [2]Ruan, X., Wang, B., Yao, K., & Wang, S. (2010). Optimum injected current harmonics to minimize peak-to-average ratio of LED current for electrolytic capacitor-less AC-DC drivers. *IEEE Transactions on Power Electronics*, 26(7), 1820-1825.
- [3]Hu, Q., & Zane, R. (2010). Minimizing required energy storage in off-line LED drivers based on series-input converter modules. *IEEE Transactions on Power Electronics*, 26(10), 2887-2895.
- [4]Barwar, M. K., Sahu, L. K., Bhatnagar, P., Gupta, K. K., & Chander, A. H. (2020, October). A Decoupled Low-Frequency Ripple Cancellation Method for High-Power LED Driver circuits. In *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society* (pp. 3597-3602). IEEE.

