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Power And An Efficient Area Aware Improved Sqrt Csla

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Abstract: Speed, area and power are the main parameters of modern day's devices. Adders are the main component of all digital devices and play a crucial role in signal processing. There are different types of adder for different type of work and environment. Time by time new adders was invented to minimize the basic problems i.e. Speed, Area and Power. Among them Carry Select Adder is the most trending area of research. All the work that has been done on adder is to optimize three parameters mentioned earlier. CSLA has better performance regarding propagation delay. In this paper we have discussed about different types of basic adder and then briefly described about different types of Carry Select Adder (CSLA). Later we have proposed a modified SQRT model changing its sequence and the whole comparison has been carried out in Xilinx 14.5 ISE environment and coded using Verilog HDL.

Key factor: Speed ,Area, SQRT, CSLA, HDL, Adder.

Introduction

As a fundamental operation, addition is the basis of complex digital signal processing. The delay and power consumption of a multi-bit adder usually determines the performance and power consumption of arithmetic circuits. For practical applications, the adder should feature high speed and low power consumption [1]. A conventional ripple carry adder (RCA) adopts a cascade structure of multiple full adders, which has a small area and low power consumption. The main concern of the RCA is the carry propagation delay, which severely limits the speed of the system. A carry select adder is one of the most efficient methods to reduce the carry propagation delay of multi-bit adders [2].

A conventional CSLA consists of a pair of RCA–RCA, the carry inputs of the two RCAs are assumed to be 0 and 1, respectively, and the correct sum and carry output are selected according to the actual carry input. It is clear that the conventional CSLA has a smaller carry propagation delay than RCA, but a pair of RCA leads to a larger area and power consumption. Many optimizations have been adopted in previous works to make CSLA more attractive. In Reference [3], a square-root (SQRT) method was adopted to implement large bit-width adders to decrease the delay. The CSLAs with increasing bit widths are connected by cascade structure in SQRT CSLA. The purpose is to provide a parallel computing path for carry propagation and reduce the delay of the adder. In Reference [4], an adder and an add-one circuit were used to replace two RCAs in conventional CSLA, so as to reduce the area of CSLA. A new add-one circuit based on "first" zero detection logic and several multiplexers were proposed in Reference [5] to reduce the power and area with negligible speed penalty. Ramkumar and Kittur [6] proposed a Binary to Excess-1 Converter (BEC) CSLA, the BEC-based structure reduces logic redundancy, thus reducing area and power consumption. But the increased BEC logic will slightly increase the delay of the adder. In Reference [7], the reduction of area using the BEC-based approach was further verified. In Reference [8], the BEC logic was replaced using

common Boolean logic to reduce the area and power consumption. In Reference [9], a CSLA without using a multiplexer for the final selection was proposed, the approach used the implementation of cin = 0 adder and then Excess 1 adder. Since the multiplexer is an important part of the CSLA and in the critical path, removing the multiplexer could reduce the area and propagation delay of the CSLA. In Reference [10], area-efficient CSLA was proposed by modifying the full adder design. The full adder was implemented using a XOR, NOT, AND and OR gates, and the logic for the required carry was selected using a multiplexer. Logic optimization in Reference [11] provided a separate carry generator for the final carry bit of each block in the SQRT CSLA. The area and power consumption of the CSLA was reduced by the logic optimization compared with regular CSLA. In Reference [12], a high-speed CSLA was proposed based on the pivotal feature that the final-sum was calculated before the calculation of the final-carry, as a result, the propagation delay was reduced. By modifying the logic formulations of the carry generation and selection scheme, as well as merging all the redundant logic operations in the carry generation and carry selection units, the CSLA in Reference [13] achieved a higher area and power efficiency. A high-speed, energy efficient CSLA dominated by carry generation logics was proposed in Reference [14] and the CSLA achieved similar power and area efficiency to BEC-based CSLA with a smaller delay.

All of the above CSLAs solve the large propagation delay problem in RCA which is due to the long carry chain, but all of them greatly increase the area and power consumption compared with RCA, which greatly limits the application of these CSLAs. Most of the strategies above are meant to reduce redundancy by optimizing logic, for example, by retaining one set of RCAs and replacing the other with some logic to reduce the area and power consumption. But actually, the design of the underlying adder suitable for the CSLA operation can optimize the area and power consumption of CSLA to a greater extent, so that the area and power consumption of the CSLA can be comparable to the RCA. In this work, transistor-level optimization was adopted to significantly reduce the area and power of the CSLA with little delay penalty. A dual carry adder composed of an XOR/XNOR cell and two pairs of sum-carry cells was proposed. Both CMOS logic and a transmission gate were applied to the dual carry adder cell to achieve fast and energy efficient operation. By sharing common logic as much as possible and transistor-level optimizations, the area and power of the proposed CSLA were significantly reduced compared with regular SQRT CSLA.

II. SQRT CSLA using BEC:

The main drawback of conventional CSLA is it is not area efficient. As a solution an (n+1)-bit Binary to excess 1 converter is used instead of n-bit RCA with Cin=1, it reduces the effective area with a slight increase in delay. Then the area count of group2 is determined as follows:

Gate count = 43 (FA + HA + Mux + BEC) FA = 13 (1 * 13)
HA = 6 (1 * 6)
Mux = 12 (3 * 4)
NOT = 1
AND = 1
XOR = 10 (2 * 5)
BEC (3-BIT) = NOT + AND + XOR = 12

Rest of all working principle is same as conventional CSLA. Above Equations present the logical operations relevant to the BEC

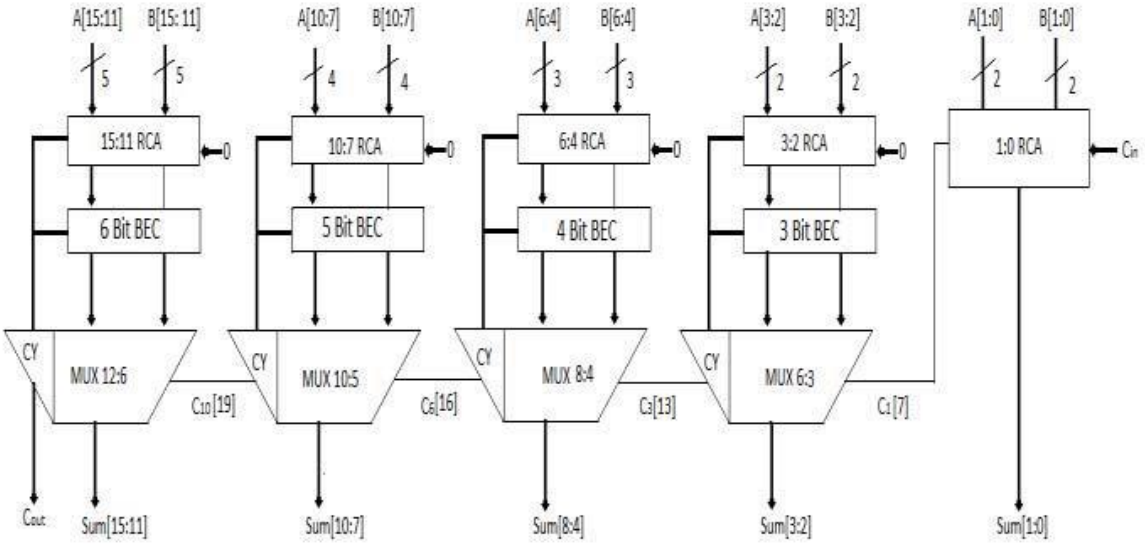


Fig 1. SQRT CSLA using BEC

III. Modified CSLA without using Multiplexer

In this model instead of CSLA with Cin=1 and multiplexer, we use some simple combinational circuit which subsist of AND and XOR gates . The circuit diagram of modified CSLA without MUX is given in Fig.2. In first stage the addition operation is done by RCA with the input Cin=0 and the output of the full adder is propagated through the combinational circuit (using AND and XORgates) with an input of previous stage's carry which will lead to final output.

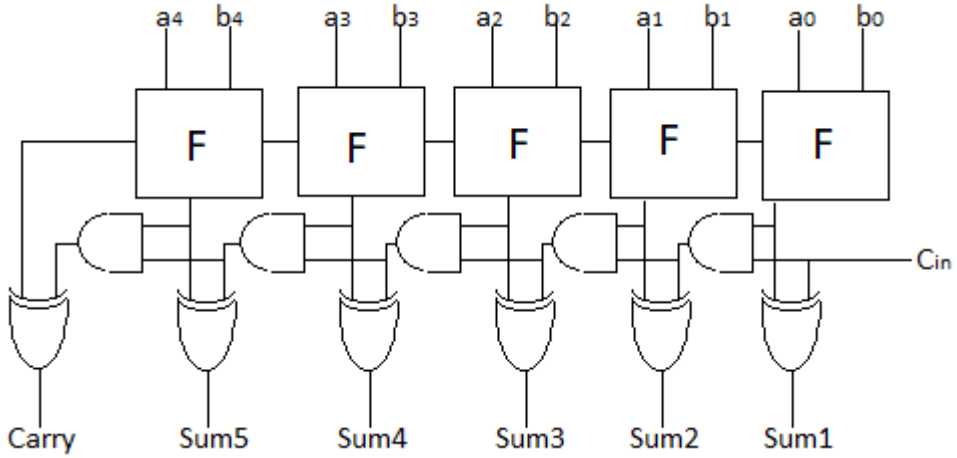


Fig.2 Modified CSLA without using Multiplexer

IV. PROPOSEDMETHOD

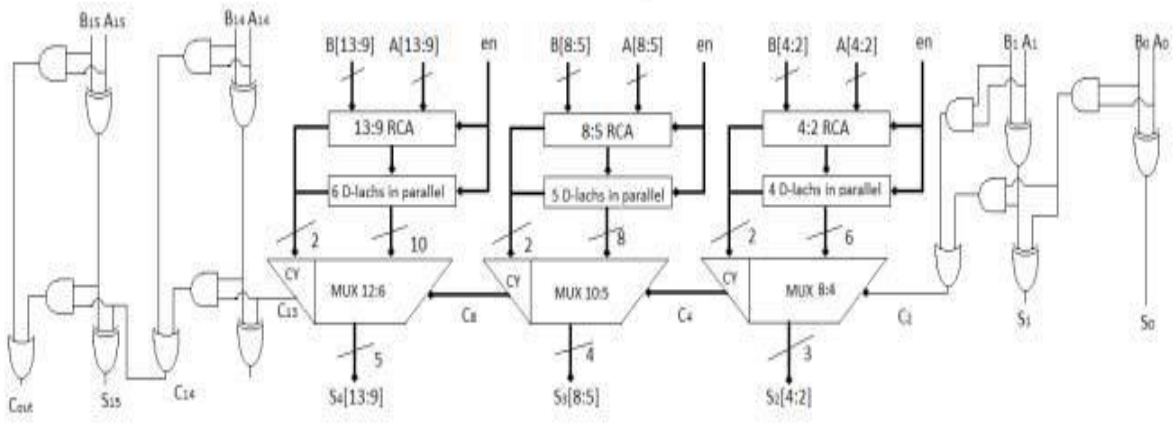
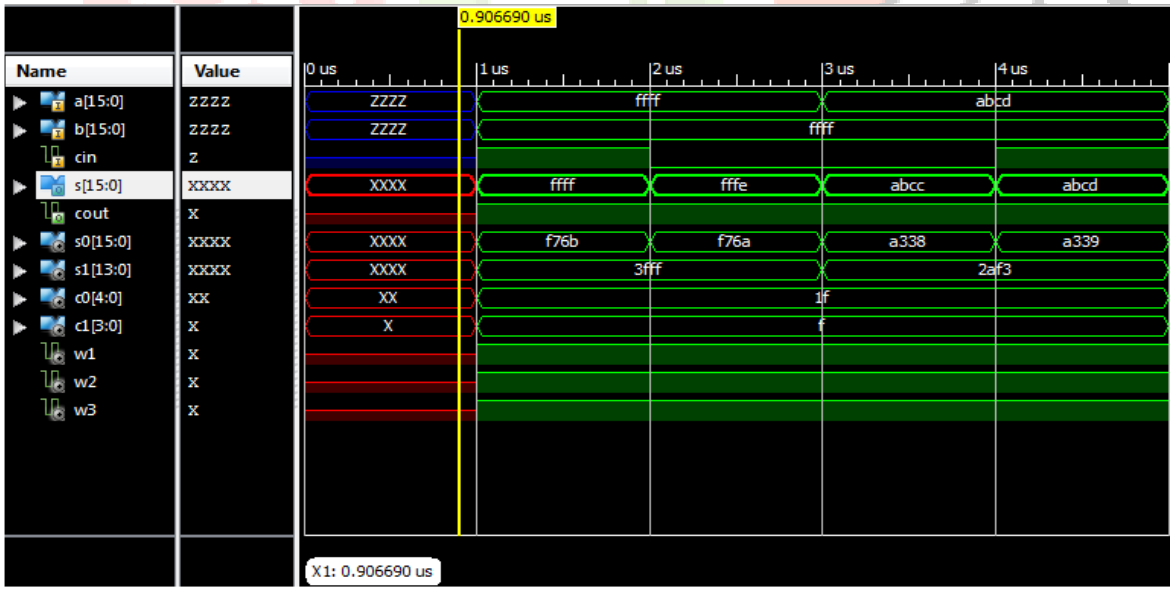


Fig.3 Proposed 16-bit CSLA adder

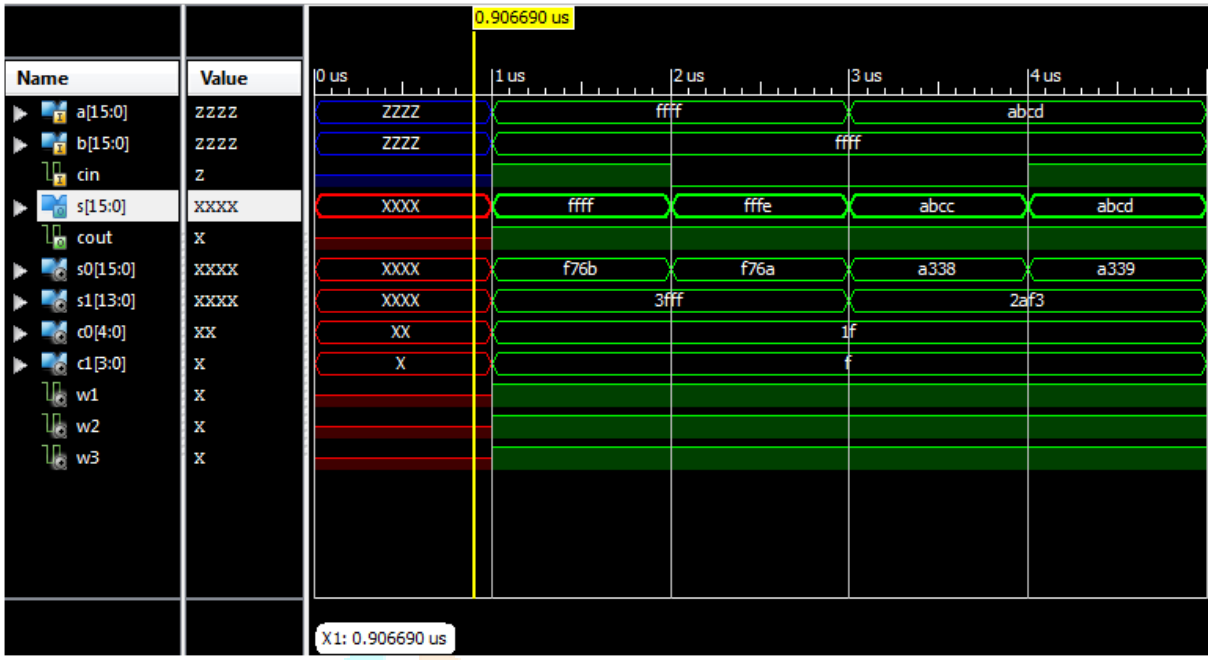
As we already discussed earlier that we are mainly focusing on to reduce the chip area and power consumption of the circuit. These two problems mainly occur due to circuit complexity or increasing of transistor number. In carry select adder we use MUX circuit to select the perfect carry. In basic adder section we have shown that for every MUX gate count is 3. SQRT model shows a circuit sequence for effective result. But main drawbacks of that circuit were its area and power consumption. It needs 4 MUXs to design a 16-bit CSLA adder. So we just modify that circuit and make it using 3 MUXs. The circuit has been shown in Fig 3. For conventional CSlA circuit we have

Gate count = 57 (FA + HA + Mux) FA = 39 (3 * 13)
HA = 6 (1 * 6)
Mux = 12 (3 * 4).
Now we have made the same adder having
Gate count = 54 (FA + HA + Mux) FA = 39 (3 * 13)
HA = 6 (1 * 6)
Mux = 19 (3 * 3)

V. RESULTS: **CSLA 16 BIT OUTPUT**



PROPOSED CSLA OUTPUT



Delay Power Area
Conventional CSlA : 4.84 35.631 2016.09
Proposed : 2.98 27.458 1756.06

VI. CONCLUSION

In this paper we have briefly describe about different type of basic adders and made a comparison between them. Later we have discussed about different type of Carry Select Adder (CSlA). We have proposed a modified SQRT D-latch circuit design and have been tasted in Xilinx ISE 14.5 environment coded in Verilog HDL. Result shows that the Chip area and Power consumption is less than the other. For 16 bit operation our circuit is 6.28% more efficient with respect to power consumption and has 7.62% less chip area. This is the initiative step toward low area and power consumptive high speed adder. Now we are working on to minimize the propagation delay which arise due to modification of that circuit.

References

1. Balasubramanian, P.; Mastorakis, N. Performance Comparison of Carry-Lookahead and Carry-Select Adders Based on Accurate and Approximate Additions. Electronics **2018**, 7, 12.

2. Mohanty, B.; Patel, S. Area–Delay–Power Efficient Carry-Select Adder. IEEE Trans. Circuits Syst. II Exp. Briefs **2014**, 61, 418–422.
3. He, Y.; Chang, C.-H.; Gu, J. An area-efficient 64-bit square root carry select adder for low power application. In Proceedings of the 2005 IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, Japan, 23–26 May 2005
4. Kim, Y.; Kim, L.-S. 64-bit carry-select adder with reduced area. Electron. Lett. **2001**, 37, 614–615.
5. Rawat, K.; Darwish, T.; Bayoumi, M. A low power and reduced area carry select adder. In Proceedings of the 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002, Tulsa, OK, USA, 4–7 August 2002.
6. Ramkumar, B.; Kittur, H. Low-power and area-efficient carry-select adder. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **2012**, 20, 371–375.
7. Priya, R.; Kumar, J.S. Enhanced area efficient architecture for 128 bit Modified CSLA. In Proceedings of the 2013 International Conference on Circuits, Power and Computing Technologies (ICCPCT), Nagercoil, India, 20–21 March 2013.
8. Manju, S.; Sornagopal, V. An efficient SQRT architecture of carry select adder design by common Boolean logic. In Proceedings of the 2013 International Conference on Emerging Trends in VLSI,

Embedded System, Nano Electronics and Telecommunication System (ICEVENT), Tiruvannamalai, India, 7–9 January 2013.

9. Kumar, U.S.; Salih, K.K.M.; Sajith, K. Design and implementation of Carry Select Adder without using multiplexers. In Proceedings of the 2012 1st International Conference on Emerging Technology Trends in Electronics, Communication & Networking, Gujarat, India, 19–21 December 2012.
10. Rahul, C.G.; Saraswathi, N. Implementation of an efficient 64-bit Carry Select Adder using Muxes. In Proceedings of the 2014 IEEE International Conference on Advanced Communications, Control and Computing Technologies, Ramanathapuram, India, 8–10 May 2014.
11. Anagha, U.P.; Pramod, P. Power and area efficient carry select adder. In Proceedings of the 2015 IEEE Recent Advances in Intelligent Computational Systems (RAICS), Trivandrum, India, 10–12 December 2015.
12. Kumar, G.K.; Balaji, N. Reconfigurable delay optimized carry select adder. In Proceedings of the 2017 International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology (ICEEIMT), Coimbatore, India, 3–4 February 2017.
13. Bahadori, M.; Kamal, M.; Afzalikusha, A.; Pedram, M. An energy and area efficient yet high-speed square-root carry select adder structure. Comput. Electr. Eng. **2017**, 58, 101–112.
14. Nam, M.; Choi, Y.; Cho, K. High-speed and energy efficient carry select adder (CSLA) dominated by carry generation logic. Microelectron. J. **2018**, 79, 70–78.