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PERFORMANCE ANALYSIS OF FULL ADDER BASED ON CMOS AND DOMINO LOGIC TECHNIQUES

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ABSTRACT

Most devices in current VLSI technology are getting more portable, and efficient devices are the most extensively utilized. The Domino logic approach is widely used in the creation of small, fast circuits. In this study, a one-bit full adder circuit with CMOS logic and domino logic was developed in the Tanner Eda software using 0.18um technology and by providing different supply voltages their parameters are measured from the waveforms in T-Spice software. This study focuses on the creation of space-saving and fast-moving devices. This study compares the size, latency, and power consumption of CMOS and Domino logic based on full adder circuits. It was discovered that a Domino logic-based one-bit full adder circuit consumed less space and uses less power than a CMOS logic-based one-bit full adder circuit.

Keywords: Full Adder, Domino Logic, CMOS Logic.

I. INTRODUCTION

Transistor density is rising at an alarming rate in the fast developing VLSI sector. According to Moore's law, transistor density will double every eighteen months [1]. As the number of transistors rises, so will the device's size, latency, and power consumption. As a result, a solution to save space while enhancing device performance is required. For decades, CMOS technology has been used in the semiconductor industry to produce circuits, but as the number of transistors rises, so does the device area and delay [2,3]. As a result, it is vital to transition to a technology that takes up less space and has a lower latency. As a result, the Domino logic is utilized to generate the one-bit full adder, and several performance parameters in both technologies, such as area, latency, and power consumption, are compared.

II. MODELING AND ANALYSIS

CMOS logic

CMOS (Complement Metal Oxide Semiconductor) is a transistor logic utilizes p-MOS and n-MOS transistors, which operate as pull-up and pull-down transistors, respectively, as illustrated in Fig.1. When the input is low, the p-MOS is activated and charges the output node to Vdd when the input is high, the n-MOS is activated and the charge stored at the output node creates a conducting channel between the output node and ground. Both transistors are coupled in this case in a complementary manner, which means that when one is turned on, the other is turned off, and vice versa. The primary benefits of CMOS logic are its high noise margin, low power dissipation, and rail-to-rail output. There are certain downsides to CMOS logic, such as the necessity for a large surface area and the slow rate of operation. As a result, circuits with a high number of transistors take up a lot of space and run slowly. As a result, another technology that requires fewer transistors and runs at high speeds is required.

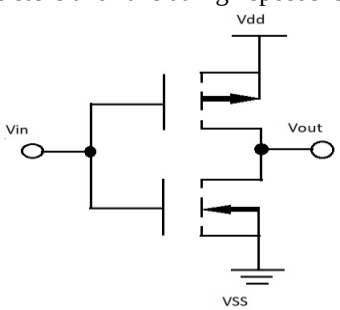

Fig 1. CMOS Logic

Domino Logic

Domino logic is an innovation in dynamic logic systems based on CMOS that use p-MOS or n-MOS for the pull down or pull up network. The Domino logic approach for generating full adders employs fewer transistors than conventional CMOS logic while producing high-performance devices [4-6]. There are various advantages of Domino logic like they have a smaller area unlike conventional CMOS logic, parasitic capacitance is smaller in domino logic so it provides high speed of operation and result is glitch free because each gate makes only one transition.

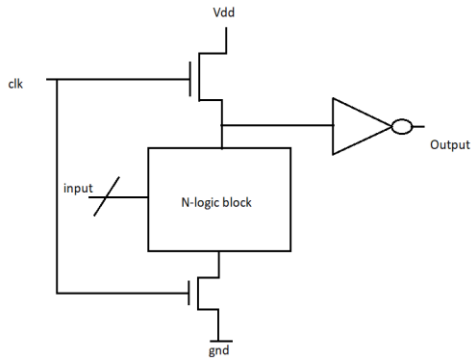

Fig 2. Domino Logic

Domino logic operates in two steps, the first being pre-charging and the second being evaluation. When the clock 'clk' is equal to zero or low, as shown in Fig. 2, the PMOS switches on and charges the output node to Vdd. The p-MOS is turned off when the clock reaches a high value, and the evaluation phase commences [7-9]. The configuration of the input determines the output during this phase. The output node may discharge if the inputs have a direct conducting link to ground; otherwise, it will remain high. As a result, the output of the circuit, mainly depends on the evaluation stage. In pre-charge phase, it will provide low output because we used an inverter in this logic style for cascading the next stage.

A digital circuit that performs numerical addition is known as an adder. Adders are employed in the arithmetic and logic units of calculators and computers. This circuit is fed three one-bit inputs denoted A, B, and C and two outputs: the sum and the carry.

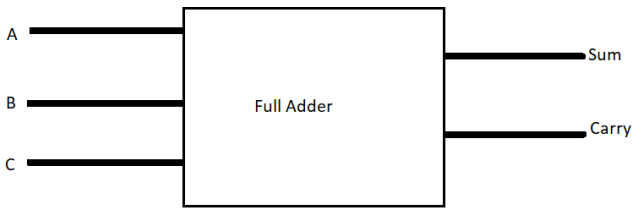

Fig 3. One-bit full adder block diagram

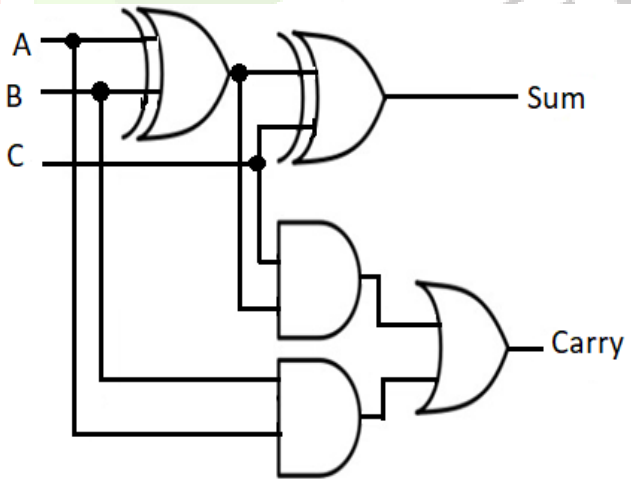

Fig 4. Logic diagram of one-bit full adder

The gate level logical diagram of a one-bit full adder, which uses two X-OR gates for sum, two AND gates, and one OR gate for carry, is shown above. The output of the two AND gates is fed into the OR gate, and the output of the OR gate is providing the carry of one-bit full adder. Table I shows the truth table for a full adder built using CMOS logic.

Table 1: Full Adder Truth Table

Inputs			Outputs	
A	**B**	**C**	**Sum**	**Carry**
Low	Low	Low	Low	Low
Low	Low	High	High	Low
Low	High	Low	High	Low
Low	High	High	Low	High
High	Low	Low	High	Low
High	Low	High	Low	High
High	High	Low	Low	High
High	High	High	High	High

Figure 5 displays a CMOS logic-based architecture of a one-bit full adder. Based on the input values, this circuit uses 14 p-MOS Transistor to charge the output capacitance and 14 n-MOS transistors to discharge the output node [9-10].

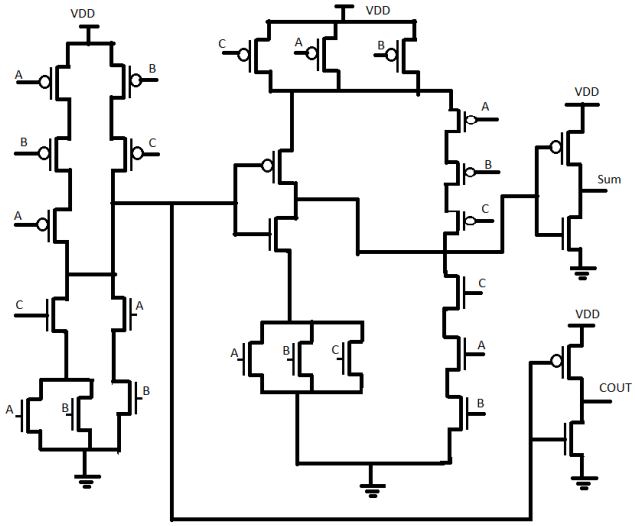

Fig 5: One-bit full adder using CMOS Logic - 28 Transistors

In order to build a one-bit full adder using CMOS logic, a total of 28 transistors are needed. Because of the large number of transistors involved, designing a one-bit full adder is highly difficult and complicated. As we can see, a large number of wires are required to connect the transistors, which adds substantial delay to the circuit.

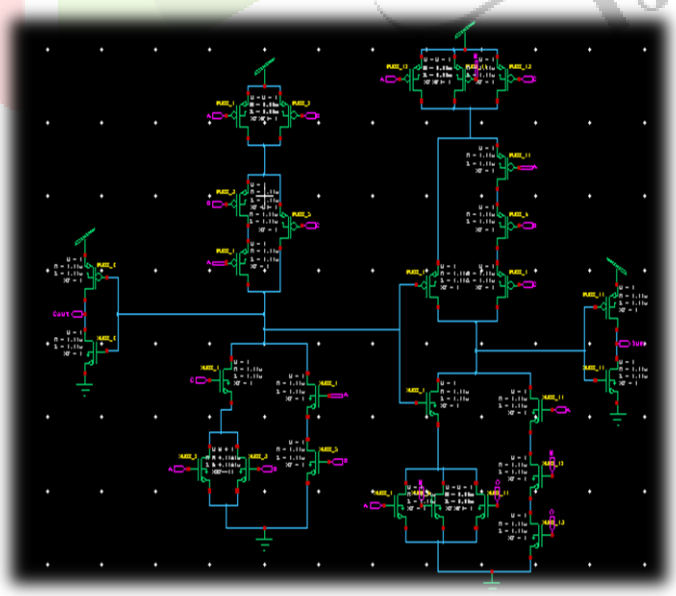

Fig 6: Schematic of one-bit full adder using Tanner software (CMOS Logic)

Design of a one-bit full adder based on Domino logic: A schematic for a one-bit full adder based on Domino logic is provided. We utilized p-MOS transistors for the pre-charge phase and inverter, and n-MOS transistors for the rest of the evaluation phase to create the one-bit full adder using domino logic [11-12].

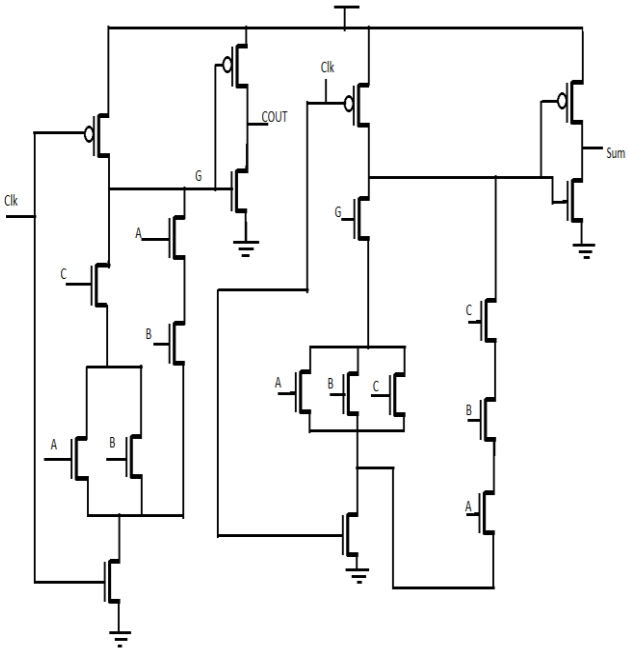

Fig 7: One-bit full adder using Domino Logic - 20 Transistors

We employed four p-MOS transistors and sixteen n-MOS transistors in this logic architecture. So, utilizing Domino logic, a total of 20 transistors are employed to create the adder circuit.

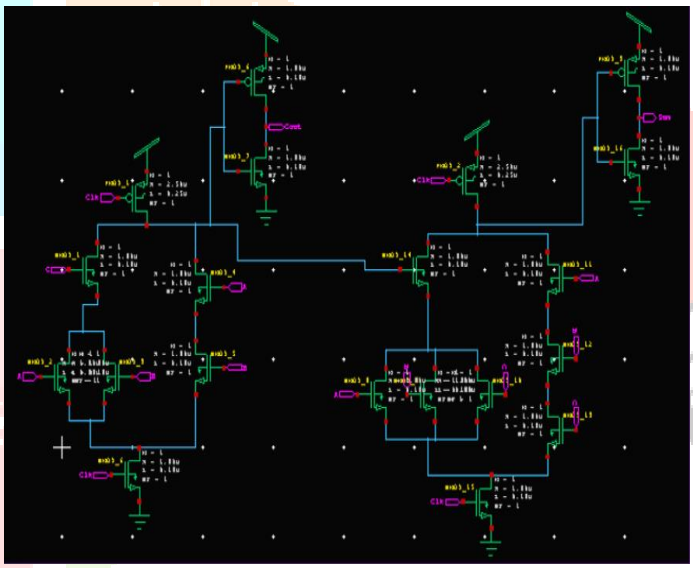

Fig 8: Schematic of one-bit full adder using Tanner software (Domino Logic)

III. RESULTS AND DISCUSSION

The CMOS logic circuit represented in Fig. 5 is used to analyze a full adder, and the results are validated using the full adder's truth table. Figure 9 displays the results of the transient analysis of the full adder circuit, which confirms the truth table. When the input has an odd number of high states, the output 'SUM' is high; otherwise, it is low. When two or more input states are high, the output 'CARRY' is also high. After getting an accurate result, we calculated the circuit delay and power.

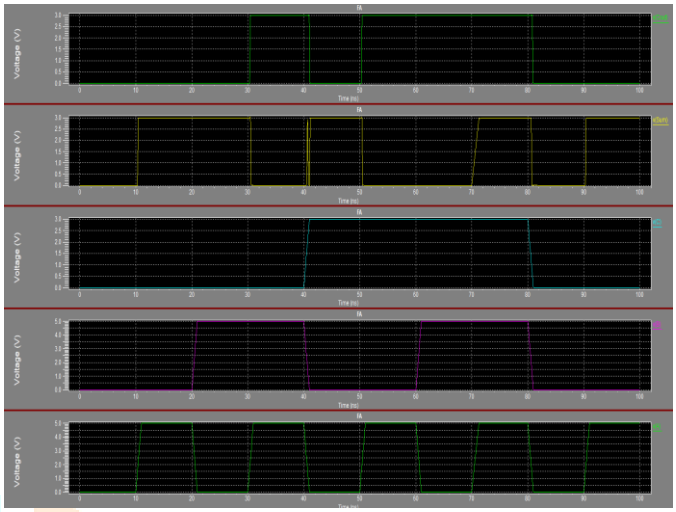

Fig 9: Simulated result of one- bit full adder based on CMOS logic.

We examined the construction of a one-bit full adder using Domino logic. Following that, we used the truth table of a full adder to check the output of this reasoning, as shown in Fig.10. When the clk signal is low, the p-MOS activates and charges the output node to Vdd, resulting in a high output. However, because we utilize an inverter to get the adder output, when the clk signal is low, it will show both sum and carry low. The clk signal provided during the simulation time will affect the timing of the pre-charge and evaluation phases.

Fig 10: Simulated result of one- bit full adder using Domino logic

Table 2: comparison of CMOS Full adder and Domino Full Adder in terms of Power

POWER(μW)		
Voltage (V)	**CMOS Logic**	**Domino Logic**
1	2.7	0.7
3	49.7	7.69
5	294.5	211.4
10	2352.4	1966.3
15	6932.2	4982.4

Table 3: comparison of CMOS Full adder and Domino Full Adder in terms of Power

DELAY(ps)		
Voltage (V)	**CMOS Logic**	**Domino Logic**
1	3.73	934.26
3	417.3	0.3
5	0.19	0.19
10	156.5	0.39
15	95.8	0.87

From the logic diagrams of CMOS full adder and Domino Logic full adder circuits it is clear that in the chip area, about 28.5 percent is saved. Because we have reduced the number of p-MOS transistors (produced in n-well), the chip space saved may be greater. Power was estimated for both logics and is shown in the above table2. According to the table, the Domino logic uses less power.

IV. CONCLUSION

A full adder circuit was constructed in this study using CMOS logic and Domino logic. To analyze the full adder circuit, Tanner EDA tools and 180nm technology were used. Domino logic was discovered to generate exceptionally accurate outcomes with less transistors and less power than CMOS design logic. It is also observed that the CMOS based full adder uses 28 transistors and Domino logic uses 20 transistors. There are almost no mistakes in Domino logic transient analysis. Domino logic is also smaller in size and has a lower latency than CMOS logic. Furthermore, because CMOS logic has higher instantaneous power than Domino logic, there is a higher danger of device failure with CMOS logic.

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