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## DESIGN OF LOW POWER LESS LEAKAGE QUARternary ADDER USING FINFET

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**ABSTRACT:** The Multi-valued logic (MVL) was more efficient logic than binary logic. A QTL Full Adder (QFA) is designed with support of Fin-Field Effect Transistor (FinFET) technology. FinFET provides low static leakage current, low switching voltage and power consumption. The Main aim is to design a Quaternary adder with minimum power and leakage with FinFET Technology.

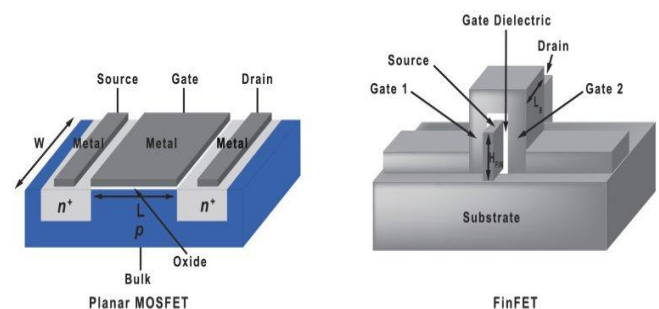
**Keywords:** Multi-valued logic (MVL), Quaternary Logic (QTL), FinFET.

### I. INTRODUCTION

The VLSI circuit has advanced Integrated Circuits (IC). The VLSI chips have external issues on chip. The MVL circuits are realized by 2 methods namely, 1) Current-mode and 2) Voltage mode. Current-mode circuits, power consumption is high because of poor current flow. The Reduction of noise is crucial task.

The Quaternary numeral system has base as 4. The Digits 0, 1, 2 and 3 was used for representing any real numbers. In Quaternary numeral system '4' is denoted as maximum number. The Quaternary logic

are denoted as {0, 1, 2, 3}. The Cost of input/output (I/O) pins should be taken into account. Every extra bus line has overall system was crucial. FinFET is known as Fin Field Effect Transistor. The FinFET word was derived from set of fins. A Multi-gate transistor has wide variety of gates. In FinFET, thin silicon film wrapped around the conducting channel. The Thickness of device depends upon channel length. FinFET device provides better performances than MOSFET technology.



**Figure 1:** Internal design of FinFET and MOSFET

## II. LITERATURE SURVEY

Hajare et al (2019) [1] designed FinFET based full adders. The MOSFET suffers with short channel effects. The FinFET based 28T and 16T 1-bit full adders was carried out in HSPICE software. The FinFET based full adder design was effective than MOSFET. A. Raghunandan and D. R. Shilpa (2019) [2] innovated High-Speed Hybrid Full Adders using FinFET 18nm Technology. The Hybrid full-adder circuits based on novel full-swing XOR-XNOR gates. This Experiment was carried out using Cadence virtuoso tool with 18nm FinFET technology. The HFA NB 26T achieved a smallest delay. V.M Senthilkumar and S. Sowmiya (2017) [3] used FinFET based 4-2 compressor with FinFET 32nm technology. The Two new approximate 4:2 compressors and full adder was designed using 10 transistors to evaluate 4 bit Dadda multiplier. This Experiment was carried out using HSPICE tool. M. Yang and E. Oruklu et al (2018) [4] applied full adder circuit design using Lateral Gate-All-Around (LGAA) FETs. Full-adder data path circuits using Lateral GAA FETs (LGAA FETs) based on BSIMCMG model are analyzed. W. -X. You et al (2019) [5] evaluated NC-FinFET based subsystem-level logic circuits. The NC-FinFET aspect on performance was discussed. H. Thapliyal et al (2018) [6] simulated MTJ/CMOS design. This Design are simulated with 45 nm CMOS technology. The MTJ/CMOS OR, AND, XOR, MUX and full adder designs had low power. H. Naseri and S. Timarchi et al (2018) [7] designed XOR/XNOR for low-power and fast full adder. The Experiment carried out using HSPICE and Cadence Virtuoso. The 65-nm CMOS process technology was utilized. Particle swarm optimization algorithm was utilized. A. Chauhan et al (2020) [8] analyzed low power quaternary adder using CNFET. Multi-valued logic (MVL) such as Quaternary Logic (QTL) was utilized. Carbon Nano-tube Field Effect Transistor (CNFET) was utilized to design QFA. The Experiment was carried out using Cadence Virtuoso. Roosta et al (2019) [9] designed multiplexer-based quaternary full adder. The Quaternary multiplexer 4:1 was designed with carbon nanotube field-effect transistors (CNFETs) 32-nm technology. The Experiment was carried out using HSPICE simulator. Takbiri et al (2020) [10] used multiple-valued logic (MVL) at Noise margin (NM) calculations. In MVL NM calculations are used to execute the equations with higher radices. A. K. Panda et al (2020) [11] used 3 operand binary adder. FPGA with 32nm CMOS technology. G. Dimitrakopoulos et al (2021) [12] discussed Sum Propagate Adders.

## III. EXISTING METHODOLOGY

### A. BINARY ADDERS

Binary Adders is used to add two binary digits. Combinational logic circuit was designed with logic gates. Binary adder is basic combinational logic circuits. It doesn't have any memory unit.

Binary	Quaternary
00	0
01	1
10	2
11	3

Table. 1(a) Represents binary to quaternary conversion

### B. CMOS TECHNOLOGY

CMOS (complementary metal-oxide semiconductor) is used in transistors. A complementary metal-oxide semiconductor (CMOS) consists of a pair of semiconductors. Hence, transistor is turned vice versa. The Main advantages of CMOS are lower power consumption, non saturating driver, and end to end complementary logic.

## IV. DISADVANTAGES OF EXISTING METHOD

The Main disadvantage of CMOS logic family is that runs slow speed. Propagation delay time for CMOS family was 50ns. The CMOS technology below 22nm suffers with short channel effects. Ripple Carry Adder (RCA), Carry Look Ahead (CLA) and Carry Save Adder (CSA) are analyzed in this paper. The Transition of output suffers with propagation delays. So that existing method suffers at computation process. Hence CMOS technology with binary or quaternary logic lags at latency, average power and area requirement (i.e. pin counts).

### V. PROPOSED METHODOLOGY

A Fin field-effect transistor (FinFET) is a multi-gate device, a MOSFET (metal-oxide-semiconductor field-effect transistor). The FinFET improves short-channel behavior, channel doping.

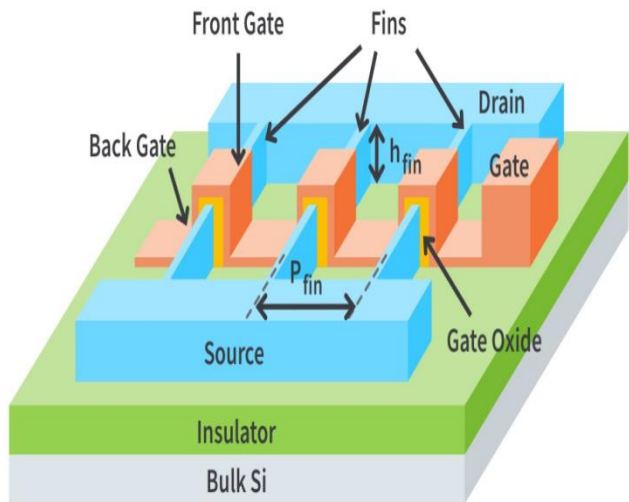


Figure 2: Internal design of FinFET

#### A. Quaternary logic

In quaternary logic 4 logic values are transmitted in the same wire. So same information is passed minimum wires. When wires count is minimized, critical path delay, area, total power and energy gets reduced. Quaternary logic has advantages over binary logic. It requires half the number of digits to store any information. The Quaternary storage mechanism is less than twice as complex as binary system.

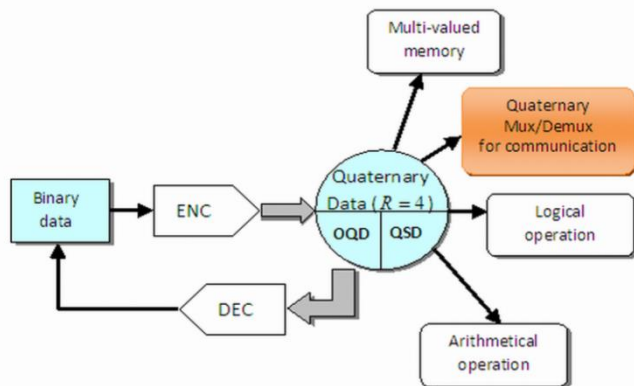


Figure 3: Quaternary logic computation

Quaternary logic is utilized to design Ripple Carry Adder (RCA), Carry Look ahead Adder CLA and Carry Save Adder (CSA) with 16nm FinFET Technology. The Average power is measured and compared with other adders.

### VI. RESULTS AND DISCUSSION

#### A. PROPOSED FINFET BASED HALF ADDER

Half adder implementation was designed with 16nm FinFET Technology.

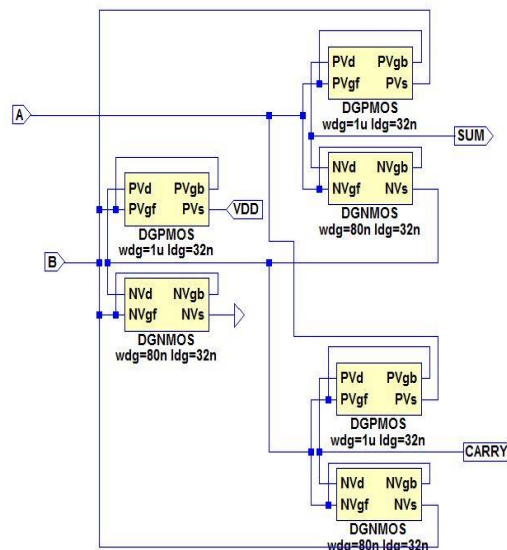


Figure 4: Half adder design with 16nm FinFET technology

The Figure 4 describes the half adder design with 16nm FinFET technology.

#### B. PROPOSED FINFET BASED FULL ADDER

The Proposed adder structure is designed using full adder with 16nm FinFET technology.

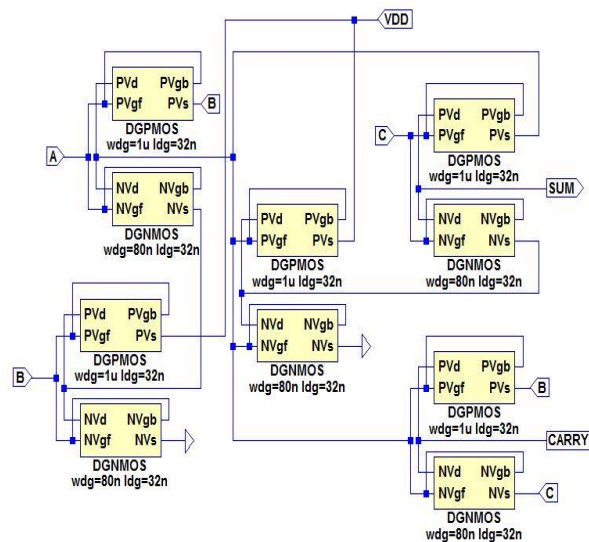


Figure 5: Full adder design with 16nm FinFET technology

The Figure 4 describes the full adder design with 16nm FinFET technology.

**C. QUATERNARY RIPPLE CARRY ADDER TRANSISTOR LEVEL IMPLEMENTATION WITH 16nm FinFET TECHNOGY IN LTSPICE**

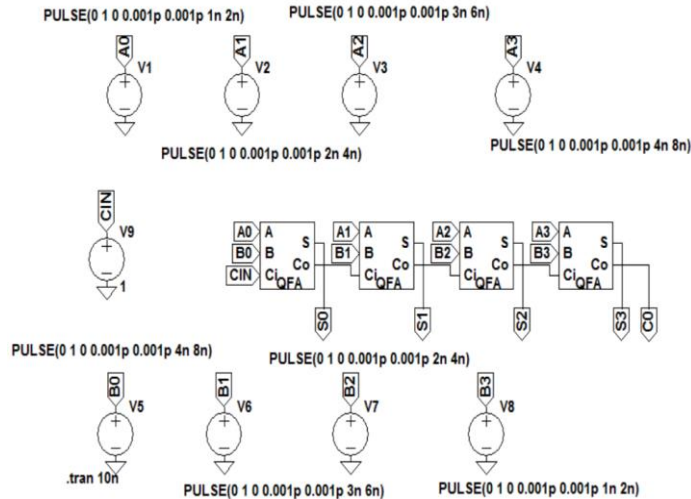


Figure 6 . Quaternary RCA Schematic

A Quaternary RIPPLE CARRY ADDER is designed using QHALF ADDER and QXOR with 16nm FinFET technology are given in figure 6

**D. QUATERNARY RIPPLE CARRY ADDER WITH 16nm FinFET TECHNOGY OUTPUT WAVEFORM**

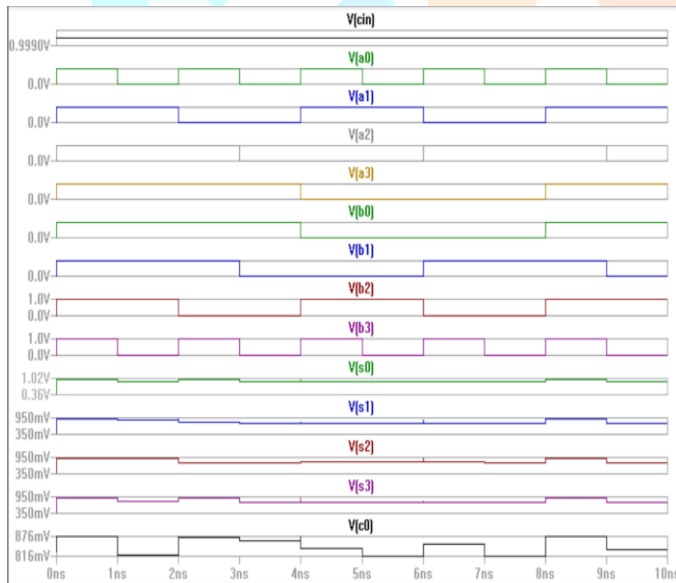


Figure 7. Quaternary RCA waveform Schematic  
Figure 7 represented a Quaternary RIPPLE CARRY ADDER WAVEFORM with 16nm FinFET technology is simulated at LT spice tool.

**E. QUATERNARY LOGIC 4 BIT CARRY LOOK AHEAD SCHEMATIC WITH 16nm FinFET TECHNOGY**

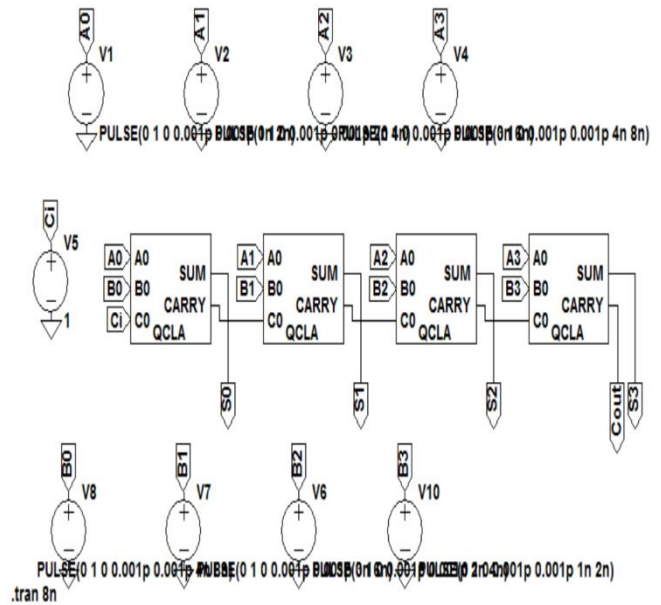


Figure 8. Quaternary RCA waveform Schematic  
A Quaternary 4 BIT CARRY LOOK AHEAD is designed using QFA with 16nm FinFET technology are given in figure 8.

**F. QUATERNARY LOGIC CARRY LOOK AHEAD ADDER WITH 16nm FinFET TECHNOGY OUTPUT WAVEFORM**

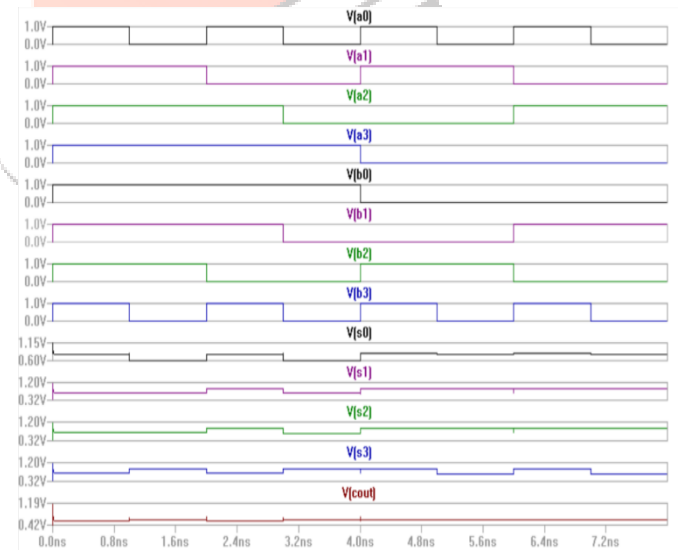


Figure 9. Quaternary CLA with 16nm FinFET technology waveform Schematic  
A Quaternary CARRY LOOK AHEAD ADDER is designed using QCLA with 16nm FinFET technology and its waveform is simulated at LT spice tool as represented in figure 9.



**G. QUATERNARY CARRY SAVE ADDER TRANSISTOR LEVEL IMPLEMENTATION WITH 16nm FinFET TECHNOGY IN LTSPICE**

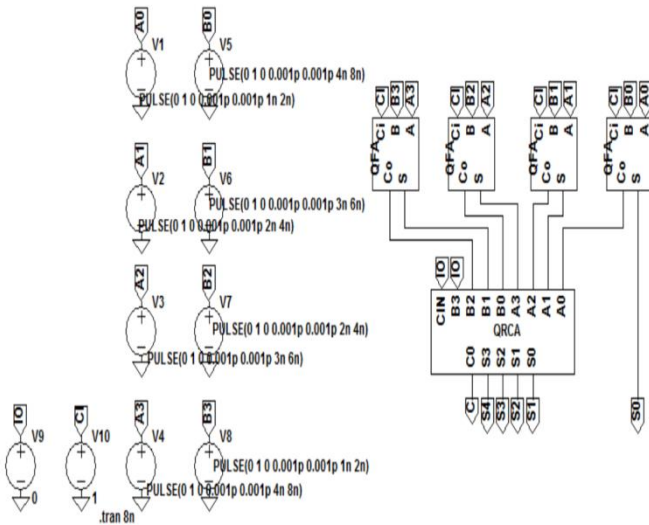
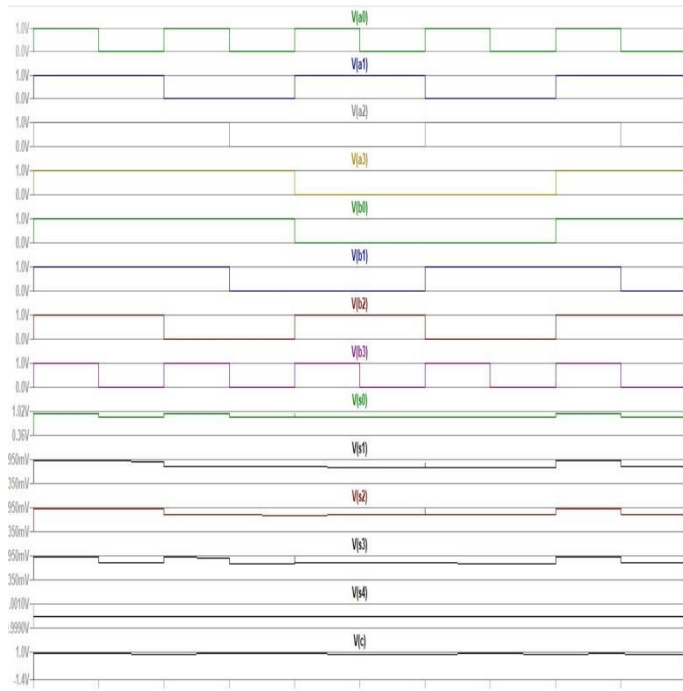


Figure 10. Quaternary CSA Schematic  
A Quaternary CARRY SAVE ADDER is designed using QFA and QRCA with CMOS technology are given in figure 10.

**H. QUATERNARY CARRY SAVE ADDER WITH 16nm FinFET TECHNOGY OUTPUT WAVEFORM**



**TABLE: 1 PERFORMANCE COMPARISION OF QUATERNARY CMOS AND FINFET**

SL.NO	PROPOSED QUATERNARY ADDER	AVG POWER CMOS	AVG POWER FINFET
1	Quaternary RCA	0.41817	0.21574
2	Quaternary CLA	0.67623	0.36018
3	Quaternary CSA	0.36547	0.17253

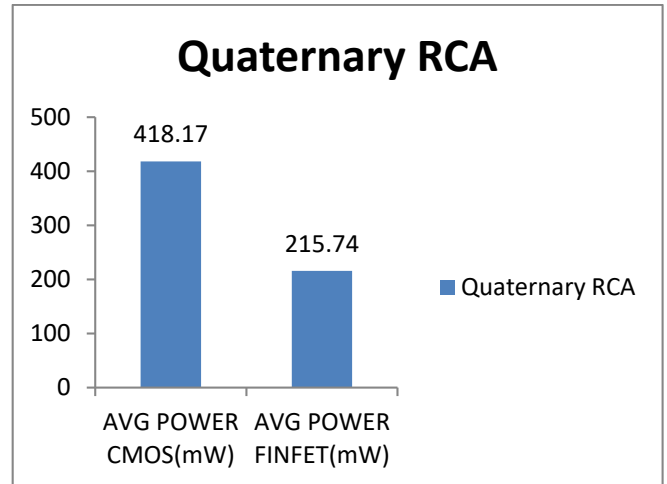


Figure.11 Quaternary RCA adder Average power on CMOS and FinFET

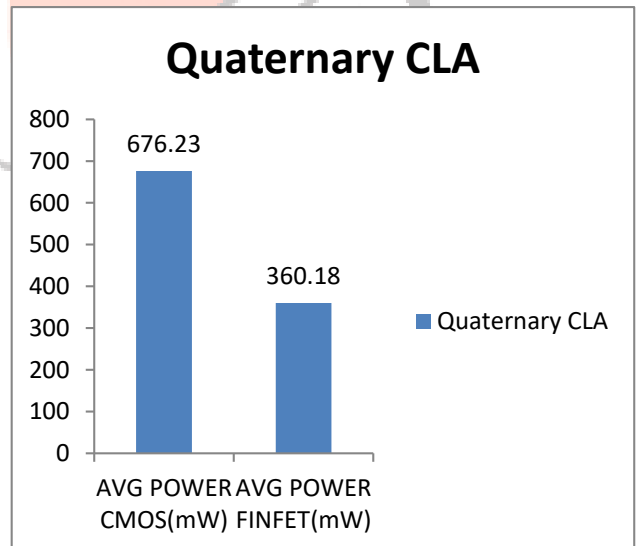


Figure.12 Quaternary CLA adder Average power on CMOS and FinFET

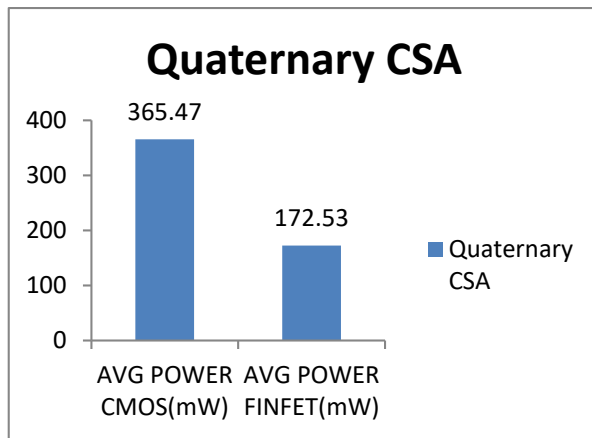


Figure.13 Quaternary CSA adder Average power on CMOS and FinFET

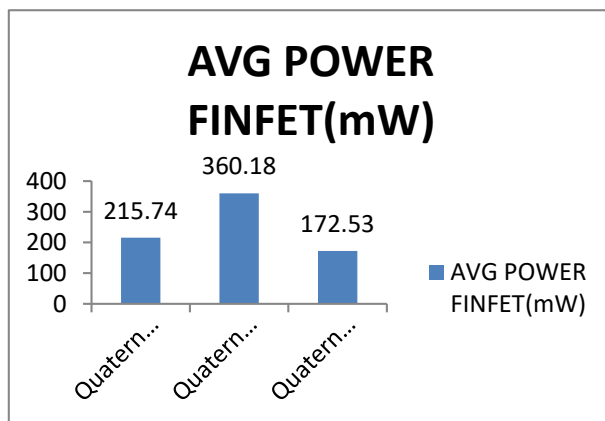


Figure.14 Quaternary CSA, Quaternary CLA, Quaternary RCA adders average power on CMOS and FinFET

## VII. CONCLUSION

This Paper proposes a quaternary adder with FinFET Technology. The Quaternary RCA, Quaternary CLA and Quaternary CSA performance were analyzed. The Average power is measured and compared with existing adders. The Proposed paper provides effective results power consumption. When a low power consumption and rapid computation reduces multiplication process. Using simulative comparisons, it has been shown that the proposed quaternary adder with FinFET technology is more efficiency than existing adders in terms of power, delay and area consumption.

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