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SIMULATION AND MITIGATION OF CUSTOMER VOLTAGE MAGNIFICATION DUE TO CAPACITOR SWITCHING

[1]Mr. Sunil T.Londhe,[2]Prof.A.V. Harkut,[3]Prof.P.R.Jawale

[1]P.G.Students at Department of Electrical (E&P) Engineering, PLITMS, Buldana,

[2]Assistant Professor at Department of Electronics & Telecommunication Engineering at PLITMS, Buldana,

[3]Associate Professor & HOD at Department of Electrical (E&P) Engineering at PLITMS, Buldana

Abstract: In the early days of development of the power system, electrical engineers were mainly concerned about 'keeping the lights on'. They designed the power system to withstand outages. The main concern was to prevent the frequency of power system from deviating from 50Hz after outages. With the development in technology, use of gadgets like computers, arc furnaces, xerox machine etc. increased. Due to the use of these devices the load on the power system increases especially during the day time because of which many a times voltage level decreases and is needed to be increased. This task of increasing the voltage profile is done by switching on of a capacitor bank in the power system. But this switching action gives rise to capacitor switching transients. These transients are very hazardous to the power system as they cause severe problem to it and components present in it. For instance, at any moment it can crash the computer or data loss and other such problems. So, it becomes necessary to know the cause of these transients so that they can be suppressed.

In this work a capacitor bank energization model is simulated in MATLAB Simulink environment. The voltage signals are captured at the source bus and load bus. The FFT analysis is carried out and mitigation of voltage magnification is done using pre-insertion resistor

I. INTRODUCTION

Nowadays a various industries are implementing an automatic power factor correction panel using capacitor banks for the improvement of power factor, but these capacitor banks are making an issue of switching transients during its energization. To improve the power factor capacitor banks may be switched several times during a day. An uncertain loads and fluctuations in voltage are responsible for the switching of capacitor banks. As a result, an unwanted voltage and current spikes having magnitude several times that of voltage and current in steady state will appears in the system, which tends to reduce the life of capacitor banks and electromagnetic switches. Therefore, to suppress this transient from the system certain techniques are implemented. One of the techniques is based on the zero-voltage closing control, this technique requires a lot of electronic equipment's, which tends to go for extra control system as a result cost and complexity of the system increases. Insertion of reactor is one of the methods for mitigation of surges but there is a problem of series resonance in the system. This research work presents a simple structure of resistive capacitor switching technique for mitigation of transients in the system. This technique contains a limiting resistor which works hand in hand to remove the switching transients occurred during the energization of capacitor bank. A limiting resistor is connected in such a way that when transient occurs in the system it should be suppressed by limiting resistor. Benefit of this system is that it has fast response.

II. Problem Statements:-

Voltage magnification occurring due to utility capacitor switching is now becomes a common phenomenon. This voltage magnification phenomenon leads to nuisance tripping of adjustable-speed drives (ASDs) and malfunctioning of other end user equipment's. As the utility and customers are now concern about power quality, there is a need to reduce or eliminate the effects of voltage magnification on customer electrical equipment. The devices that are commercially available to reduce or eliminate the effects of voltage magnification include high-resistance or low-resistance pre-insertion inductors used with circuit switchers, controlled closing circuit breakers or vacuum interrupters, and circuit breakers with pre-insertion resistors. This research work mainly focuses the problem of occurrence of voltage magnification issue due to capacitor switching and its mitigation using the pre-insertion resistors.

III. Aim and Objectives of work

The aim of this dissertation work is to simulate and mitigate the customer voltage magnification due to capacitor switching.

Objectives:

- Simulate the capacitor bank energizing model for simulating voltage magnification due to capacitor switching.
- Study the effect of Isolated capacitor switching.
- Study the effect of Back-to-Back capacitor switching.
- Mitigate the voltage magnification phenomenon by using different capacitor switching transients reducing techniques.

➢ Transient:

The term transient has long been used in the analysis of power system variations to denote an event that is undesirable but momentary in nature. The notion of a damped oscillatory transient due to a RLC network is probably what most power engineers think of when they hear the word transient. Other definitions in common use are broad in scope and simply state that a transient is "that part of the change in a variable that disappears during transition from one steady state operating condition to another." Unfortunately, this definition could be used to describe just about anything unusual that happens on the power system. Broadly speaking, transients can be classified into two categories:

- Impulsive Transient
- Oscillatory Transient

➢ Capacitor switching:

Capacitors energizing transient events are one of the most common transient events present in power systems. The transient events occur when a capacitor is switched on. At the switching instant, a fast change in the bus voltage occurs because the voltage in the Capacitor cannot change instantaneously. The transient frequency is determined by the combination of the capacitance of the capacitor bank and the system inductance. The oscillation frequency in the voltage waveform is typically between 300–1000 Hz and lasts for less than half a cycle of the power frequency. There are mainly two kinds of capacitor energizing events, namely the isolated energizing and back-to-back energizing.

➢ Effects of capacitor switching

A transient from its point of origin will be propagated in either direction in the distribution system and will be transferred through the transformer inductive/capacitive couplings to other voltage levels.

The application of shunt capacitors can lead to the following effects:

- Severe harmonic distortion and resonance with load generated harmonics
- Increase the transient inrush current of power transformers in the system, create over voltages, and prolong its decay rate.
- Capacitors themselves can be stressed due to the switching transients.
- They may discharge into an external fault, and produce damaging over voltages across Current Transformers secondary terminals.
- Impact sensitive loads, i.e., drive system and bring about a shutdown.

Thus, we see that the capacitor switching results in Voltage Magnification, undesired tripping of Adjustable Speed Drives and production of Harmonics in the system.

IV. Voltage Magnification

Voltage magnification occurs when the transient oscillation, initiated by the energization of the distribution capacitor bank, excites a series resonance formed by the low voltage system. The result is a higher overvoltage at the low voltage bus.At many facilities, fixed capacitors are used to reduce cost. Fixed capacitors are those that are permanently connected to the load bus and are not switched on and off as the load changes. When the load on the facility is low, the voltage may increase due to the capacitor being sized for the higher load. The limit on steady state voltage is generally taken to be 110% of the rated voltage. If the voltage is allowed to rise above this point, transformers will saturate and overheat, mal operation of equipment may occur and equipment life will be reduced. If the prevailing bus voltage happens to be high, due to conditions on the distribution system feeding the facility, the voltage rise would be added to this already higher voltage. Therefore, system voltage should be checked when considering voltage rise.

➢ The magnified transients are worst when:

- The size of switched capacitor bank is significantly larger (almost 10 times) than the low voltage power factor correction bank.
- The energizing frequency is close to the series resonant frequency formed by the step-down transformer and the power factor correction capacitor bank.
- There is relatively little damping (resistive) provided by the low voltage load.

Typically, the transient over voltages will simply damage low-energy protective devices (MOV's) or cause an undesirable trip of a power electronic device. However, there have been several cases of complete failure of customer equipment (single device).

➢ Tripping of Adjustable Speed Drives

Most of the appliances utilities consuming power comprise of Adjustable Speed Drive or other power electronic process device. Undesired tripping refers to the undesired shutdown of an adjustable-speed drive due to the transient overvoltage on the device's dc bus. Very often, this overvoltage is caused by transmission and/or distribution capacitor bank energization. Considering the fact that many distribution banks are time clock controlled, it is easy to see how this event can occur on a regular basis, thereby causing numerous process interruptions for the plant.

The nuisance tripping event consists of an overvoltage trip due to a dc bus overvoltage on voltage-source inverter drives (pulse-width modulated - PWM). Typically, for the protection of the dc capacitor and inverter components, the dc bus voltage is monitored and the drive trips when it exceeds a preset level. This level is around 120% of the operational DC voltage. The potential for nuisance tripping is primarily dependent on the switched capacitor bank size, overvoltage controls for the switched bank, the dc bus capacitor size, and the inductance between the two capacitors. It is important to note that nuisance tripping can occur even if the customer does not have power factor correction capacitors.

➢ Condition of Voltage Magnification

Voltage magnification occurs when the transient oscillation initiated by the energization of the distribution capacitor bank excites a series resonance formed by the low voltage system. The result is a higher overvoltage at the low voltage bus.

The highest transient voltages occur at the lower voltage capacitors when the following conditions are met:

- The natural frequencies f1 and f2 are nearly equal.

- The capacitive MVAr of the switched capacitor bank is significantly greater (>10) than the lower voltage capacitor.
- There is little damping on the low voltage system (mostly motor load).

The magnified transient at the lower voltage bus can reach 4 per-unit.

➢ Mitigation of Voltage Magnification

- **Synchronous closing control**

  Method for controlling overvoltage by switching when the voltage across the switch at the closing instant is equal to zero (zero voltage on capacitor - zero voltage on bus).

- **Pre-insertion device:**

  Method for controlling overvoltage by inserting an impedance (usually inductance or resistance) in series with the component to be energized voltage.

- **Arresters:**

  Method for controlling overvoltage by "clipping" at a specified protective level.

- **Capacitor Bank Calculations**

The current flowing through the capacitor at normal power frequency is

$$I = \frac{Q}{\sqrt{3}V} = \frac{40 * 10^3}{\sqrt{3} * 400} = 57.7350A$$

The capacitance for each leg can be determined via the following method:

$$X_c = \frac{V^2}{Q}$$

$$C = \frac{Q}{V^2\omega} = \frac{40 * 10^3}{400^2 * 2\pi * 50} = 795.7747\mu F$$

The minimum source inductance required to limit the transient to an acceptable level is determined as follows. Assume that the rated (short-circuit) breaker current is 10 kA. Use a tolerance factor of 5 % for the voltage (V = 400V x 1.05=420V)

$$X_L = \frac{V}{\sqrt{3} * 10 * 10^3} = \frac{420}{\sqrt{3} * 10 * 10^3} = 0.0242487\Omega$$

$$L = \frac{X_L}{\omega} = 77.18604\mu H$$

The instantaneous voltage V_0 is the peak phase voltage across the capacitor when breaker B1 is closed. If the capacitor is initially charged, then this value must be added or subtracted from V_0:

$$V_0 = \frac{\sqrt{2}}{\sqrt{3}}(V_{rated}) = \frac{\sqrt{2}}{\sqrt{3}}(400) = 326.5986V$$

The switching surge impedance is determined by the combination of source inductance and the capacitance in a single leg of a bank:

$$Z_{surge} = \sqrt{\frac{L}{C}} = 0.3114399\Omega$$

The following equations can be used to determine the magnitude and frequency of the inrush currents when breaker is closed at a voltage peak. Since the transient frequency of the inrush current is much higher than the 50 Hz power frequency, we can assume the instantaneous voltage (V_0) will remain constant over the transient period.

$$I_{peak} = \frac{V_0}{Z_{surge}} = 1048.7062A$$

$$f = \frac{1}{2\pi\sqrt{L} * C} = 642.1785Hz$$

The inrush current magnitude is approximately 20 times higher than the peak current at the power frequency.

The pre-insertion resistance will damp out the transients. Its value can be determined using the following equation:

$$R_{optimum} = \sqrt{\frac{L}{C}} = 0.3114\Omega$$

V. System Studied

The capacitor bank energizing model developed in Simulink is shown in figure 1. It is used to simulate customer voltage magnification caused by capacitor bank energization for power factor correction in the power system. The model consists of 11 kV, 30 MVA, 50 Hz three-phase source feeding through 11 kV/0.4 kV, 1 MAV delta/wye transformers to 100 kW resistive and 100 kvar inductive load. The voltage measurement is carried at 11 kV and 0.4 kV buses. Each feeder bus consists of a capacitor bank connecting through a three-phase circuit breaker. The capacitor bank at 0.4 kV bus has a capacity of 40 kvar, which can compensate power factor up to 0.857 for a 100 kvar inductive load. The capacitor bank at 11 kV bus usually has a higher capacity, in this model 100 kvar is used. The capacitor bank energizing model is capable of simulating customer voltage magnification caused by energization of capacitor bank at 11 kV bus or at 0.4 kV bus. A 0.2 second simulation time is set to run the simulation.

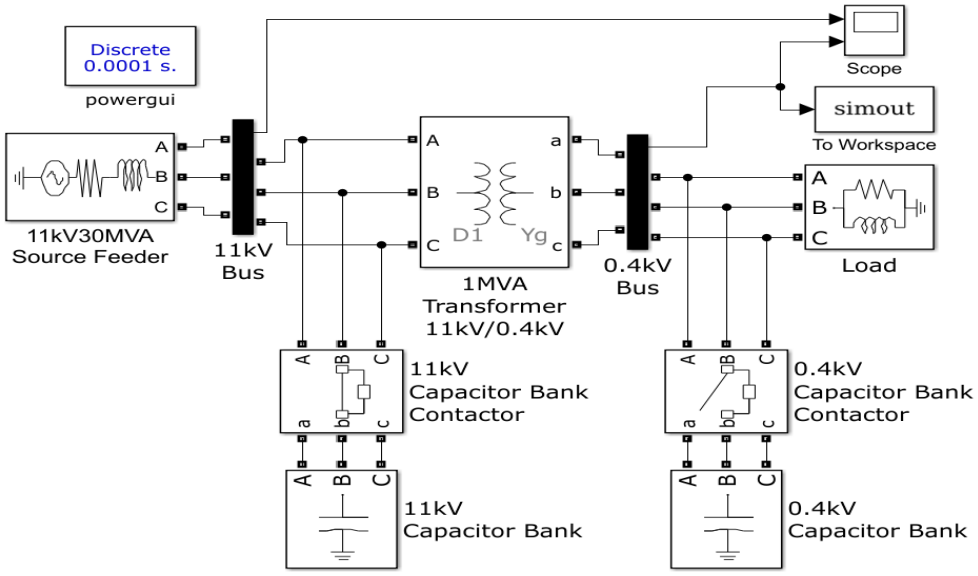

Figure 1:- Capacitor Bank Energizing Model Developed in Simulink

➢ Simulation Cases

The capacitor bank energization model is simulated using MATLAB Simulink Environment. Here star connected capacitor banks configuration are used. In general, there are two capacitor switching configurations. Configuration1 is when a signal capacitor bank is connected to the A.C bus. This is typically referred to as isolated capacitor switching. Another configuration is when there are multiple capacitor banks A.C bus. When a bank is switched on to the bus with other banks all ready connected, this is referred to as back-to-back capacitor.

In this dissertation both isolated and back-to-back capacitor switching configurations with star connected capacitor banks are considered.

In Simulink circuit there are total 2 capacitor banks. They are connected to the A.C bus with the help of circuit breakers. In this dissertation work 3 cases are considered.

Case 1: Without Pre-insertion resistor

1) Back-to-Back switching of 0.4kV capacitor bank
2) Isolated switching of 0.4kV and 11kV capacitor bank

Case 2: With Pre-insertion resistor of 0.3Ω

1) Back-to-Back switching of 0.4kV capacitor bank
2) Isolated switching of 0.4kV and 11kV capacitor bank

Case 3: With Pre-insertion resistor of 3Ω

1) Back-to-Back switching of 0.4kV capacitor bank
2) Isolated switching of 0.4kV and 11kV capacitor bank

In each case the capacitors are switched at instants 0^o,45^0 and 90^0 of R phase(which is a reference phase). Here in this report we have just present the result of capacitor switching at 0^o only. But in actual practice we have take the result at 0^o,45^0 and 90^0 of R phase(which is a reference phase).

VI. Methodology

The capacitor bank energization model shown in figure 1 is simulated using MATLAB Simulink environment. Total 3 cases of capacitor switching are simulated at 00, 450 and 900 switching instants. The voltage waveform is captured at the source and load. The duration of simulation run is kept 0.2 seconds. The waveform is sampled at 10 KHz sampling frequency.

The voltage magnification phenomenon occurs due to the switching of capacitor bank at the source and load buses. The evaluation of this phenomenon is done by measuring the voltage peak during the transient period in the captured voltage waveform. Further the FFT analysis of the captured voltage waveform is done with the help of MATLAB toolbox. The percentage of THD is estimated in each case corresponding to 11kV and 0.4kV voltage waveforms.

In case 1 both isolated and back-to-back switching of capacitor bank is done to simulate voltage magnification phenomenon. In case 2 the mitigation of voltage magnification is done by using the pre-insertion resistor (0.3Ω) technique of mitigation. In case 3 the mitigation of voltage magnification is done by using the pre-insertion resistor (3Ω) technique of mitigation. In each case FFT analysis is done and the THD percentage are calculated. Finally, the comparison of the THD percentage in each case is done to evaluate the performance of mitigation technique.

VII. Simulation Waveforms and FFT Analysis

The simulation waveforms of voltages for each case at 0^0, 45^0 and 90^0 instants are represented along with its FFT analysis.

1) Back-to-back capacitor switching of 0.4kV capacitor at 0^0 instant of R-phase:

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. Figure 2 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 0^0 instant of R-phase.

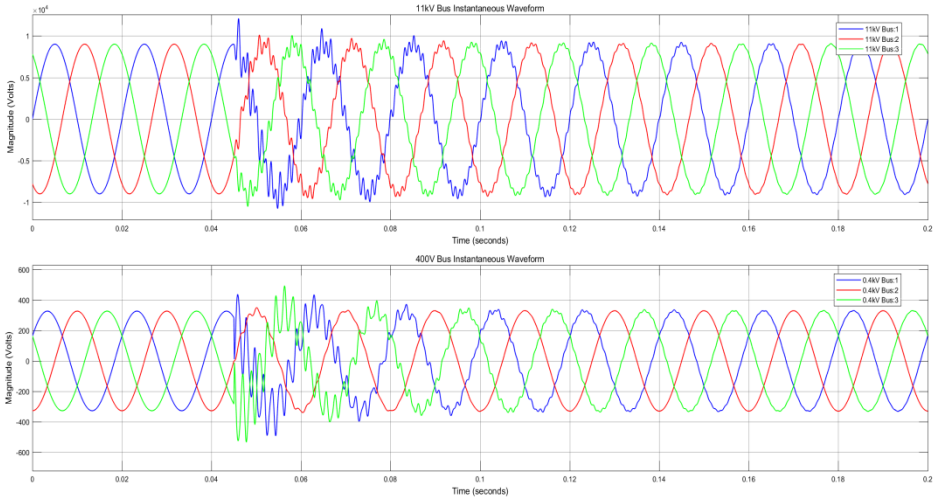

Figure 2:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 3 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 2.85%.

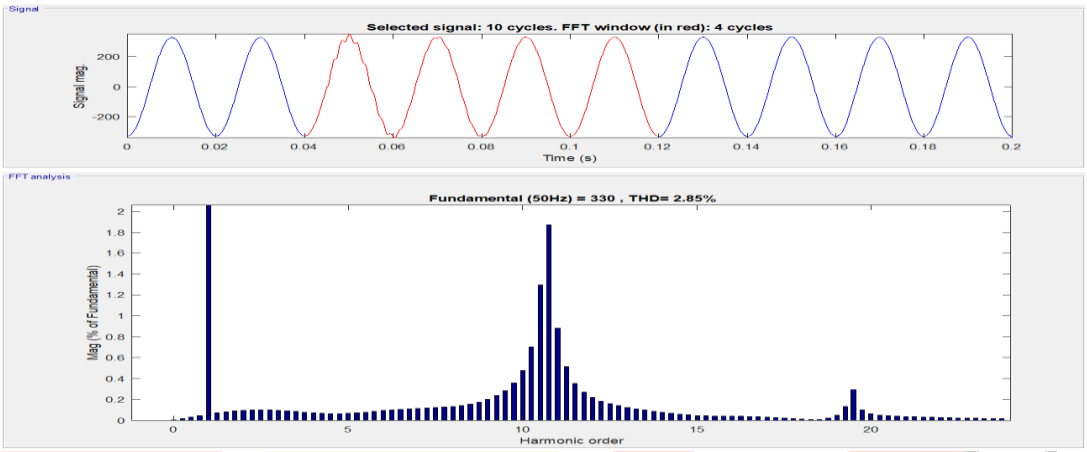

Figure 3:- FFT analysis of voltage waveform at 0.4kV bus

Figure 4 shows the FFT analysis of voltage waveform at 11kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 6.63%.

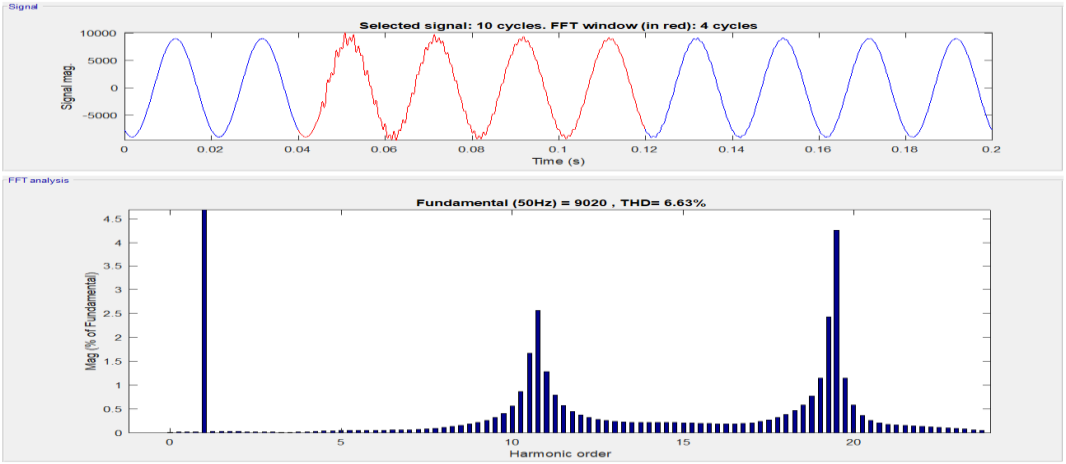

Figure 4:- FFT analysis of voltage waveform at11kV bus

2) Isolated capacitor switching of 0.4kV capacitor at 0^0 instant of R-phase:

The capacitor bank is energized from a bus that does not have other capacitor banks energized called as isolated capacitor switching. In this case the capacitor banks connected at 0.4kV bus is switched in an isolated mode. A capacitor bank at 11kV is off and the capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. Figure 5 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the isolated switching of 0.4kV capacitor at 0^0 instant of R-phase.

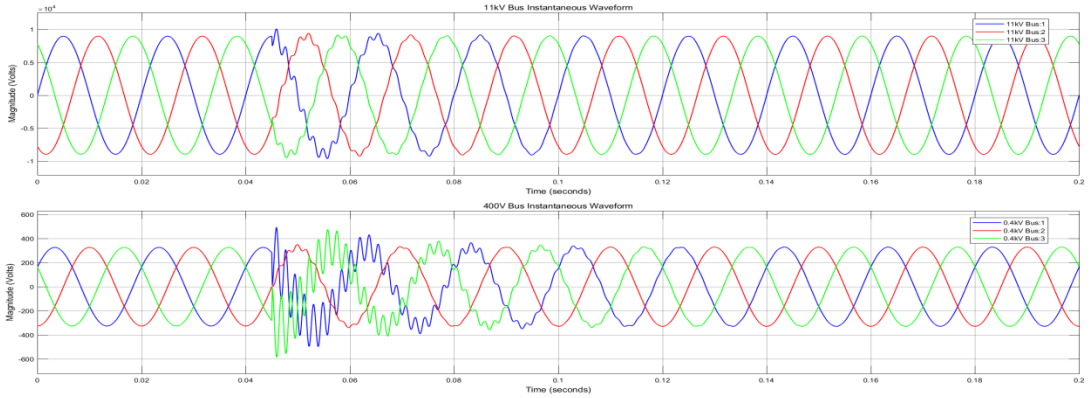

Figure 5:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 6 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 3.03%.

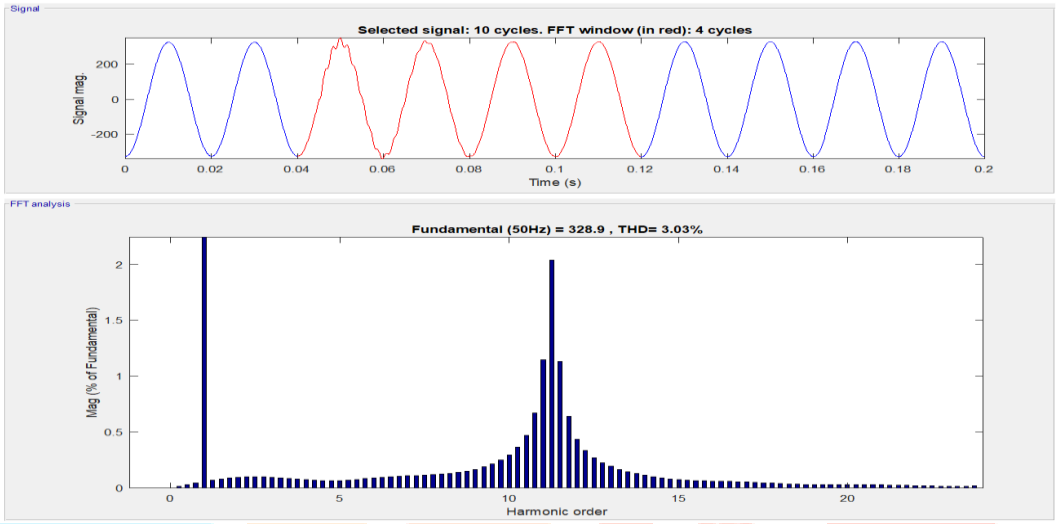

Figure 6 :- FFT analysis of voltage waveform at 0.4kV bus

Figure 7 shows the FFT analysis of voltage waveform at 11kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 2.91%.

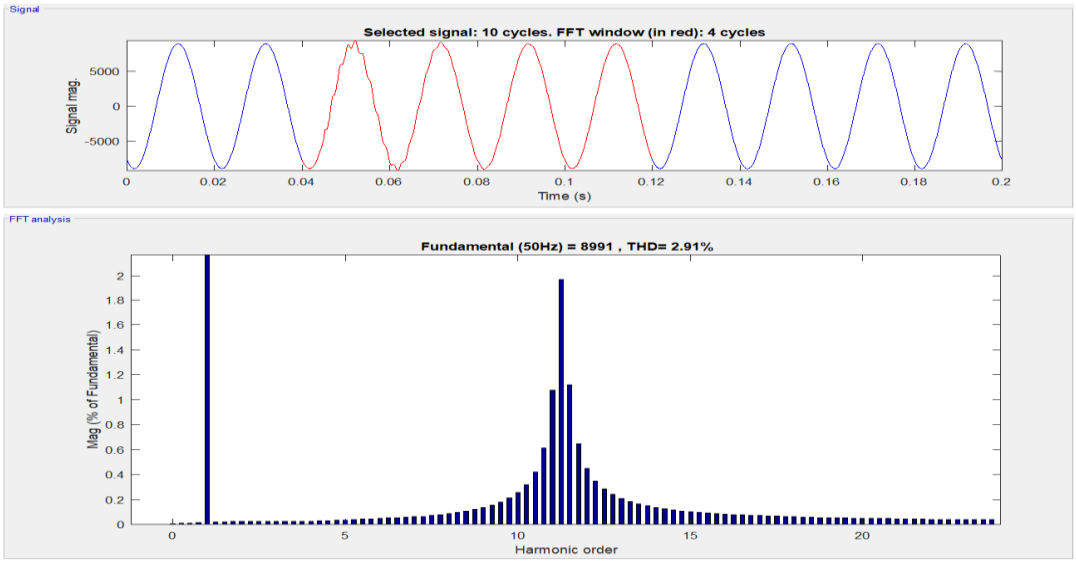

Figure 7:- FFT analysis of voltage waveform at11kV bus

VIII. Mitigation of Voltage Magnification

At the switching instant, the voltage in the capacitor cannot change instantaneously. The bus voltage is pulled down, and then rises as the capacitor begins to charge. During the process, the capacitor voltage may overshoot. This phenomenon of voltage magnification is mitigated by various techniques. In this dissertation pre-insertion resistors are used to mitigate the voltage magnification effect. As per the calculation the pre-insertion resistor of 0.3 Ω is required to mitigate the voltage mitigation. Here we have considered 0.3 ohm and 3 Ω pre-insertion resistors for mitigation of voltage magnification caused by capacitor switching. Figure below shows the results of pre-insertion resistor method of mitigation of voltage magnification.

With Pre-insertion Resistor of 0.3 Ω

1) Back-to-back capacitor switching of 0.4kV capacitor at 0^0 instant of R-phase:

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already energized and capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 0.3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification

caused by capacitor switching. Figure 8 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 0^0 instant of R-phase with the pre-insertion resistor of 0.3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.

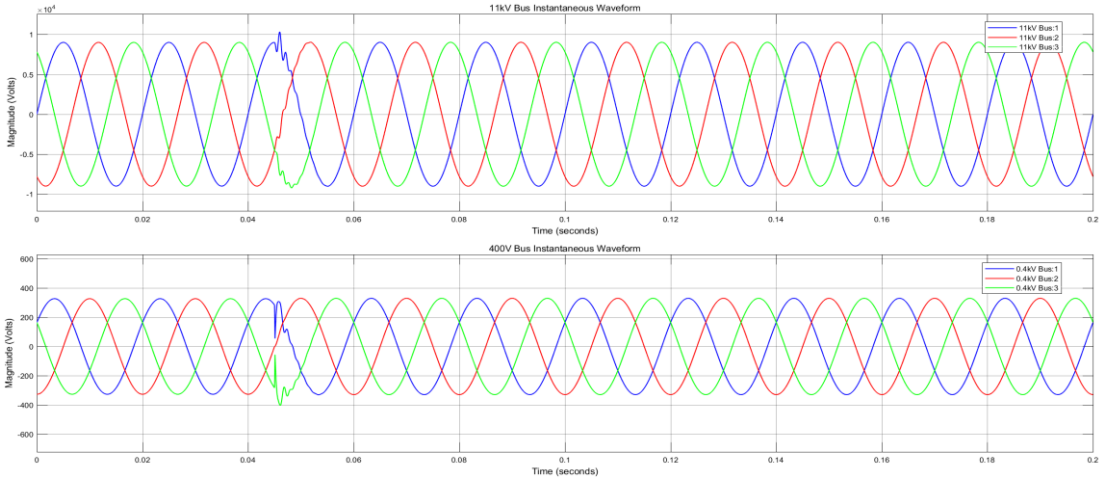

Figure 8:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 9 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.60%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching

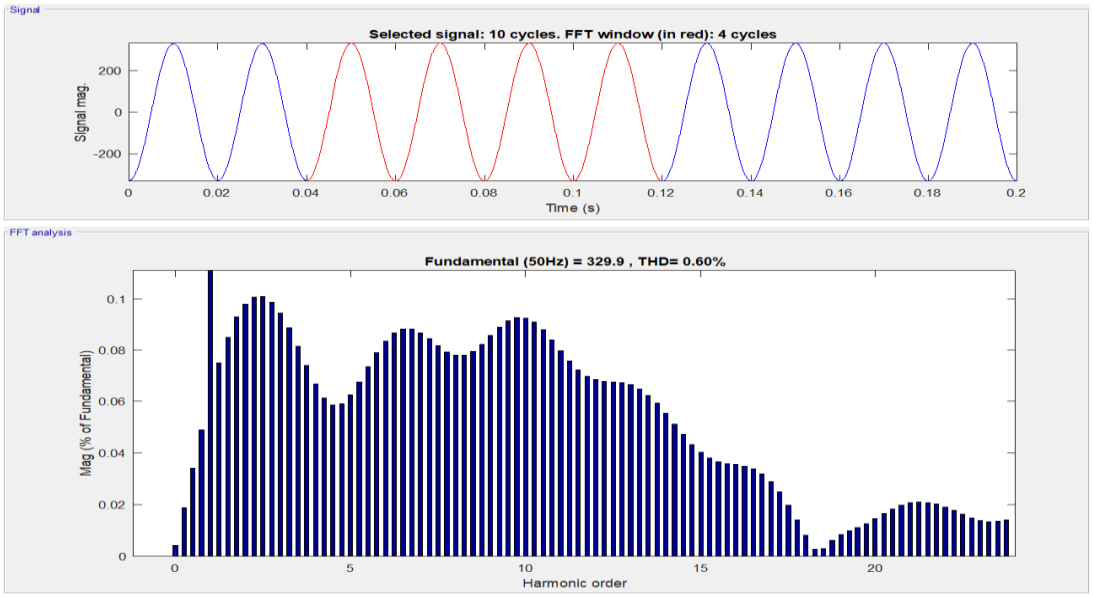

Figure 9:- FFT analysis of voltage waveform at 0.4kV bus

Figure 10 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 1.24%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

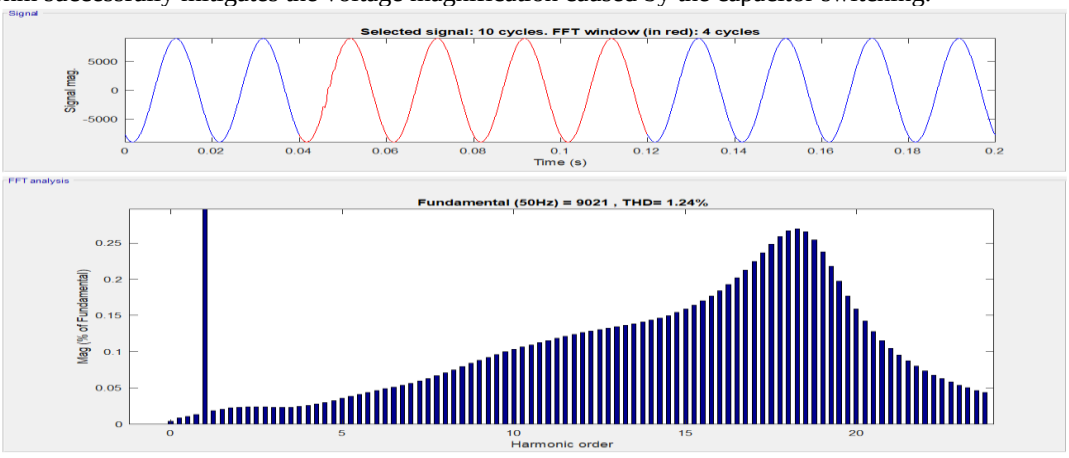

Figure 10:- FFT analysis of voltage waveform at11kV bus

2) Isolated capacitor switching of 0.4kV capacitor at 0^0 instant of R-phase:

The capacitor bank is energized from a bus that does not have other capacitor banks energized called as isolated capacitor switching. In this case the capacitor banks connected at 0.4kV bus is switched in an isolated mode. A capacitor bank at 11kV is off and the capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. During the energization of capacitor bank using

the circuit breaker a pre-insertion resistor of 0.3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 11 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the isolated switching of 0.4kV capacitor at 0^0 instant of R-phasewith the pre-insertion resistor of 0.3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.

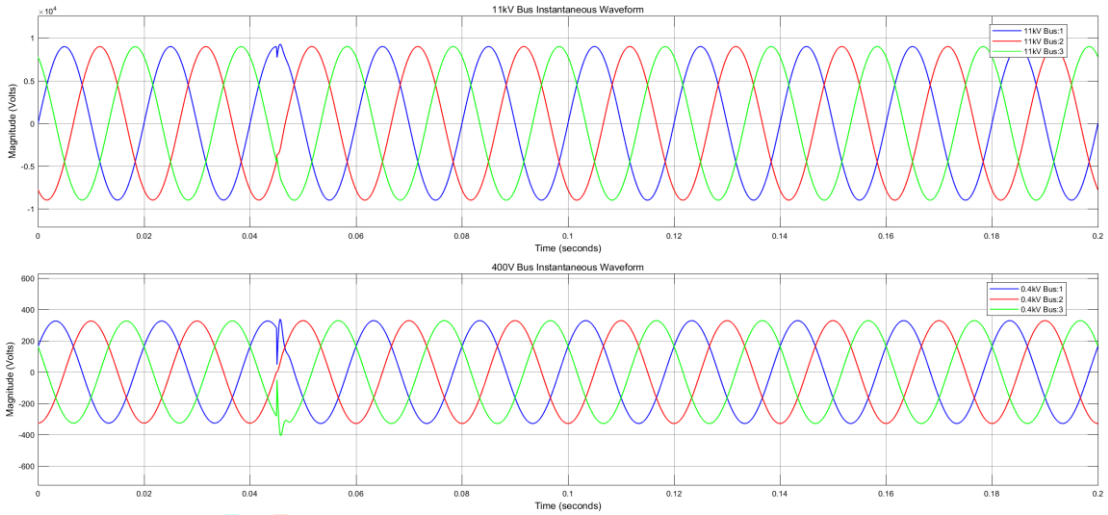

Figure 11:-Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 12 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.59%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

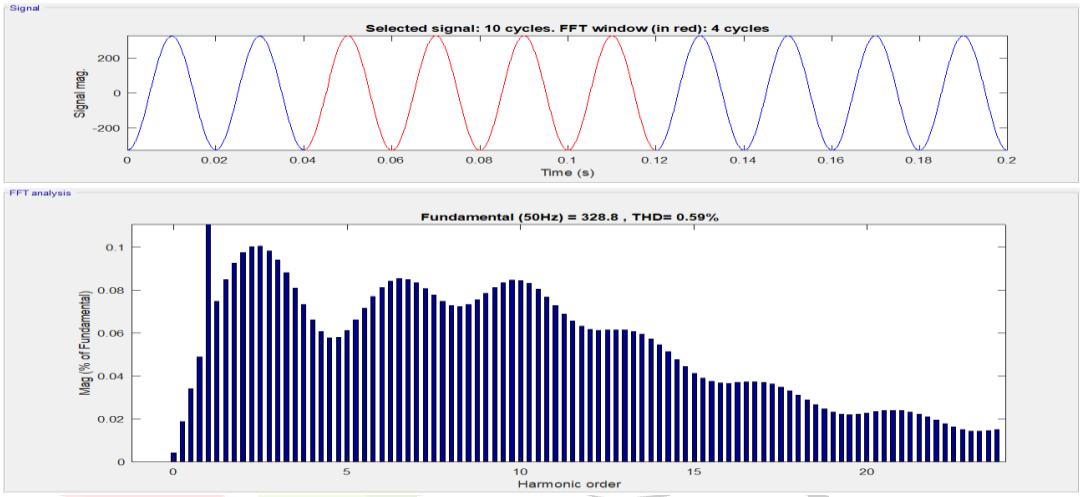

Figure 12:- FFT analysis of voltage waveform at 0.4kV bus

Figure 13 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.54%. From the THD percentage it is cleared that the pre-insertion resistor of 0.3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

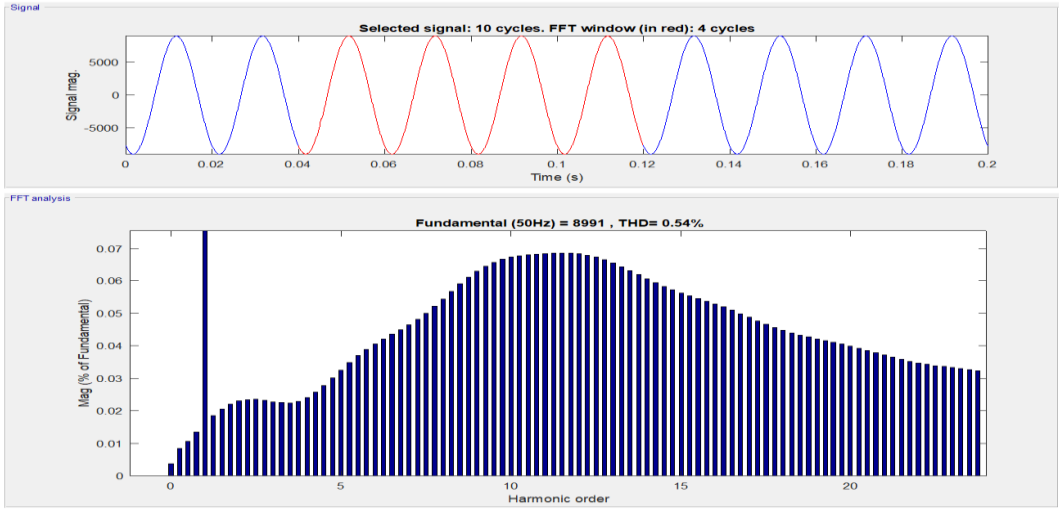

Figure 13:- FFT analysis of voltage waveform at11kV bus

With Pre-insertion Resistor of 3 Ω

1) **Back-to-back capacitor switching of 0.4kV capacitor at 0^0 instant of R-phase**:

A back-to-back capacitor switching is the energization of a capacitor bank near a capacitor bank already energized. In this case the capacitor banks connected at 11kV and 0.4kV buses are switched back-to-back. A capacitor bank at 11kV is already

energized and capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 14 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the back-to-back switching of 0.4kV capacitor at 0^0 instant of R-phase with the pre-insertion resistor of 3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.

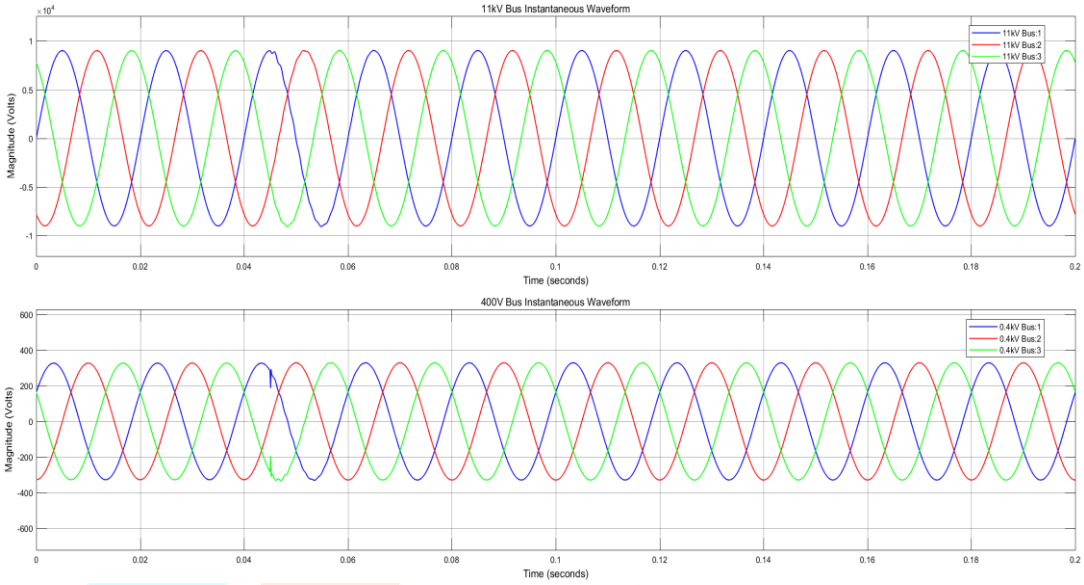

Figure 14:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 15 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.20%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

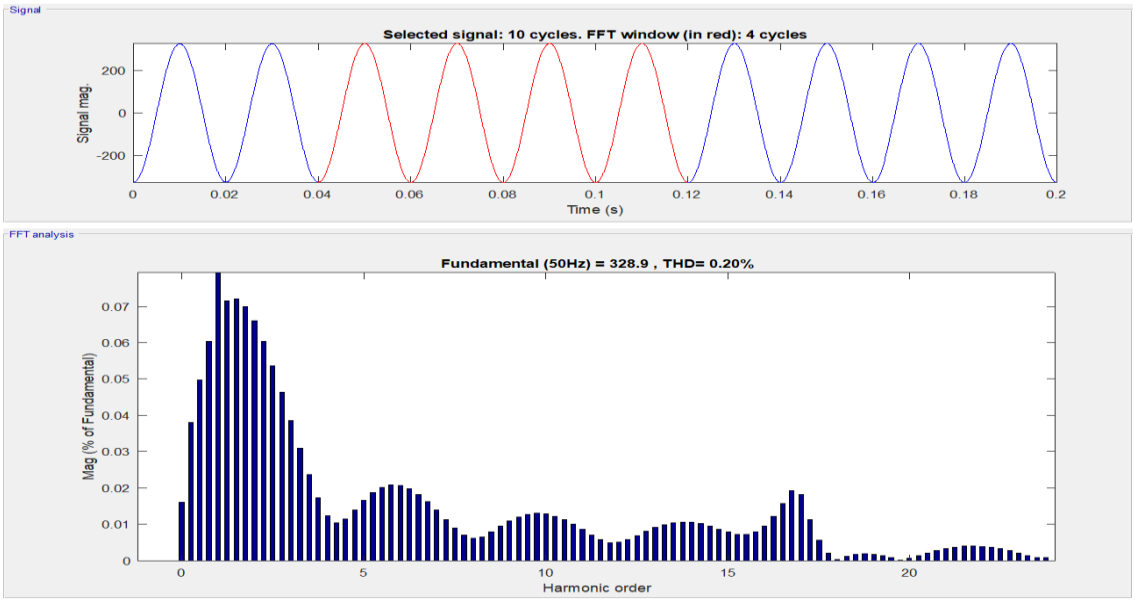

Figure 15:- FFT analysis of voltage waveform at 0.4kV bus

Figure 16 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.33%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

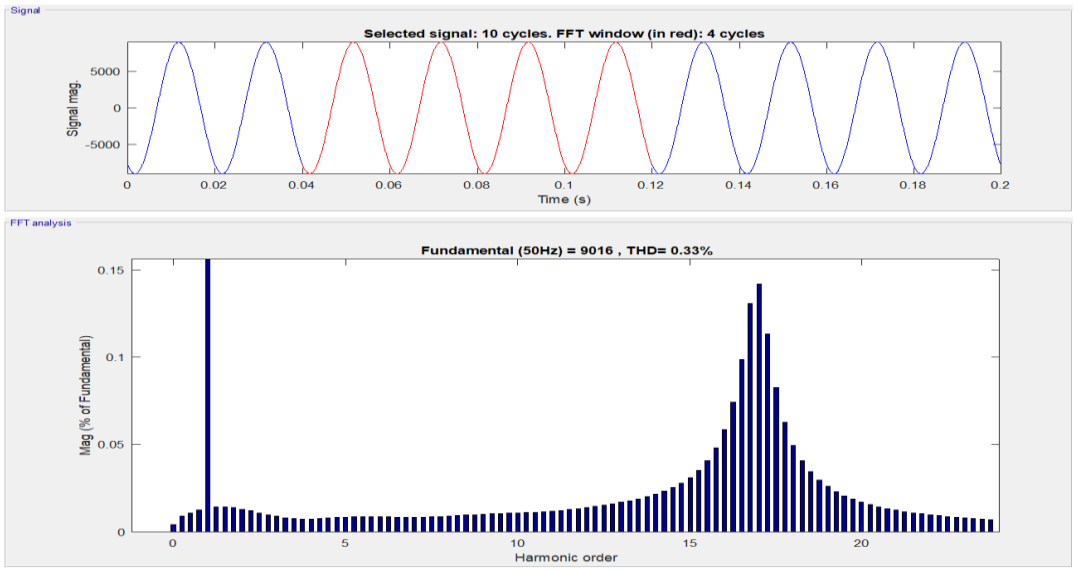

Figure 16:- FFT analysis of voltage waveform at11kV bus

2) Isolated capacitor switching of 0.4kV capacitor at 0^0 instant of R-phase:

The capacitor bank is energized from a bus that does not have other capacitor banks energized called as isolated capacitor switching. In this case the capacitor banks connected at 0.4kV bus is switched in an isolated mode. A capacitor bank at 11kV is off and the capacitor bank at 0.4kV is energized at 0^0 instant of R-phase. During the energization of capacitor bank using the circuit breaker a pre-insertion resistor of 3 ohm is inserted in the switching circuit in order to mitigate the voltage magnification caused by capacitor switching. Figure 17 shows the instantaneous voltage waveforms of 11kV and 0.4kV buses under the isolated switching of 0.4kV capacitor at 0^0 instant of R-phase with the pre-insertion resistor of 3 ohm inserted in the circuit breaker used to energize the capacitor bank. From the figure it is clearly seen that the voltage magnification effect is mitigated by the pre-insertion resistor.

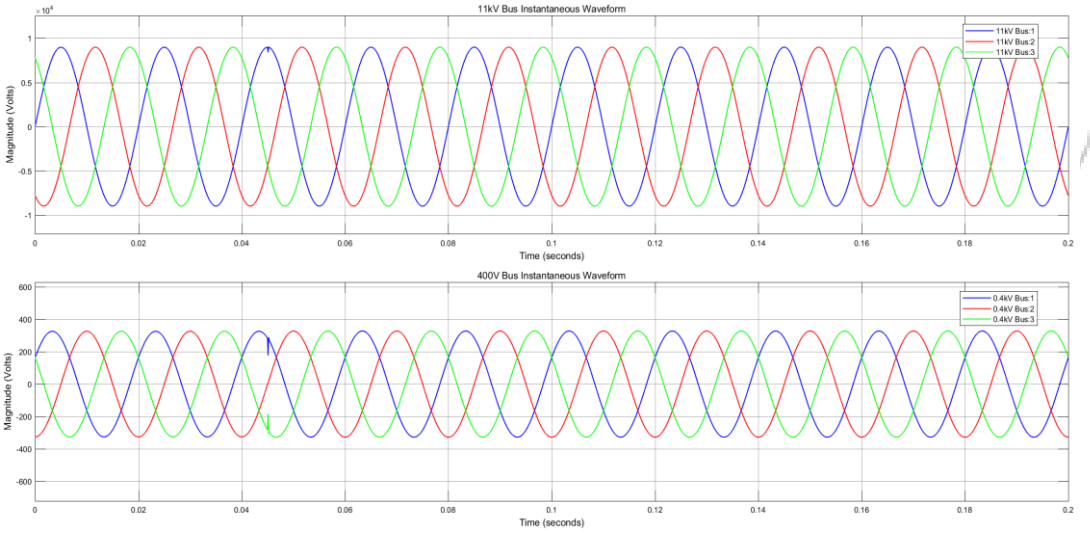

Figure 17:- Voltage waveform of 11kV and 0.4kV bus due to back-to-back capacitor switching

Figure 18 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.20%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

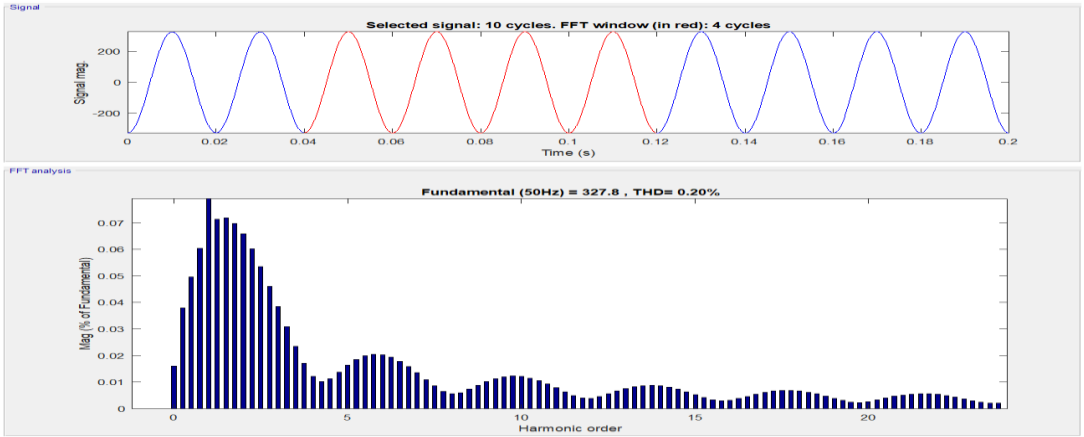

Figure 18:- FFT analysis of voltage waveform at 0.4kV bus

Figure 19 shows the FFT analysis of voltage waveform at 0.4kV bus. The analysis is carried over the complete 10 cycles of the voltage signal and the THD percentages are found to 0.16%. From the THD percentage it is cleared that the pre-insertion resistor of 3 ohm successfully mitigates the voltage magnification caused by the capacitor switching.

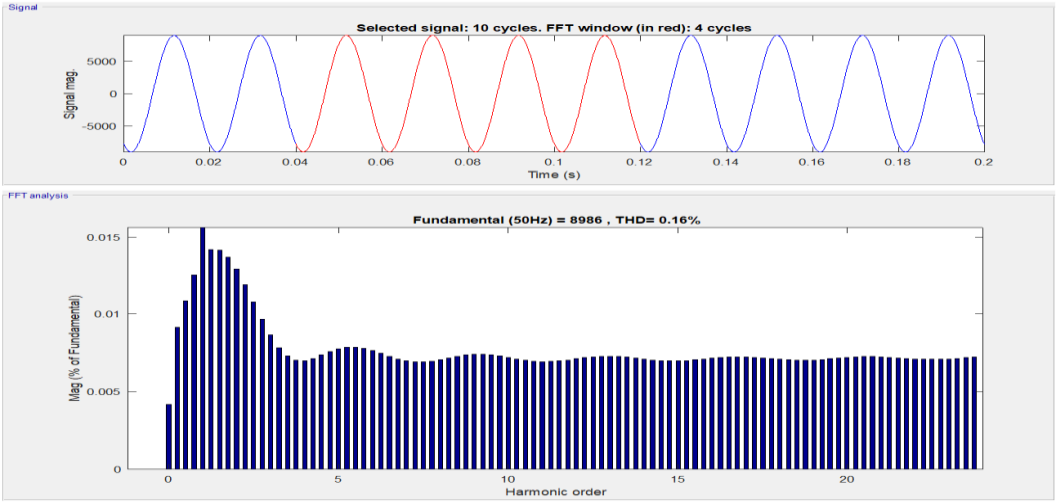

Figure 19:- FFT analysis of voltage waveform at11kV bus

IX. Comparative Analysis

At the switching instant, the voltage in the capacitor cannot change instantaneously. The bus voltage is pulled down, and then rises as the capacitor begins to charge. During the process, the capacitor voltage may overshoot. The comparative analysis of the THD percentage in each case is done and tabulated as below.

Table 1:- Back-to-back capacitor switching of 0.4kV capacitor at 0^0, 45^0 and 90^0 instants of R-phase:

Capacitor Switching Instant	THD % Without Pre-Insertion Resistor	THD % With 0.03Ω Pre-Insertion Resistor	THD % With 3Ω Pre-Insertion Resistor
Zero Degree	2.85	0.60	0.20
Fourty Five Degree	2.85	0.60	0.20
Ninty Degree	30.98	6.22	1.83

Table 2:- Back-to-back capacitor switching of 11kV capacitor at 0^0, 45^0 and 90^0 instants of R-phase:

Capacitor Switching Instant	THD % Without Pre-Insertion Resistor	THD % With 0.03Ω Pre-Insertion Resistor	THD % With 3Ω Pre-Insertion Resistor
Zero Degree	6.63	1.24	0.33
Fourty Five Degree	6.63	1.26	0.34
Ninty Degree	11.72	2.24	0.60

Table 3:- Isolated capacitor switching of 0.4kV capacitor at 0^0, 45^0 and 90^0 instants of R-phase:

Capacitor Switching Instant	THD % Without Pre-Insertion Resistor	THD % With 0.03Ω Pre-Insertion Resistor	THD % With 3Ω Pre-Insertion Resistor
Zero Degree	3.03	0.59	0.20
Fourty Five Degree	3.03	0.59	0.20
Ninty Degree	33.98	6.25	1.86

Table 4:- Isolated capacitor switching of 11kV capacitor at 0^0, 45^0 and 90^0 instants of R-phase:

Capacitor Switching Instant	THD % Without Pre-Insertion Resistor	THD % With 0.03Ω Pre-Insertion Resistor	THD % With 3Ω Pre-Insertion Resistor
Zero Degree	2.91	0.54	0.16
Fourty Five Degree	2.91	0.54	0.16
Ninty Degree	5.15	0.95	0.28

X. Conclusion

In this dissertation the voltage magnification phenomenon which originated from utility capacitor bank switching is simulated and studied. The characteristics of the switching transients coming from the utility system of the capacitor bank are analyzed. For customers having the power quality problems, these can be controlled by the different mitigation techniques as we have seen in the MATLAB simulation results. The information obtained from the simulations and results depicts that transients are produced in the current and voltage when capacitor banks are switched. Both Isolated switching and Back-to-back switching of capacitor bank is done. Magnified transients up to 2 p.u. are possible. It is observed that the transients are more at ninty degree switching instant and less at zero degree switching instant. Transients occurred during the energisation of capacitor bank under both isolated switching and back-to-back switching are successfully eliminated by using the pre-insertion resistor. The pre-insertion resistor technique of mitigation of voltage magnification caused by capacitor switching is most simple and less expensive technique applied in the real-world power utility. It can be concluded from the simulation results that the pre-insertion resistor techniques can remove the transients successfully.

References

[1] A. Kalyuzhny, S. Zissu and D. Shein, "Analytical Study of Voltage Magnification Transients Due to Capacitor Switching," in IEEE Transactions on Power Delivery, vol. 24, no. 2, pp. 797-805, April 2009, doi: 10.1109/TPWRD.2008.2002844.
[2] R. A. Adams, S. W. Middlekauff, E. H. Camm and J. A. McGee, "Solving customer power quality problems due to voltage magnification," in IEEE Transactions on Power Delivery, vol. 13, no. 4, pp. 1515-1520, Oct. 1998, doi: 10.1109/61.714840.
[3] Y. J. Gaikwad and A. R. Thorat, "Resistive Capacitive Switching Technique for the Mitigation of Power Capacitor Switching Transients," International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC), Melmaruvathur, India, 2019, pp. 109-112, doi: 0.1109/ICCPEIC45300.2019.9082389.
[4] D. S. Sargar, S. G. Kanade and S. S. Kunte, "Mitigation of Power Capacitor Switching Transients Using Resistive Capacitive Switching," International Journal of Current Engineering and Scientific Research (IJCESR), Volume-5, Issue-2, 2018.
[5] Katyara, Sunny. (2015). Analysis and Mitigation of Shunt Capacitor Bank Switching Transients on 132 kV Grid Station, Qasimabad Hyderabad.
[6] E. Contreras and I. León, "Simulation of Costumer Voltage Magnification due to Capacitor Switching Using EMTP," (2003).
[7] Mohammad, S.G. & Gomes, Chandima & AbKadir, M.Z.A. & Jasni, Jasronita & Izadi, Mahdi., "Protection technique for transient overvoltage due to capacitor bank switching in distribution systems using high pass filter," 10. 17151-17157.
[8] Tan, Rodney & Ramachandaramurthy, Vigna K.. (2015). A Comprehensive Modeling and Simulation of Power Quality Disturbances Using MATLAB/Simulink. 10.5772/61209.
[9] Iizarry-Silvestrini, M. F. and T. E. Vélez-Sepúlveda. "Mitigation of Back-to-Back Capacitor Switching Transients on Distribution Circuits." (2007).
[10] R. Deshmukh and V. R. Aranke, "Mitigation Techniques for Capacitor Bank Switching Transients," International Journal of Research in Electronics and Computer Engineering, Vol. 6 Issue 4 (October- December 2018).
[11] A. S. Dharmadhikari and A. A. Bhole, "Analysis and Mitigation Techniques of MV Capacitor Bank Switching Transients on 132 kV Substation," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 6, Issue 6, June 2017.
[12] A.J.. Schultz, I. B. Johnson, and N. R. Schultz, "Magnification of switching surges," AIEE Trans. Power App. Syst., vol. PAS-77, pp. 1418–1426, Feb. 1959.
[13] J. Zaborszky and J. W. Rittenhouse, "Fundamental aspects of some switching overvoltages on power systems," AIEE Trans. Power App. Syst., vol. PAS-82, no. 64, pp. 815–822, Feb. 1963.
[14] IEEE Application Guide for Capacitance Current Switching for AC High Voltage Circuit Breakers Rated on a Symmetrical Current Basis, ANSI/IEEE Std.C37.012–1979 (R2000), 1979.
[15] D. M. Dunsmore, E. R. Taylor, B. F. Wirtz, and T. I. Yanchula, "Magnification of transient voltages in multi-voltage-level-shunt-capacitor- compensated circuits," IEEE Trans. Power Del., vol. 7, no. 2,pp. 664–673, Apr. 1992.
[16] M F McGranaghan, et al, "Impact of Utility Switched Capacitors on Customer Systems Part IT - Adjustable Speed Drive Concerns," Presented at the 1991 IEEE-PES Winter Meeting, New York, New York, February 3 - 7, 1991.
[17] Blooming, T.M., Carnovale, D.J.: 'Capacitor application issues', IEEE Trans. Ind. Appl., 44, (4), pp. 1013–1026.
[18] Mitigation of power capacitor switching transients using resistive capacitive switching by Dhananjay S. Sargar Dr. Sanjay G. Kanade Soumitra S. kunte, ISSN(PRINT): 2393-8374,(ONLINE): 2394-0697, Volume-5, Issue-2,2018.
[19] Teymoor Ghanbari et al. "Three-phase resistive capacitor switchingtransient limiter for mitigating power capacitor switching transients," IET Generation, Transmission & Distribution, pp. 1-12, The Institution of Engineering and Technology 2015.
[20] Skeans, D.W.: 'Recent development in capacitor switching transient reduction'.Proc. T&D World Expo. Substation Section, pp. 1–13