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Synthesis and Timing Analysis of an Automatic Coffee/Tea Vending Machine

[1]Meghana M
PG student, VLSI and Embedded Systems
Dept. of ECE,
B.N.M. Institute of Technology
Bangalore, India

[2]Dr. P. A. Vijaya
Professor and Head
Dept. of ECE,
B.N.M. Institute of Technology
Bangalore, India

Abstract: Vending Machine is a machine which can vend different products which is an automated process with no requirement of manual handling, which are mostly widely used due to fast lifestyle. In this paper, a FSM based automatic coffee/tea vending machine is designed and synthesized using Verilog. In order to make sure that the machine works effectively in real time, timing analysis is done on the design with some timing constraints. The design synthesize is done on Cadence, and the timings analysis are done in Cadence Genus tool. The end results of this project shows that the machine works efficiently for the given inputs at expected time and the design also has a positive slack after performing timing analysis with some constraints.

***Index Terms* – Vending Machine, FSM Model, Synthesis, Timing Analysis, Cadence Genus tool.**

I. INTRODUCTION

Vending Machine is a machine which dispenses items such as coffee, tea, snacks, beverages, alcohol, cigarettes, lottery tickets, consumer products and even gold and gems to customers automatically, after the customer inserts currency or credit into the machine**.** These steps would not be time consuming at all but the time at which the vending machine respond to the stimulus is very important and critical. So it is necessary to make it more accurate with respect to timing constraints. The designed vending machine will provide Coffee or Tea to the people on the insertion of a 5 Rupee coin, using extremely simple steps. Note that the machine not return the coin back if no inputs are selected.

A. Finite State Machine

A finite state machine (FSM) or finite state automation, or simply a state machine is a mathematical abstraction sometimes used to design digital logic or computer programs. It is a behavior model composed of finite number of states, transitions between those states, and actions, similar to a flow graph in which one can inspect the way logic runs when certain conditions are met. Any sequential digital circuit can be converted into a state machine using state diagram. In a state diagram the circuit’s output is defined in a different set of states i.e. each output is a state. There is a state register to hold the state of the machine and a next state logic to decode the next state. There is also an output register that defines the output of the machine. The next state logic is the sequential part of the machine and the output and current state are the register part of the logic. There are two types of state machines: 1) Moore Machine 2) Mealy Machine. A Moore Machine is a machine whose output values are determined solely by its current state, whereas Mealy Machine is a machine whose output values are determined both by its current state and by the values of its inputs. The Mealy machine model is shown in Figure 1. The proposed algorithm for vending machine is a sequential circuit which is based on Mealy Model.

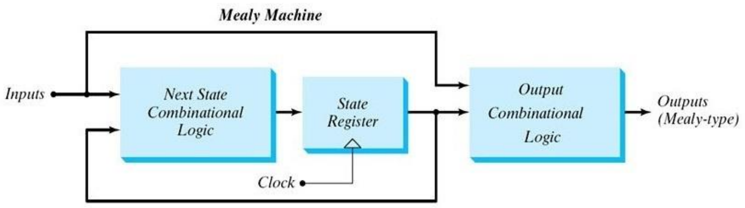


Figure 1. Mealy Model

B. Synthesis

Synthesis is a process that transforms a simple RTL design into a gate level netlist with all types of constraints that are specified by the designer. This process has certain goals: to generate a gate level netlist, to insert clock gates for power optimization, to optimize the area logically and to maintain the logical equivalence between RTL and Netlist. There are 3 processes in synthesis. 1) Translation: converts the RTL code to Boolean expression 2) Mapping: cells are mapped to standard cells of the library 3) Logic optimization: Synopsys Design Constraint (SDC) files are generated to help optimization and achieve the targeted time, power and area. Synthesis are of 2 types. 1) Logical synthesis: Process of converting a high level description of design into an optimized gate-level representation and the circuit description is written in HDL such as Verilog. The output SDC file obtained in this process is further used for physical synthesis process. 2) Physical synthesis: Transforms gate level net list to layout that can be realized/etched on silicon. In this paper we are discussing with respect to logical synthesis.

C. Timing Analysis

Timing analysis is a method of validating the timing performance of a design by checking all possible paths for timing violations without having to simulate, generating vectors and functionality checks. Timing is important to verify how fast the designed chip runs, and interacts with other chips. To ensure the timing of a chip is accurate as the targeted time, certain timing constraints are applied to the design and the analysis is done. Getting a positive slack is the main aim in timing analysis as it indicates the correct timing functionality of the design.

D. Programming language and Software

The design described in this paper is done in Verilog, which is standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction. It is also used in the verification of analog circuits and mixed-signal circuits, as well as in the design of genetic circuits. The designed code is simulated on Cadence platform which is a leading provider of EDA and semiconductor IP. Its custom/analog tools help engineers design the transistors, standard cells, and IP blocks that make up SoCs. The timing analysis is done using Cadence Genus Synthesis Solution which is a next-generation RTL synthesis and physical synthesis tool that delivers up to a 10X boost in RTL design productivity with up to 5X faster turnaround times.

II. DESIGN IMPLEMENTATION

In this paper, an automatic vending machine is constructed in terms of state diagrams with the help of Cadence tool. The customer can get two different types of products of same prices, namely Coffee and Tea. The prices of these products are Rupees 5. The code is written and synthesized in Verilog HDL. The synthesis and timing analysis report is generated using Cadence Genus Tool.

A. State Diagram

An automatic coffee/tea vending machine is designed based on the FSM model shown in Figure 2. The state machine has four states, 'wait for coin insert', ''wait for user input', 'dispense coffee' and 'dispense tea'. The event 'insert coin', transitions the state to 'wait for user input'. The system stays in this state until a user is received from the button "pu_coffee" and "pu_tea". Depending on the input, coffee or tea is dispensed. If coffee or tea is not selected, the machine doesn't return the coin back, it returns to its previous state of 'insert coin'. After dispensing tea or coffee, the machine returns to its initial state of 'insert coin'.

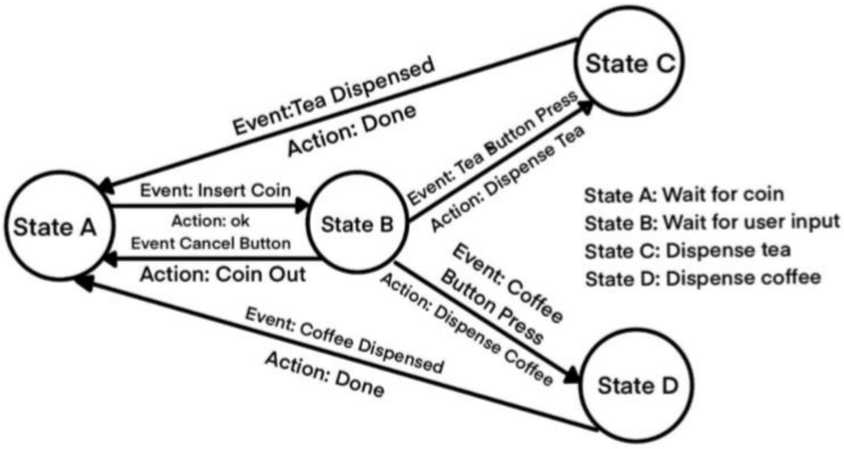


Figure 2: FSM for vending machine

III. SIMULATION RESULTS

The designed Verilog code is simulated and synthesized in Cadence. The following desired results are obtained. Figure 3 – 6 shows the waveforms obtained for different cases as the machine enters different states. The RTL schematic of the design is as shown in Figure 7.

Note: Price of Coffee/tea is Rs. 5

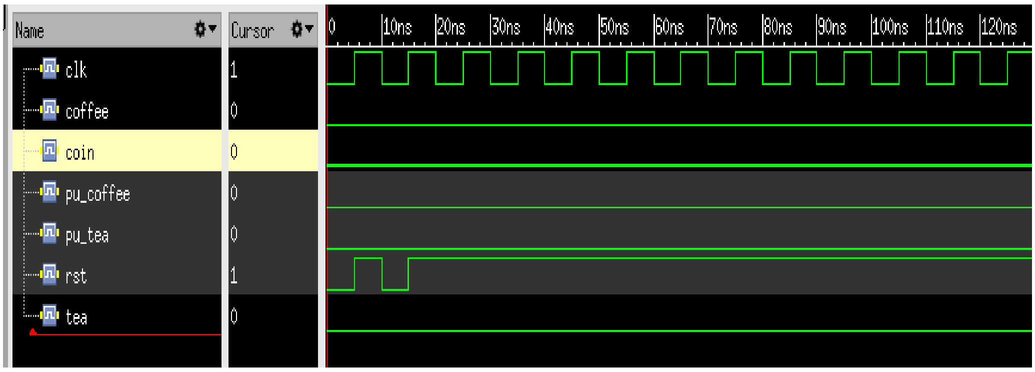


Figure 3: Output waveform when the machine is in State A i.e., initial condition of the vending machine

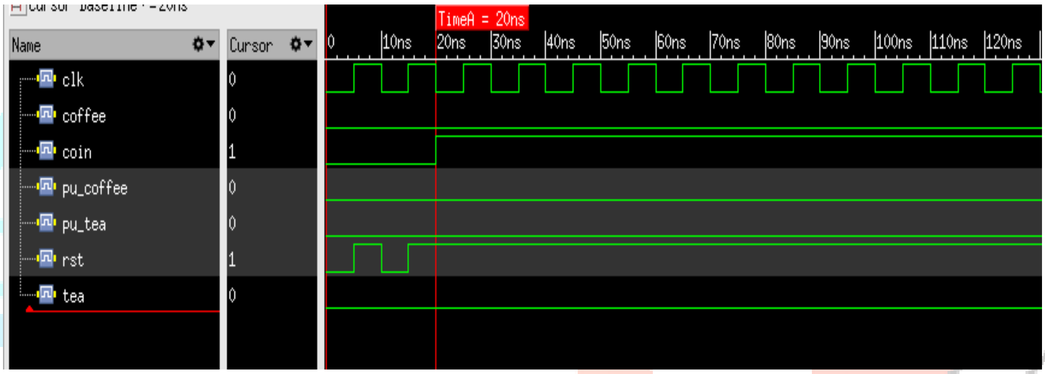


Figure 4: Output waveform when the machine is in State B i.e., a coin is inserted and neither coffee nor tea are selected

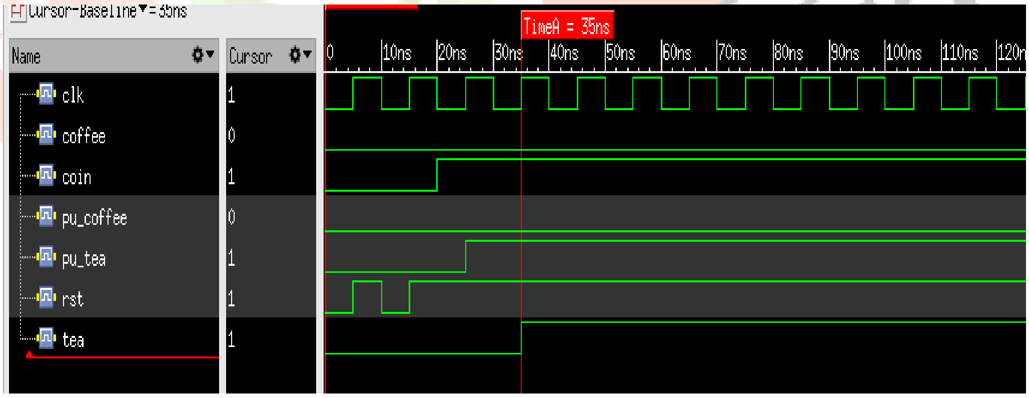


Figure 5: Output waveform when the machine enters State C i.e., coin is inserted, user selects tea, and machine dispense Tea

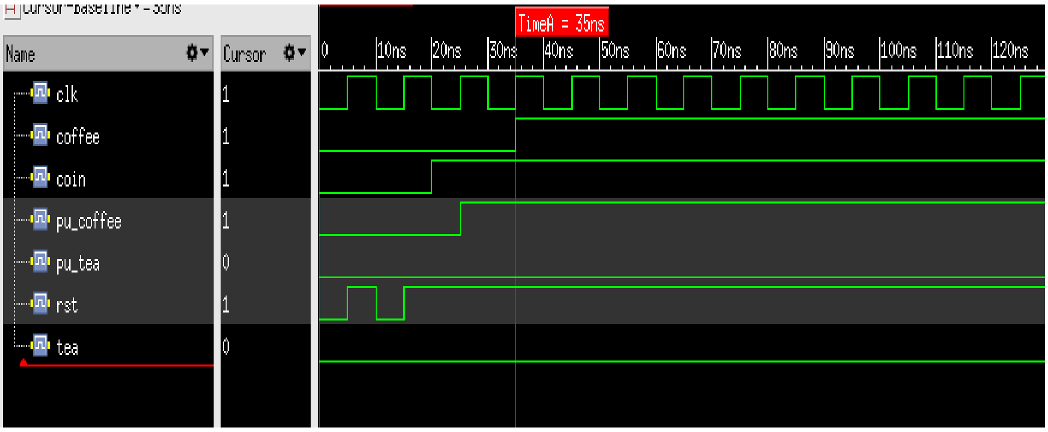


Figure 6: Output waveform when the machine enters State D i.e., coin is inserted, the user selects coffee, and machine dispense Coffee

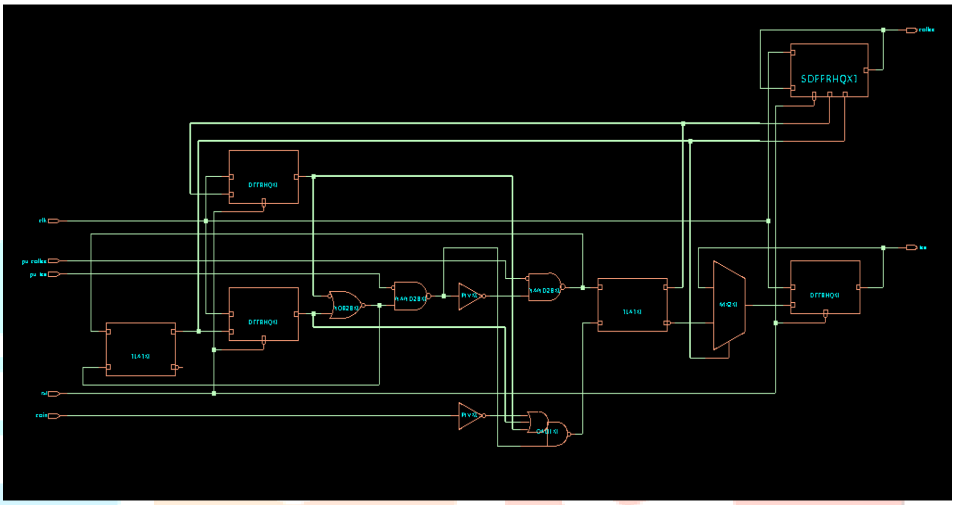
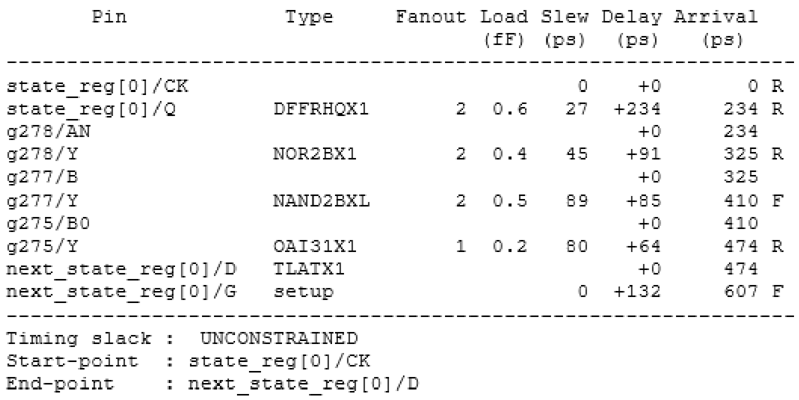


Figure 7: RTL Schematic of the Verilog design obtained from Cadence tool

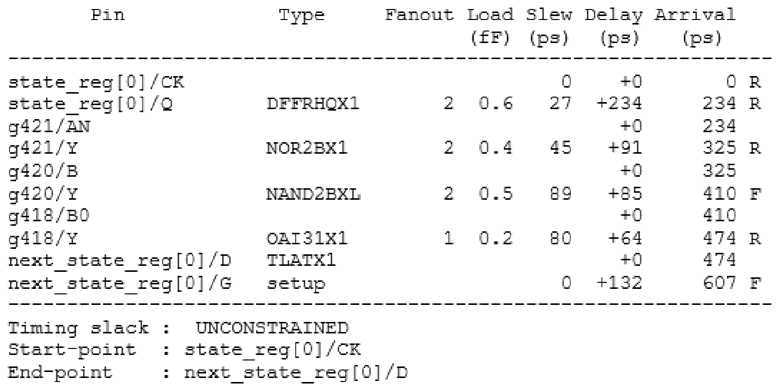
IV. TIMING REPORTS

Timings analysis is done by giving certain timing constraints and the following are the reports. Figure 8 shows a general timing report obtained without any timing constraints where the timing slack is not constrained. Figure 9 shows the timing report with constraints applied such as effort medium. The timing slack is still unconstrained. Figure 10 shows a constrained timing report with clock and effort high. Clock is constrained by creating a clock of period 0.5. The reports shows that the capture arrival is 500R and the setup arrival is 437R with timing slack as 63ps. Figure 11 is a report obtained when the clock is optimized with uncertainty of 0.01, maximum input delay is 0.1 along with the effort high. The reports show that the setup time is increased from 437 to 457 while the uncertainty delay is -10 which leaves the timing slack to reduce to 33ps. Figure 12 shows with similar constraints as in Figure 11 except that the output delay is constrained instead of input delay. The timing slack still remains the same. At the end of the analysis, the timing slack is said to be positive as shown in Figure 13.



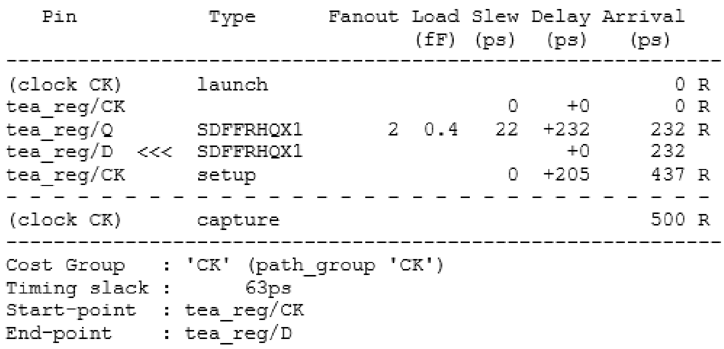
```
       Pin              Type      Fanout  Load Slew Delay Arrival
                                          (fF) (ps)  (ps)   (ps)
-----------------------------------------------------------------
state_reg[0]/CK                                  0    +0      0 R
state_reg[0]/Q        DFFRHQX1        2    0.6  27  +234    234 R
g278/AN                                             +0    234
g278/Y                NOR2BX1         2    0.4  45   +91    325 R
g277/B                                              +0    325
g277/Y                NAND2BXL        2    0.5  89   +85    410 F
g275/B0                                             +0    410
g275/Y                OAI31X1         1    0.2  80   +64    474 R
next_state_reg[0]/D   TLATX1                        +0    474
next_state_reg[0]/G   setup                      0  +132    607 F
-----------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : state_reg[0]/CK
End-point    : next_state_reg[0]/D
```

Figure 8: General timing report without any timing constraints.



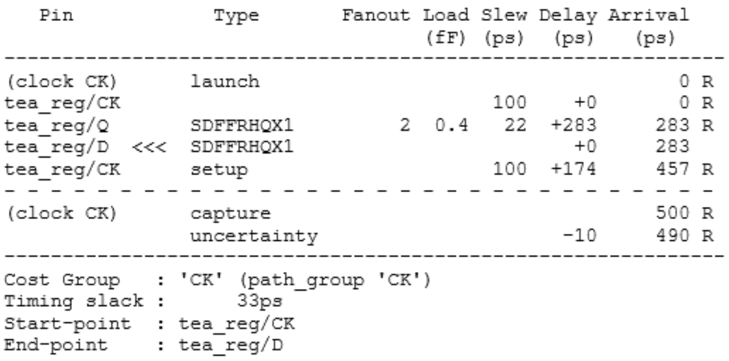
```
       Pin              Type      Fanout Load Slew Delay Arrival
                                          (fF) (ps)  (ps)    (ps)
-----------------------------------------------------------------
state_reg[0]/CK                                    0    +0       0 R
state_reg[0]/Q        DFFRHQX1      2  0.6   27  +234     234 R
g421/AN                                             +0     234
g421/Y                NOR2BX1       2  0.4   45   +91     325 R
g420/B                                              +0     325
g420/Y                NAND2BXL      2  0.5   89   +85     410 F
g418/B0                                             +0     410
g418/Y                OAI31X1       1  0.2   80   +64     474 R
next_state_reg[0]/D   TLATX1                        +0     474
next_state_reg[0]/G   setup                   0  +132     607 F
-----------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : state_reg[0]/CK
End-point    : next_state_reg[0]/D
```

Figure 9: Timing report with effort medium



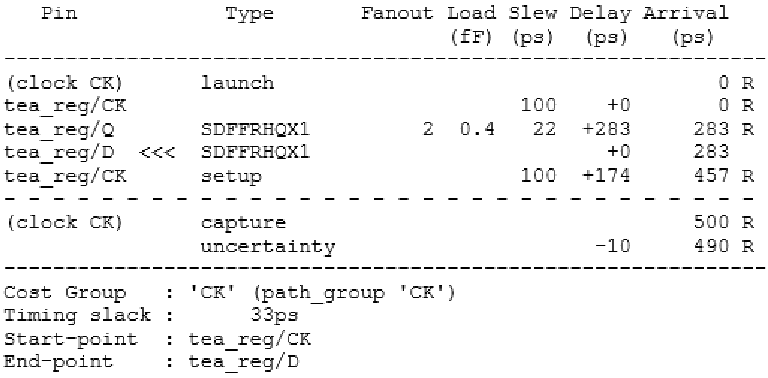
```
   Pin            Type       Fanout Load Slew Delay Arrival
                                    (fF)  (ps)  (ps)   (ps)
------------------------------------------------------------
(clock CK)       launch                                 0 R
tea_reg/CK                                  0     +0     0 R
tea_reg/Q        SDFFRHQX1       2   0.4   22   +232   232 R
tea_reg/D   <<<  SDFFRHQX1                       +0   232
tea_reg/CK       setup                      0   +205   437 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock CK)       capture                              500 R
------------------------------------------------------------
Cost Group   : 'CK' (path_group 'CK')
Timing slack :      63ps
Start-point  : tea_reg/CK
End-point    : tea_reg/D
```

Figure 10: Timing report with constrained clock and effort high



```
   Pin            Type       Fanout Load Slew Delay Arrival
                                    (fF)  (ps)  (ps)   (ps)
------------------------------------------------------------
(clock CK)       launch                                 0 R
tea_reg/CK                                100     +0     0 R
tea_reg/Q        SDFFRHQX1       2   0.4   22   +283   283 R
tea_reg/D   <<<  SDFFRHQX1                       +0   283
tea_reg/CK       setup                    100   +174   457 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock CK)       capture                              500 R
                 uncertainty                    -10   490 R
------------------------------------------------------------
Cost Group   : 'CK' (path_group 'CK')
Timing slack :      33ps
Start-point  : tea_reg/CK
End-point    : tea_reg/D
```

Figure 11: Timing report with optimized clock, input delay, and effort high



```
   Pin            Type       Fanout Load Slew Delay Arrival
                                    (fF)  (ps)  (ps)   (ps)
------------------------------------------------------------
(clock CK)       launch                                 0 R
tea_reg/CK                                100     +0     0 R
tea_reg/Q        SDFFRHQX1       2   0.4   22   +283   283 R
tea_reg/D   <<<  SDFFRHQX1                       +0   283
tea_reg/CK       setup                    100   +174   457 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock CK)       capture                              500 R
                 uncertainty                    -10   490 R
------------------------------------------------------------
Cost Group   : 'CK' (path_group 'CK')
Timing slack :      33ps
Start-point  : tea_reg/CK
End-point    : tea_reg/D
```

Figure 12: Timing report with optimized clock, output delay, and effort high

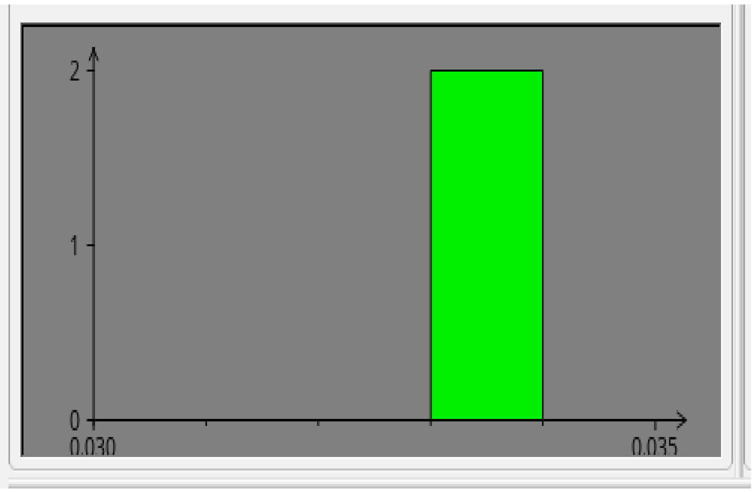


Figure 13: Positive timing slack graph for the design

V. CONCLUSION

The results prove that the vending machine will deliver the desired product for the given inputs. And also, the machine is optimized with respect to time to perform in high speed. It is also observed that the design gives a positive slack for the optimization done. It is always good to have positive slack rather than having zero slack. This is because in further process of chip design (like in backend) there may slight timing variations which can be accommodated if there is a positive slack.

VI. FUTURE SCOPE

Some of the future scope for this work are listed below:

i. Timing analysis on the design after physical synthesis can be done and the timing reports can be compared to check if the design meets the required constraints.
ii. Power optimization can be performed by constraining leakage power.
iii. Hardware implementation using FPGA can be done to ensure the design works in real time.
iv. The design can be modified and extended for other types of products.

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