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Design and Implementation of Vending Machine Using Verilog HDL

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Abstract:

In this brief, we have implemented vending machine using Verilog. The Verilog code is implemented on FPGA (Xilinx basys3). This machine acknowledges both either cash (money) or card (credit). In the present work, we have designed the Vending machine with the assistance of a mealy machine state chart. The configuration is demonstrated utilizing Verilog HDL dialect which is a hardware description language used to portray the computerized framework. The model is validated by performing the suitable experiments in a test-bench. The Verilog code created for vending machine model and implemented using Xilinx Vivado. The Vending machine we planned can be utilized by both cash and card. The card framework will be more practical and aides for a rapid access. The target here is to outline a proposed vending machine which acknowledge cash or card as inputs and conveys the items at that obliged sum has been stored furthermore returning back the change. It is conceivable to withdraw the stored cash during the process if the client wishes after squeezing a cross out cash. In this work, we have designed a vending machine with less construction modelling when compared to similar work performed using IOT thereby reducing power consumption.

Keywords: FPGA; vending machine; Xilinx basys3; Xilinx Vivado; Verilog HDL.

Introduction:

Vending machines are utilized to pick-up different items like espresso, beverages, postcards, and gums when cash is embedded into it. The vending machines are more sensible and functional than the traditional methods of picking the items. The vending machines can be used in schools, universities, rail route stations, and airplane terminals for offering tickets and drinks. They are also used in banks for providing tokens to the clients. The vending machine can be utilized at different places like schools, universities, and rail route stations. These machines reduce cost, time, and work.

Vending machine using IOT and embedded systems has become outdated. In the 21st century growth of VLSI industry has been rapidly evolving; therefore, making vending machines using hardware descriptive language of VLSI as the novel idea of this work. The present model is validated for the simulations against the experimental results obtained using FPGA. The results obtained using simulations through Xilinx are in good agreement with the experimental results obtained using FPGA (basys3).

The work in this paper is organized into three sections. The first section is the introduction, followed by the results and discussions in the second section. The third section represents the conclusion highlighting the utility of the present work.

Table 1
State table for withdrawing an item of 100 INR cost

CURRENT STATE	100 RS	25 RS	CHANGE	NEXT STATE	OUTPUT
S0	0	0	0	S0	0
	0	1	0	S25	0
	1	0	0	S100	0
	1	1	25	S125	1
S25	0	0	0	S0	0
	0	1	0	S50	0
	1	0	25	S125	1
	1	1	50	S150	1
S50	0	0	0	S50	0
	0	1	0	S75	0
	1	0	0	S100	1
	1	1	75	S175	1
S75	0	0	0	S0	0
	0	1	0	S100	1
	1	0	75	S175	1
	1	1	100	S200	1
S100	0	0	0	S100	1
	0	1	25	S125	1
	1	0	100	S200	1
S125	0	0	0	S0	0
S150	0	0	0	S0	0
S175	0	0	0	S0	0
S200	0	0	0	S0	0

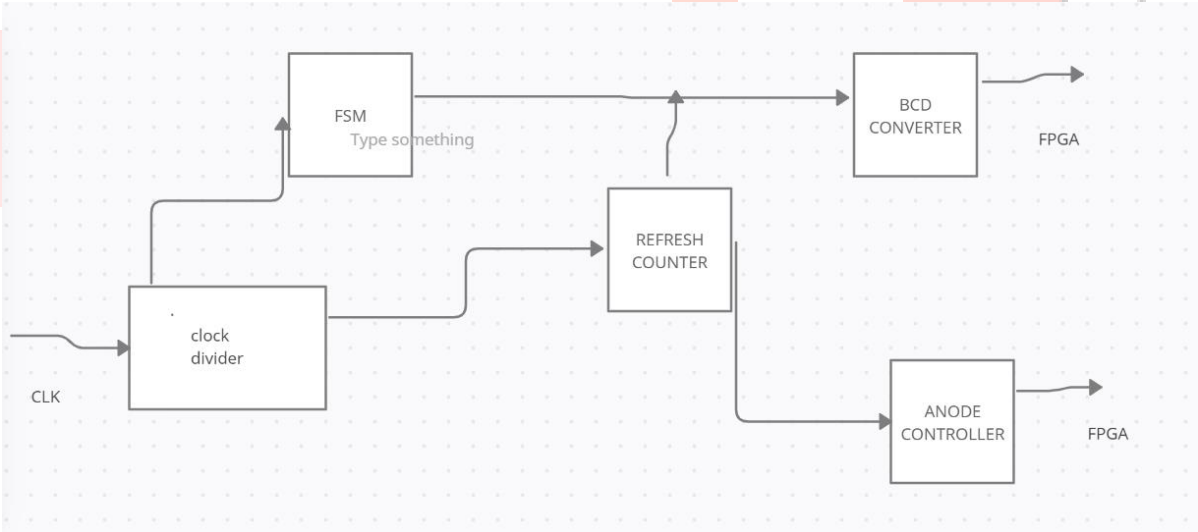

Fig. 1: Block diagram of vending machine

Description of different blocks of the vending machine

(a) Clock divider

Clock divider is an input signal of frequency F_{in} with an output signal of frequency F_{out}, expression as $F_{out}= F_{in}/n$; where n is the interior frequency divider.

Results And Discussions:

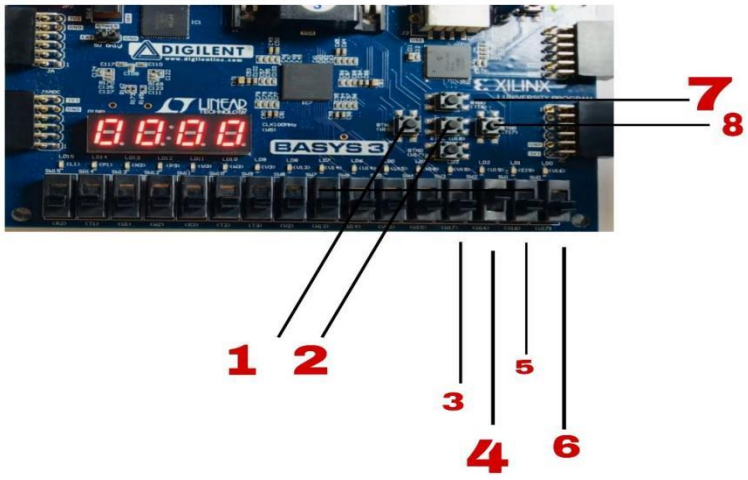

Fig. 2: Description of inputs and outputs of vending machine

The above-mentioned image description as follows:
If 1 is pressed it indicated the insertion of rupees 100
If 2 is pressed it represents OK
If 3 is pressed it represents the selection of items worth rupees 200
If 4 is pressed it represents the selection of items worth rupees 150
If 5 is pressed it represents the selection of items worth rupees 75
If 6 is pressed it represents the selection of items worth rupees 25
If 7 is pressed it represents RST
If 8 is pressed it indicated the insertion of rupees 25

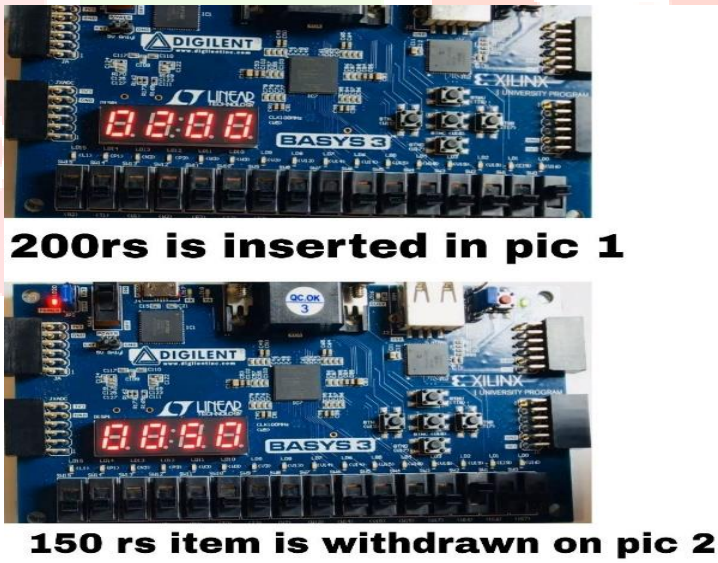

Fig. 3: Demonstration of inserting rupees 200 and withdrawing items worth rupees150

200 rs is inserted on pic 1

25 rs item is drawn on pic 2

Fig. 4: Demonstration of inserting rupees 200 and withdrawing items worth rupees 25

Simulation results

Fig. 5: Simulated waveform of vending machine using Xilinx Vivado

For every rising edge of the clock the input checks for rupees 100 and 25 simultaneously. If any one of them is active high then it checks for the items, we tend to select items of worth rupees 200, 150, 75 or 25. If any of these items are selected then output is drawn and change is given respective to it and accordingly displayed by the Xilinx basys3 FPGA.

Conclusion

The objective of the present work is the implementation of vending machine using Verilog HDL. This task is accomplished through Xilinx Vivado with few modules that includes clock divider, FSM, refresh counter, BCD convertor, and anode/cathode controller. The output of the vending machine is derived in Xilinx Vivado. Xilinx basys3 is used for the hardware implementation. The utility of the present work has wide range of opportunities in public domain like malls, cafeteria, universities, parks, airports for distribution of snacks, fare-tickets, etc.

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