



Design of a Two-Bit Magnitude Comparator Based on Pass Transistor, Transmission Gate and Conventional Static CMOS Logic

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Abstract: In recent years, low power has emerged as an attractive target for high-level VLSI circuits. A 2-bit GDI-based Magnitude Comparator has also been suggested and implemented utilizing modified GDI semiconductors in order to satisfy something quite comparable at the highest spot on the demand list. In cutting-edge VLSI setup circuits, comparators are a necessary component. In the present instances, reduced devices are motivated by a demand for low power and a smaller on-chip space. Using Modified GDI innovation, we present a new Magnitude Comparator for adjusting the range of lower supply voltages. In terms of varied pattern boundaries, the suggested GDI approach based degree comparator has the benefit of requiring less management. When compared to a standard CMOS size comparison, fewer semiconductors are predicted to be present. Tanner EDA Tool version 12.6 at 45nm cycle innovation is used to frame and simulate both circuits.

Index Terms - VLSI, GDI semiconductors, Pass Transistor, Transmission Gate and Conventional Static CMOS Logic.

I. INTRODUCTION

In recent times, the market revenue for circuit planning has been driven by three things: low power, fast, and a small geography. Therefore, increased demand for low-power, rapid implanted systems used in mobiles, tablets, etc., has led to downsized innovation to Nano regimes, which make it possible to complete more versatility on one chip. The greatness comparator is an essential component of computerized systems. Organizing is currently by and large an imperative issue in programming. Coordinating is important for chief interaction, for example in correspondence and registration. Managing data issues can be understood by comparing, where comparing plays an important role in the areas of equal handling, multiprocessing, and multi-access recollections. A greatness In the field of industry, the greatness comparator is also used as part of a Digital Signal Processor (DSP) for handling data, a chip for deciphering guidance, and a microcontroller for controlling the temperature of heaters.

1.1 COMPARATOR

The comparator's basic capability is to consider two n-bit values and decide on a result based on the correlation findings. The outcome can be one of the three possible outcomes, i.e., whether and which number is more prominent, equivalent to, or less prominent. Three paired variables that show if $A > B$, $A = B$, or $A < B$ address the aftereffect of correlation.

The Circuit for a 2-Bit Degree Comparator is shown in Figure 1. It observes two integers. If $A > B$, F1 counterparts to 1 are produced; if $A = B$, F2 reciprocals are produced. Furthermore, if $A < B$, F3 is equivalent to 1. Table 1.1 contains the truth table for the 2-Bit degree comparator. Comparator may be used in a few different Logic ways. Different kinds of use include a High Execution MUX based CMOS comparator, Comparator Hybridizing PTL reasoning, and Pseudo reasoning. Complementary CMOS Logic can typically implement a 2-bit comparator with 66 semiconductors.



Figure 1.1 2-Bit extent comparator

1.1 Truth table:

A1	A0	B1	B0	F3	F2	F1
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0

0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Table1.1

$F1 = A1' B1 + A0' B0 (A1 B1 + A1 B1)$ -1
 $F2 = (A1' B1' + A1 B1) (A0' B0' + A0 B0)$ -2
 $F3 = A1 B1' + A0 B0' (A1' B1' + A1 B1)$ -3

1.2 CONVENTIONAL CMOS MAGNITUDE COMPARATOR:

The Logic Function of the Magnitude Comparator can be recognized usually using 66 Transistors as showed up in Fig 1.2 As it uses more number of semiconductors it includes a more area and more will be the Power Dissemination.

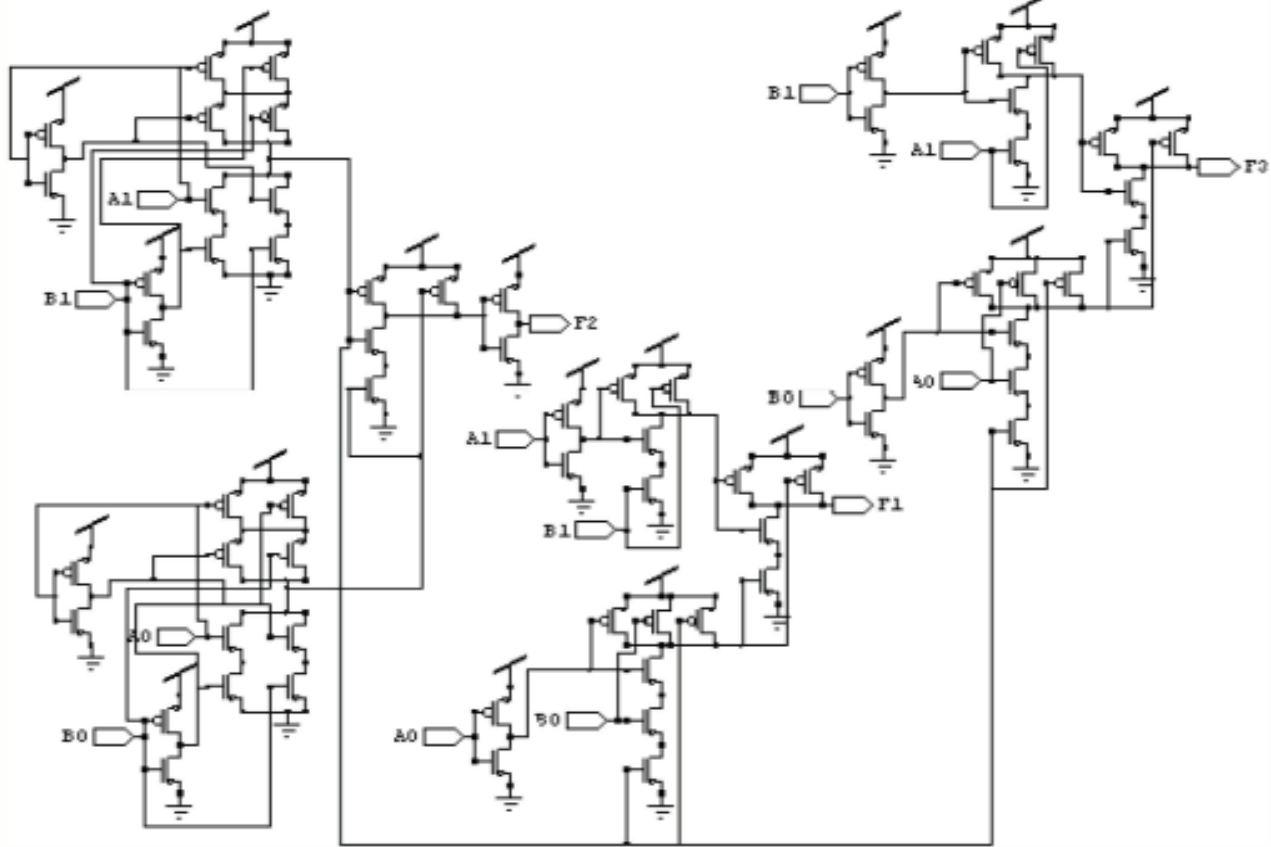


Figure1.2: CMOS 2-bit Magnitude Comparator

II. LITERATURE SURVEY

2.1 Gate Diffusion Input (GDI):

Entryway Diffusion Input (GDI) is a Technique with which a wide number of combinational limits can be executed with only 2 MOS semiconductors. Focal points of GDI strategy are high throughput, low control usage and low zone as this technique decreases the semiconductor check. Fundamental Cell of GDI resembles a major CMOS inverter. G, P and N are considered as commitments to the GDI Cell.

- G is the data associated typical to the entrance terminals of NMOS and PMO
- N input is associated with source/Drain of NMOS
- P input is associated with the source/drain of PMOS

The execution of a high level circuit is decided by its speed in making yield when an info is given to it. The most notable development for arranging progressed circuits is the CMOS innovation. Auer the improvement of CMOS rationale, there was extending need to upgrade circuit as far as speed. One framework considered was by using Pass Transistor Technology (PTL) which impacts use of lesser number of doorways to acknowledge to an activity. The Transmission Gate (TG) is one of them which are regularly a blend of NMOS and PMOS semiconductors associated in equal. The GDI cell represents to one more kind of pass semiconductor innovation which seems to be indistinguishable from CMOS yet fluctuates in the stock provided for the info terminals. The standard inclinations of PTL over normal CMOS setup are according to the accompanying 1) less number of semiconductors gives it low power scattering and lesser postponement. 2) Lesser number of semiconductors so low region and lesser interconnect impacts. In any case, PTL propels also experience the evil impacts of two essential issues, for instance, decreased circuit speed at low power activities and more important static power scattering.

GDI method that can be used to design fast, low power circuits using only several semiconductors. The GDI cell resembles a CMOS inverter structure. In a CMOS inverter the piece of the PMOS is related with VDD and the wellspring of NMOS is grounded. However, in a GDI cell this may not actually occur. There are a few imperative differences between the two.

Larger piece of both NMOS and PMOS are related with N or P (independently) that is all there is to it can bediscretionarily uneven not in any manner like in CMOS inverter. Also, the most fundamental difference among CMOS and GDI is that in GDI N, P and G terminals could be given an inventory 'VDD' or can be grounded or can be given information signal dependent upon the circuit to be created and hence effectively restricting the amount of semiconductors used as a piece of case of most rationale circuits

2.2 BASIC GDI CELL

A Basic GDI cell contains four terminals - G (the common input of the NMOS and PMOS semiconductors), P (the external scattering center point of the PMOS semiconductor), N (the outer scattering center of the NMOS semiconductor) and the D center point (the typical dispersion of the two semiconductors). P, N and D may be used as one or the other info or result ports, dependent upon the circuit structure. Table 2.2.1 shows how unique plan changes of the information sources P, N and G in the fundamental GDI cell connect with different Boolean capacities at the result D GDI enables easier entryways, cut down semiconductor number incorporate, and low power scattering various executions, as contrasted and standard CMOS and Pass-semiconductor Logic (PTL) frame methods .

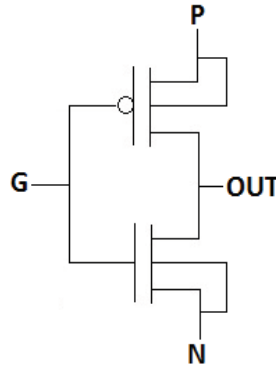


Fig 2.2 Basic GDI cell

Table 2.2.1 some logic functions that can be implemented with a single GDI cell

N	P	G	D	Function
'0'	B	A	HB	F1
B	'1'	A	H + B	F2
'1'	B	A	A + B	OR
B	'0'	A	AB	AND
C	B	A	HB+AC	MUX
'0'	'1'	A	H	NOT

When compared with other logic styles implemented using CMOS, Transmission gates and NMOS pass gate GDI is found to be advantageous with high performance or speed, low power consumption and low silicon on chip area.

2.3 OPERATIONAL ANALYSIS

The most broadly perceived issue with PTL framework is its low voltage swing. An extra help equipment may be used besides to clear out the issue of low swing and push ahead drivability. The issue of low swing can be appreciated with the help of an inconsistent limit displayed in table

Table 2.3.1 GDI truth table for inverter

Functionality Of any Random Function using GDI A	B	Functionality	Logic
A	B	Y	
0	0	pMOS Trans Gate	V _{tp}
0	1	CMOS Inverter	1
1	0	nMOS Trans Gate	0
1	1	CMOS Inverter	0

The issue of low swing happens just when A=0 and B=0 where the voltage level is V_{TP} rather than 0. This happens because of the poor high to low progress attributes of PMOS. In whatever is left of the cases it gives full swing.

2.4 MODIFIED GDI TECHNIQUE

Despite the fact that GDI has several advantages, its execution deteriorates when employed below 90nm. In the conventional CMOS method, fundamental GDI suffers some few fundamental restrictions such as swing corruption and fabrication complexity. It is preferred to defeat these Modified GDI. Platform ends of PMOS and NMOS are connected to VDD and GND independently in Modified GDI, as shown in Fig 2.4.1

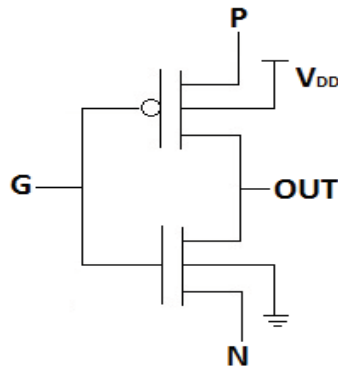


Fig 2.4.1 Modified GDI cell

Altered GDI is Compatible for CMOS manufacture Process. Spillage streams can be seen in sub-limit headways. Adjusted GDI Provides broad reduction of both sub-breaking point and door spillage streams stood out from static CMOS Process.

2.5 OPERATIONAL ANALYSIS OF MODIFIED GDI CELL

N	P	G	OUT	Function
B	A	A	AB	AND
A	B	B	A+B	OR
B	A	Sel	Sel'A+SelB	MUX

The operational analysis of AND gate is presented.

2.6 PROPOSED 2- BIT MAGNITUDE COMPARATOR

New Region effective Designs for extend comparator with 18 semiconductors is provided. Method Is introduced GDI Magnitude Comparator Schematic Illustration

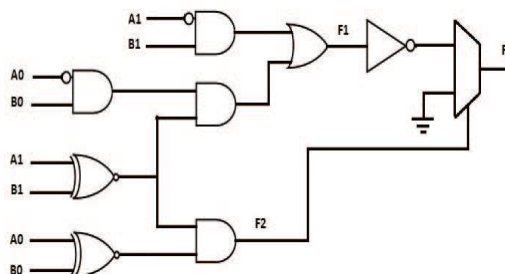


Fig 2.6.1 Block Diagram of proposed 2-Bit Magnitude Comparator

III. PASS TRANSISTOR AND TRANSMISSION GATE

3.1 Pass Transistor

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between node so circuit, instead of as switches connected directly to supply voltages.[1] This reduces the number of active services, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input.[2] If several devices are chained in series in a logic

path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

3.2 An Example of Pass-Transistor Logic

It is possible to use a single NMOS transistor as a PTL switch; the switch is considered closed when the voltage applied to the gate is logic high, and it is considered open when the voltage applied to the gate is logic low. The following diagram shows an AND gate (or at least something similar to an AND gate) that uses only one transistor.

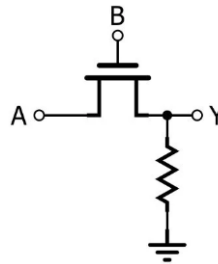


Figure – 3.1: Pass Transistor

The output (Y) is logic high when the input (A) is logic high and the switch-control signal (B) is logic high, and it is not logic high for all other combinations. That sounds like the AND truth table, but can we really call this an AND gate? That depends on your perspective. The problem is that the circuit doesn't drive a logic low when the B input is logic low. It's simply disconnected, i.e., floating. To establish a logic low, we need a pull-down resistor: Now we have a functional AND gate, and we've used only one transistor and one resistor, whereas a standard CMOS-inverter-based AND gate requires six transistors. However, the PTL circuit is by no means equivalent to the standard CMOS version. First of all, it does not reliably provide a low-resistance path to ground. Second, it dissipates static power whenever the output is logic high—current flows from the input, through the NMOS, through the pull-down resistor, to ground.

This means that we have lost an extremely beneficial property of inverter-based logic, namely, that the power supply delivers significant amounts of current only during switching. (That's why CMOS power dissipation is proportional to frequency—more switching means more current, and more current means more power.)

3.3 NMOS vs. CMOS in Pass-Transistor Logic

As demonstrated in the preceding section, PTL is built around MOSFET switches that either pass (hence the name) or block a signal. Using an NMOS transistor as the switch is certainly a good way to reduce transistor count, but a lone NMOS isn't impressive in terms of performance. A much better solution is the CMOS transmission gate:

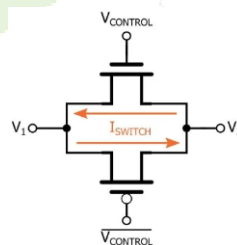


Figure 3.2: shows the symbol of a transmission gate with input and output terminals and the controlling gate terminal.

The lone NMOS and the CMOS transmission gate are briefly compared in this article. There's no doubt that the transmission gate is, in general, the superior implementation, but consider the trade-off. Obviously an additional transistor is required, but note also that the PMOS is driven not by the switch-control signal but by the complement of the switch-control signal. This is not a problem if the circuit that generates the input signal is, for example, a D flip-flop that provides both a Q and a \sim Q output. Usually, though, only one input signal is available, and in such cases the use of a CMOS transmission gate means that we must also have an inverter to create the control signal for the second FET.

3.4 Assessing Pass-Transistor Logic

At this point you may be wondering why I bothered to write an article about such a decidedly mediocre version of MOSFET-based digital logic. The overwhelming dominance of standard CMOS circuitry is enough to confirm that PTL has limited usefulness. However, it's critical to understand that carefully designed PTL implementations can provide acceptable functionality while reducing transistor count. Even if the reduction is small relative to an individual sub circuit, such as an XOR gate or a flip-

flop, the overall effect can be significant in a device that includes thousands of identical sub circuits. In a follow-up article I'll present advantageous PTL versions of widely used digital circuits.

IV. DISCUSSION ON RESULT

Because innovation is altering at such a rapid pace, it is critical to create and develop new techniques or circuits that reduce control usage and zone. A novel technique is presented for the design and execution of a 2-bit Magnitude comparator employing a superior GDI method, namely the Modified GDI method in terms of power and area. The framework employing Modified GDI approach distinct from Conventional CMOS and current GDI comparator gives an astounding charge decrease and reduced on-chip space performed in 45nm interaction development.

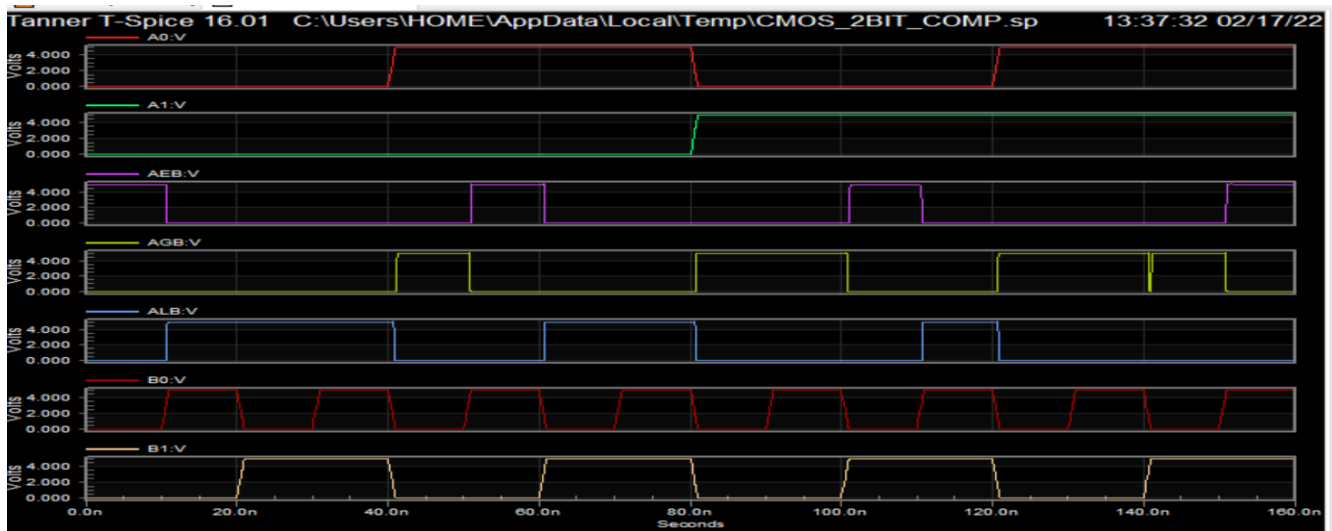


Figure4: Output waveforms for existing and proposed

5. CONCLUSION

The suggested GDI size comparator circuit execution with complete snake reasoning seemed astonishing execution surprisingly, with current conventional CMOS based frame. In the preceding section, we reviewed the near to execution of regular CMOS and presented GOI significant comparator with concession to regulate utilization at various levels of information voltage, temperature, and repeat. The more compact area of the proposed GDI degree comparator results in more restricted interconnects and, as a result, reduced crosstalk. Allow for more adept game planning and guiding. As a result, it is assumed that the suggested degree comparator using GDI technology requires less power and a smaller area than the CMOS significance comparator. As a result, this novel arrangement is an excellent choice for low-power capable system frames.

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