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SINGLE PHASE SIXTY THREE LEVEL INVERTER FOR HARMONICS MITIGATION USING ONLY NINE SWITCHES WITH SELF VOLTAGE BALANCING

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Abstract: The higher power quality compared to typical inverter circuits has created a demand for multi-level inverter topologies in industrial applications over the past few decades. It has grown in popularity as a result of lower harmonic distortion, better sine wave-like waveform quality, and lower switch voltage. Although the advantages of MLI outweigh the disadvantages In terms of power quality, researchers have been working to eliminate and mitigate the MLI problem by focusing on reducing the number of switches, reducing the number of sources, and managing voltage balancing. This article introduces a single-phase 63-level inverter for suppressing harmonics and power surges. It uses 9 switches with a reverse voltage configuration and uses H-bridge inverters with reduced power switches and power diodes to minimize switching losses. The proposed approach was simulated in MATLAB/SIMULINK, with improved waveforms with a low THD of 2.74%.

Index Terms - MLI, H-bridge inverter, PWM generator, MOSFET, PIC.

I. INTRODUCTION

Multi-level inverters (MLIs) are an advanced type of DC-AC converter. Multi-stage inverters are increasingly used in high-power industrial networks. Researchers have created many control algorithms and topologies to improve the performance of multi-level inverters [1]. For higher voltages, one switching device cannot be directly connected. The result is a multi-level inverter with a power semiconductor switch connected in series with a capacitor that isolates the DC connects voltage. The voltage across the capacitor is switched in such a way that it produces a stepped output signal that is closer to a sinusoidal shape in an electric drive system [2]. In recent years, MLI has received a lot of attention and is now frequently used in medium voltage and high voltage AC drives. Using semiconductor switch arrays with power and voltage specifications lower than their rated output and voltage, MLI synthesizes the output voltage at two or more levels [3]. MLI is suitable for use in uninterruptible power supplies (UPS), sun oriented Generators, organizations that work with high-voltage direct current (HVDC), and other DC-AC devices applications are all examples of DC-AC applications. Among them are many benefits presented by these converters, top notch yield voltage with limited consonant contortion and high productivity because of the low exchanging recurrence of the semiconductor device should be noted [4]. The ratio between the amplitudes of the DC input source determines the composition of the MLI. If the amplitudes are equal, the inverter is said to be symmetrical. On the off chance that the amplitudes are not equivalent, the inverter is supposed to be unbalanced [5] from the opposite side, this definition includes the relationship of a transformer to a cascaded topology based on a transformer supplied from a solitary DC source, like the geography under study. If all inverter stages have the same ratio, then the inverter configuration is symmetric. Otherwise, it is asymmetric [6]. Multilayer inverters are preferred over resonant circuits in applications that require AC voltages with approximate sinusoidal envelopes because MLI offers the advantages of lower power switch voltages, minimal total harmonic distortion, and fewer filtering components [7].

MLI has many advantages over two level inverters including quasisinusoidal output voltage, increased power and voltage capacity, least exchanging misfortunes and dv/dt, and diminished normal mode voltage. Then again, MLI has a few disservices, including countless power semiconductor switches, the need and complexity of multiple DC power supplies [8]. In terms of multilevel inverters, today`s challenges focus on improving inverter efficiency, power quality and inverter efficiency by reducing THD, conduction and switching losses. On the other hand, the switching loss is larger than the conduction misfortune and is relative to the quantity of exchanging states [9]. Inverter cost, number of parts, size and intricacy are connected with the quantity of switches and their sources. Learning the topology with fewer switches and sources is important and useful. To address the above deficiencies, a few reasonable choices have been devised and created. A nine-level structure based on switched logic

networks was proposed in [10] capacitors with fewer components was proposed. The MLI proposed in [11] is a topology optimized for 5 or more stages, and consists of two main multi-level converter units and a T-structured 3-stage inverter. [12] Presents the topology of a novel 3-phase 7-level inverter consisting of two 2-level flying capacitor inverters using H-bridge cells. [13] proposed a novel 5-level 3-phase MLR using a single source consisting of a 2-phase transformer and a Scott-T transformer. H-bridge cascade inverters fixed neutral inverters and floating capacitor inverters are on the whole normal multi-stage inverter geographies. The H-Bridge Cascade Inverter (CHB) is one of the most widely used inverters widely used inverters famous topologies in renewable energy systems. Each DC link requires several banks of electrolytic capacitors to assimilate the wave force of the H-span cells. Indeed, electrolytic Multilayer inverter modules' lifetime and dependability are reduced by capacitors. [14, 15].

Considering the above factors, a single-phase 63-level inverter is used. It can generate 63 levels of result voltage from a DC supply voltage. The proposed framework is efficient because it uses fewer switches and produces minimal total harmonic distortion at the output.

II. PROPOSED SYSTEM

The proposed 63-stage single-phase inverter consists of a conventional single-stage H-span inverter, nine switches and five voltage sources. The switching device used here is a MOSFET with high operating frequency and minimal switching loss compared to other transistors like BJT and IGBT. The square Figure 1 shows a diagram of the suggested framework.

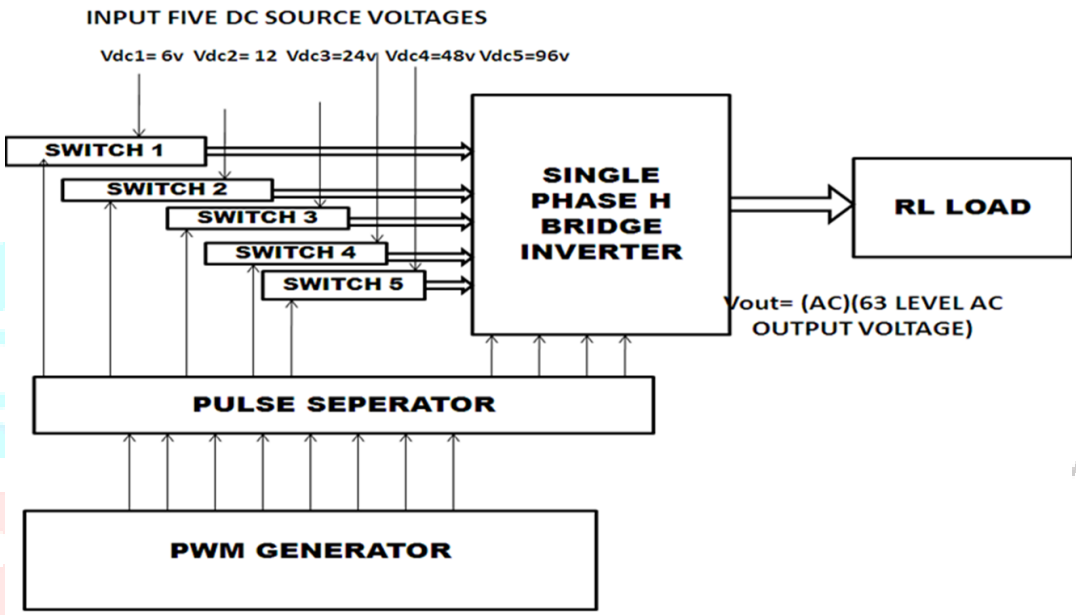

Figure 1 Proposed block diagram

A) H-BRIDGE INVERTER

This 63-level inverter has a cascaded full-bridge MOSFET inverter circuit. This H-bridge inverter circuit also has 5 switches connected to it. To protect the dv/dt and di/dt switching devices, all switches are connected to a snubber circuit (RC). When the switch is in the off position, the circuit is terminated with 5 diodes in parallel with the 5 switches.

B) LOAD:

The most extreme result power level of the inverter in this task is 40W. The most extreme result Voltage degree of the inverter is 240 volts. For this energy score we are able to make use of mild or little length engines. This venture carried out in a model. The five sources' voltage levels are interesting. So this method for arrangement is called as high stunned inverter. The level of the not entirely settled by the balance list and the applied DC voltage level of the inverter. The quantity of the voltage levels of the inverter can be changed to increase the inverter levels. The PIC (Personal Information Center) is a regulator is utilized to produce the PWM signal in the inverter circuit. This inverter uses a MOSFET switching element (IRF840). Because the hardware is designed as a prototype, the allowable power of the inverter is small.

C) PROPOSED SYSTEM OPERATION

The proposed single-stage 63-level inverter involves a 5-level inverter as displayed in Figure 2. This incorporates an ordinary single-stage span inverter, five switches and five voltage sources. For inverters with similar number of levels, this H-span configuration enjoys critical upper hands over elective geographies, for example, power decrease switches and power diodes. Legitimate exchanging of the inverter can generate 63 levels of output voltage.

((Vdc, 30Vdc/31, 29Vdc/31, 28Vdc/31, 27Vdc/31, 26Vdc/31, 25Vdc/31, 24Vdc/31, 23Vdc/31, 22Vdc/31, 21Vdc/31, 20Vdc/31, 19Vdc/31, 18Vdc/31, 17Vdc/31,16Vdc/15, 14Vdc/31, 13Vdc/31, 12Vdc/31, 11Vdc/31, 10Vdc/31, 9Vdc/31, 8Vdc/31, 7Vdc/31, 6Vdc/31, 5Vdc/31, 4Vdc/31, 3Vdc/31, 2Vdc/31, Vdc/31,0, -Vdc/31,- 2Vdc/31,- 3Vdc/31,- 4Vdc/31,- 5Vdc/31,- 6Vdc/31,- 7Vdc/31,- 8Vdc/31,-) 9Vdc/31,- 10Vdc/31,- 11Vdc/31,- 12Vdc/31,- 13Vdc/31,- 14Vdc/31, -15Vdc/31,- 16Vdc/31,- 17Vdc/31,- 18Vdc/31,- 19Vdc/31,- 20Vdc/31,- 21Vdc/31,- 22Vdc/31, -23Vdc/31,- 24Vdc/31,- 25Vdc/31,- 26Vdc/31,- 27Vdc/31,- 28Vdc/31,-29Vdc/31, - 30Vdc/31 –Vdc) from the dc supply voltage.

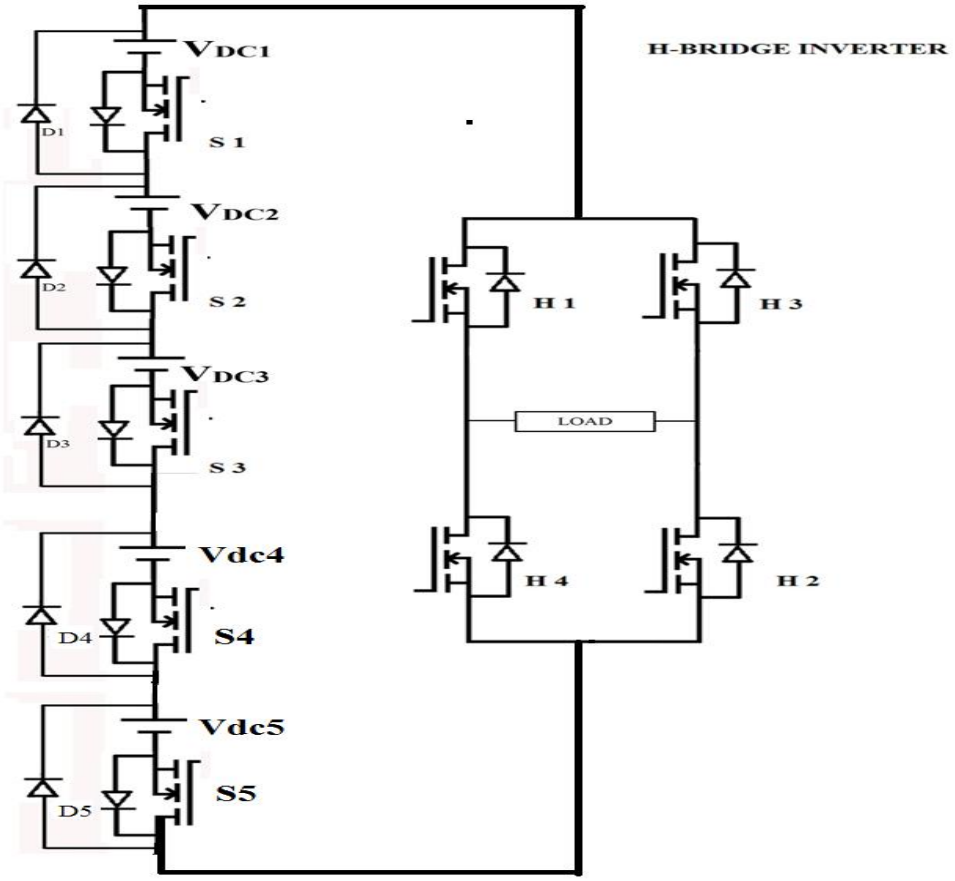

Figure 2 Circuit diagram of sixty three level inverter

- The suggested the operation of an inverter can be divided into 63 exchange states and the resulting 63 voltage levels were generated as follows.
- Negotiation Result 31/31 (31VDC/31): H1 turns on when the positive load terminal is connected when the information power heap terminal is linked to Vdc, H2 turns on. S1, S2, S3, S4, S5 are all turned on.
- Negotiation Result 30/31 (30VDC/31): H1 is turned on by combining the positive bottom terminal with DC voltage and H2 is turned on by the partner of the data dummy terminal. Switches the All of the switches S2, S3, S4, and S5 are switched on and the voltage provided to the storage terminals is 30 VDC. Current/31.
- 29/31 Positive Output (29VDC/31): H1 continues to connect Vdc to the positive weight terminal and H2 continues to communicate with the negative weight terminal of the information power supply. The voltage connected to the stack terminals is 29 volts, and switches S1, S3, S4, and S5 are on.VDC. Current/31.
- 28/31 positive output (28VDC/31): H1 connects the positive weight terminal to DC voltage and H2 connects the negative weight terminal of the information power supply. Switches S3, S4, S5 are switched depending on the voltage at the terminals of the store is 28Vdc. Current/31.
- 27/31 consistent result (27VDC/31): Because H1 is on, connect the positive lower terminal to Vdc, and because H2 is on, connect the positive upper terminal to Vdc. information power's store terminal. The switches S5, S4, S2, and S1 are all turned on. The stack terminals are exposed to a voltage of 27Vdc. Current/31.
- 26/31 predictable outcome (26VDC/31): H1 is ON, so the positive and unfavorable terminals are related with Vdc, and H2 is turned on, so the data power pile terminal is connected. All of the switches S2, S4, and S5 are on. The voltage is high applied to the stack terminals is 26Vdc. Current/31.
- 25/31 Positive Output (25VDC/31): H1 is turned on to link the data power supply's positive weight terminal to DC voltage, and H2 is turned on to connect the data power supply's negative weight terminal to DC voltage. The switches S1, S4, and S5 are all turned on. The pile terminals are subjected to a voltage of 25VDC/31.

- 24/31 Positive Output (24VDC/31): H1 is turned on, which connects the positive weight H2 is switched on, which links the data power supply's negative weight terminal to Vdc, and H1 is turned on, which connects the data power supply's positive weight terminal to Vdc S4,S5 is turned on. The load terminals have a voltage of 24 VDC supplied to them Current/31.
- 23/31 Positive Output (23VDC/31): Since Turn on H1, link the positive weight terminal to Vdc, and turn on H2 to connect the data power's negative weight terminal. The switches S5, S3, S2, and S1 are all turned on. The load terminal is connected to a voltage source 23V DC. Current/31.
- 22/31 Positive Output (22VDC/31): H1 continues to connect DC voltage and positive weight terminal; the negative weight terminal of the H2 is connected to the negative weight terminal of the data power supply by turning it on. Switches S5, S3, S2 are switched on the load's voltage is applied terminal is 22V DC. Current/31.
- 21/31 reliable outcome (21VDC/31): H1 is ON and the positive and unfavorable terminals are related with since H2 is turned on, the data power load terminal is at Vdc. is connected. The switches S5, S3, and S1 are all turned on. The stack terminals are subjected to a voltage of 21 VDC/m 31.
- Reliable Results 20/31 (20VDC/31): Turn on H1 and connect the lower positive pin to Vdc, turn on H2 to connect the data power stack pin. Switches S5, S3 is now active. The load's voltage is applied terminal is 20VDC. Current/31.
- Expected result 19/31 (19VDC/31): Since Connect the lower If H1 is on, connect the positive terminal to Vdc, and if H2 is on, connect the data power dummy terminal to Vdc. All of the switches are switched on: S5, S2, and S1. The terminal voltage is the voltage applied to the terminals of the magazine is 19VDC. Current/31.
- 18/31 Positive Output (18VDC/31): H1 continues to connect the positive weight H2 connects the data power supply's negative weight terminal to Vdc, and H1 connects the positive weight terminal to Vdc. S5 and S2 are both turned on. The load terminals are exposed to a voltage of 18V DC. Current/31.
- 17/31 positive output (17VDC/31): H1 continues to communicate with the positive weight terminal of Vdc and H2 connects with the negative weight terminal of the data power supply. Switches S5, S1 are on. The voltage applied to the pile terminal is 17VDC. Current/31.
- 16/31 positive output (16VDC/31): Turn H1 ON, connect positive weight terminal to Vdc, turn H2 ON, and connect to negative weight terminal of data power. Only the S5 Activates. The voltage applied to the terminals of the stack is 16VDC. Current/31.
- Reliable Results 15/31 (15VDC/31): Connect the bottom positive pin to DC voltage as H1 is on and the data power stack pin as H2 is on. The switches S1, S2, S3, and S4 are all turned on. The load terminals are exposed to a voltage of 15VDC/31.
- 14/31 Positive (14VDC/31): If H1 is on and interacts with the positive terminal of the file with Vdc and H2 is on, then the storage partner is the data terminal at the disadvantage. Switches S2, S3, and S4 are all turned on. The stack terminals are exposed to a voltage of 14VDC/31.
- 13/31 Positive Result (13Vdc/31): H1 turns on and connects the positive stack pin to Vdc and H2 turns on to interact with the opposite pin of the data supply load. S2, S3, and S4 have all been activated. A voltage of is applied to the stack terminals. The voltage applied to the terminals of the magazine is 13VDC. Current/31.
- 12/31 positive output (12VDC/31): H1 keeps connecting DC voltage and positive weight terminal and H2 keeps connecting negative weight terminal of data power supply. Both S2 and S4 are turned on.The file terminal is subjected to a voltage of 12VDC/31.
- Reliable Results 11/31 (11VDC/31): H1 is ON, positive and negative terminals are connected to Vdc, H2 is ON, so connect data power terminals. Switches S1, S2, and S4 are all turned on. The stack terminals are exposed to a voltage of 11VDC. Current/31.
- Match 10/31 (10VDC/31): Turn on H1 and connect the positive and negative terminals to Vdc, and turn on H2 to connect the storage terminals. Switches S4, S2 are switched on A 10Vdc voltage is applied to the magazine terminals. Current/31.
- 9/31 Positive outcome (9Vdc/31): H1 is turned on, interacting with the H2 is turned on, dealing with the stack hostile terminal of the pile positive terminal to Vdc information supply. The switches S4, S1 are both turned on. The load terminals are exposed to a voltage of 9Vdc/31.
- 8/31 Positive outcome (8Vdc/31): H1 is on, the load positive terminal is connected to Vdc, and H2 is off N, communicating the data supply stack unfavourable terminal. S4 is the only one who turned on. The voltage applied to the terminals of the magazine is 8VDC/31.
- Consistent result 7/31 (7Vdc/31): Connect the positive bottom When Connect the terminal to Vdc when H1 is on, and the storage terminal to the storage terminal when H2 is on data supply. S1, S2, and S3 are all turned on. The stack terminals are exposed to a voltage of 7VDC. Current/31.
- H1 turns on and interacts with the positive terminal of the pile with Vdc, and H2 turns on and interacts with the opposite terminal of the information feed stack. 6/31 Positive Result (6Vdc/31): H1 turns on and interacts with the positive

terminal of the pile with Vdc, and H2 turns on and interacts with the opposite terminal of the information feed stack. S2 and S3 are both turned on. 6VDC/31 is the voltage applied to the load terminals.

- H1 is active, connecting the load positive to Vdc, and H2 is active, suggesting a poor data supply stack output. H1 is on, connecting the load positive to Vdc, and H2 is on, indicating a poor output from the data supply stack. 5/31 Positive (5Vdc/31): H1 is on, connecting the load positive to Vdc, and H2 is on, indicating a bad output from the data supply stack. Both S1 and S3 are turned on. The voltage applied to the pile terminals is 5Vdc/31.
- H1 is ON, connecting the pile antagonistic terminal of the data supply to Vdc, and H2 is ON, connecting the store positive terminal to Vdc. 4/31 Positive result (4Vdc/31): H1 is ON; connecting the pile antagonistic terminal of the data supply to Vdc, and H2 is ON, connecting the store positive terminal to Vdc. The S3 switch is easily activated. 4Vdc/31 is the voltage applied to the store terminals.
- 3/31 Positive result (3Vdc/31): H1 is on, connecting the load antagonistic terminal of the information supply to Vdc, and H2 is on, connecting the stack positive terminal to Vdc. S1 and S2 are both turned on. The load terminal is connected to a 3Vdc supply. Current/31.
- 2/31 (2Vdc/31) Expected Result: Connect the positive and negative terminals to Vdc on H1, and the data power load terminals to Vdc on H2. S2 is turned on. 2VDC/31 is the voltage applied to the stack terminals.
- 1/31 consistent result (1Vdc/31): Turn on H1 and connect the positive and unfavourable terminals to Vdc, then turn on H2 to connect the information power pile terminals. S1 is the only one that turns on. 1VDC/31 is the applied voltage to the pile terminals.
- Zero outcomes: All switches S1, S2, S3, H1, H2, H3 and H4 are in the OFF position.

D) PWM GENERATOR

This project utilizes multi-transporter beat width adjustment innovation to create a 63-level result voltage. Seven similarly measured offset three-sided transporter signals are contrasted with a sinusoidal reference signal.

This PWM signal is applied to switches S1, S2, S3, and S4. It then, at that point, contrasts the three-sided transporter's two sinusoidal indications and the 180-degree offset sign to avoid hybrid difficulties between the two devices, these PWM beats feature a no man's land. These PWM pulses are received by the single-stage inverter circuit switches H1, H2, H3, and H4. A MOSFET is used in this trading setup. Minimal expense contrasted with IGBT. It utilizes a Peripheral Interface Controller (PIC) processor. It has a place with the classification of exceptionally huge scope incorporated frameworks. Many pins are multiplexed in the PIC. So it very well may be utilized as an information or result pin. DSPIC regulators are a lot quicker than advanced sign processors. This regulator is utilized to produce PWM beats for 63 inverter levels.

III. RESULTS AND DISCUSSION

The proposed method is put to the test in MATLAB/SIMULINK, with the results shown below.

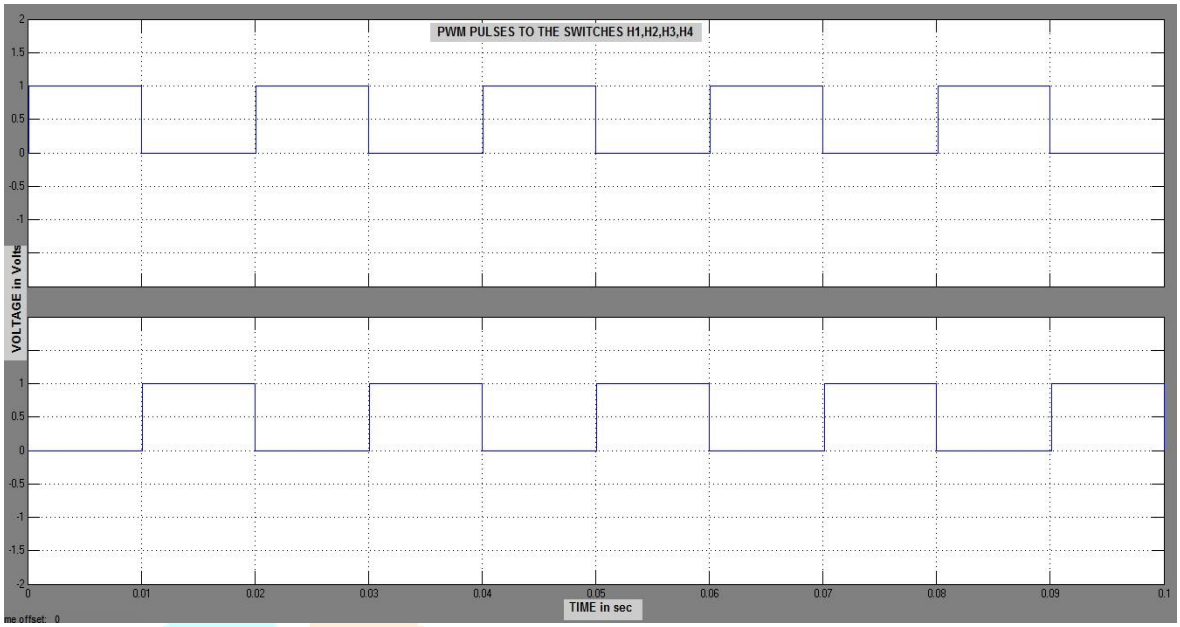

Figure 3 PWM pulses to H1, H2, H3, and H4

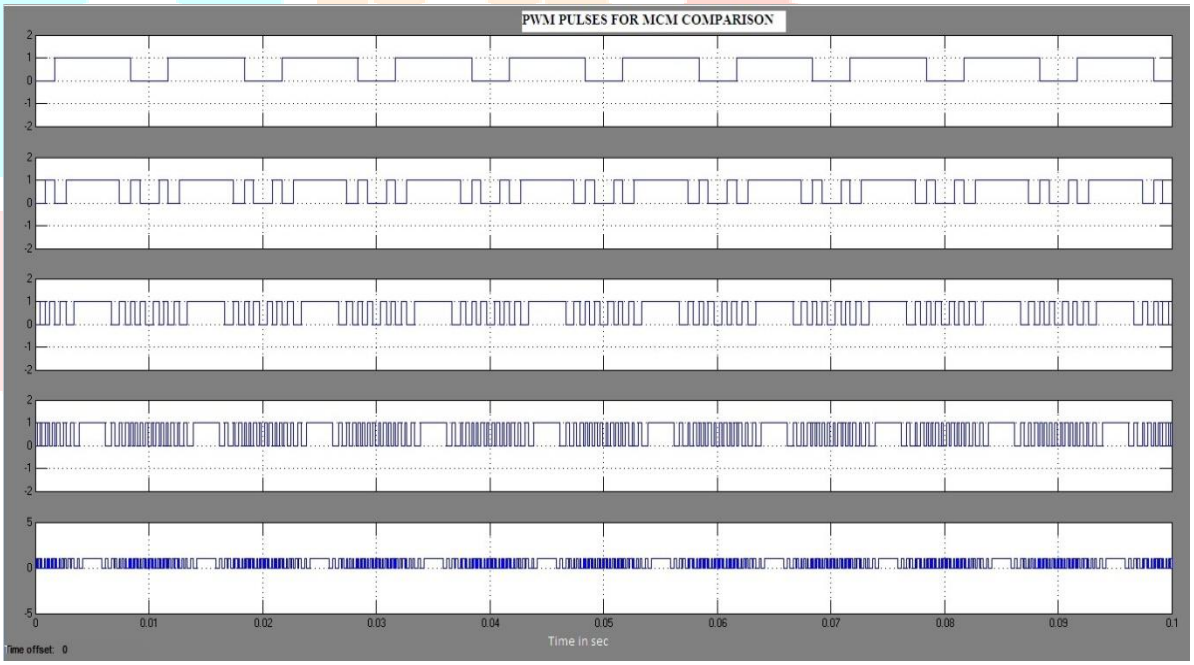

Fig.4 PWM pulses for 63 switches of a level inverter.

Figure 3 shows the PWM beats applied to the switches H1, H2, H3, H4, Figure 3 - PWM beats applied to the switches S1, S2, S3, S4, S5. This heartbeat has a changing recurrence of 5 kHz to control the assistant switch and is important to control the result voltage of the inverter.

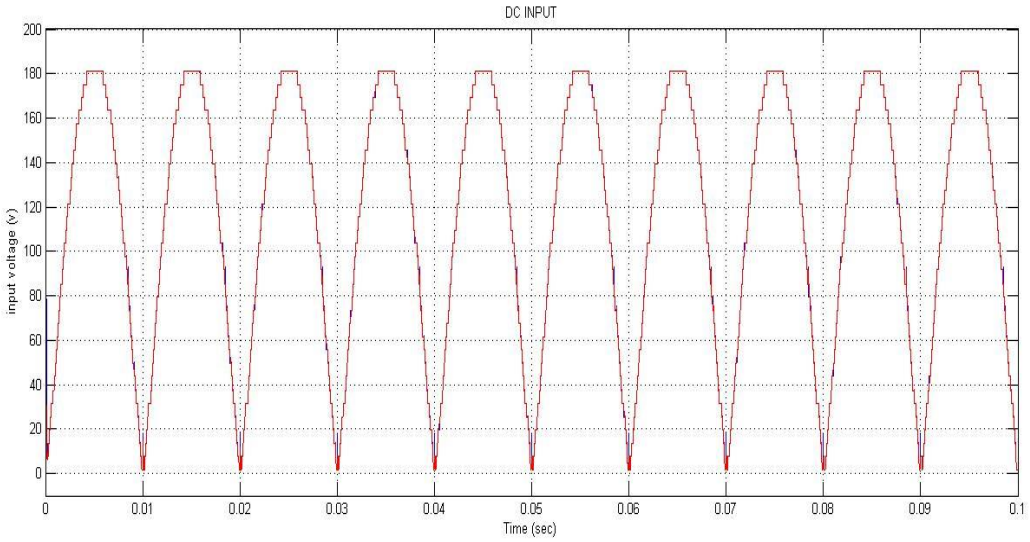

Figure 5 DC Output Voltage Waveform

Figure 5 shows the 63 output levels before switching to a single-phase inverter. This level of yield voltage is applied to the inverter to isolate the positive and negative result levels.

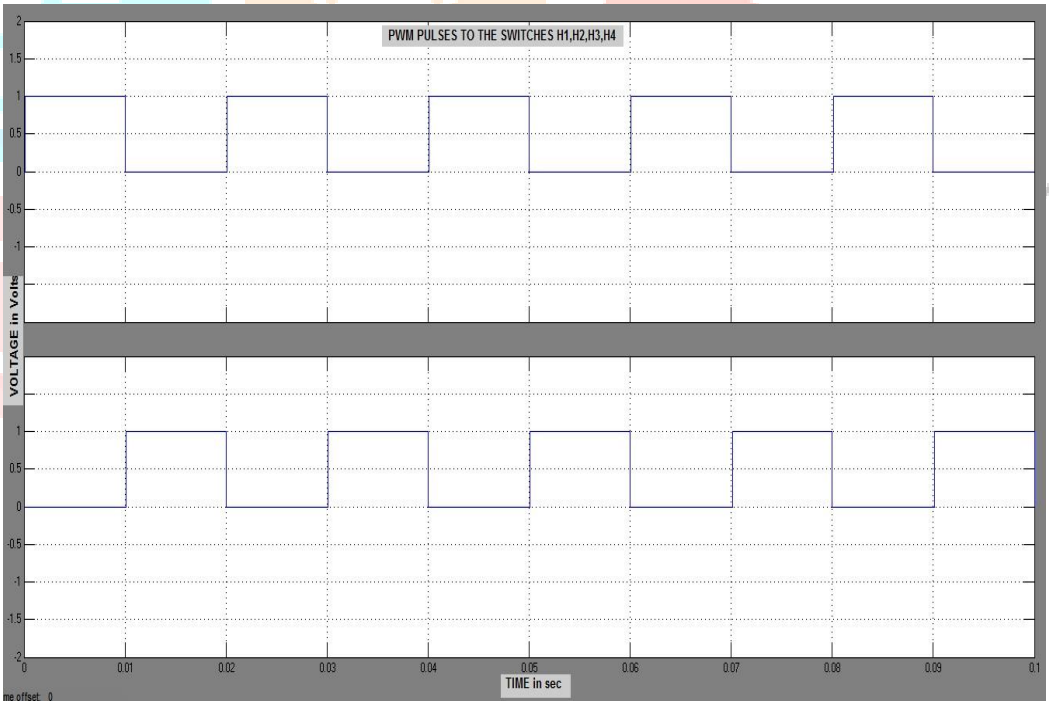

Figure 6 PWM Pulses for a H-Bridge Inverter

Figure 6 shows the PWM beats applied to a solitary stage inverter. It has a 180 degree balanced and the reference signal has a crucial recurrence of 50 Hz.

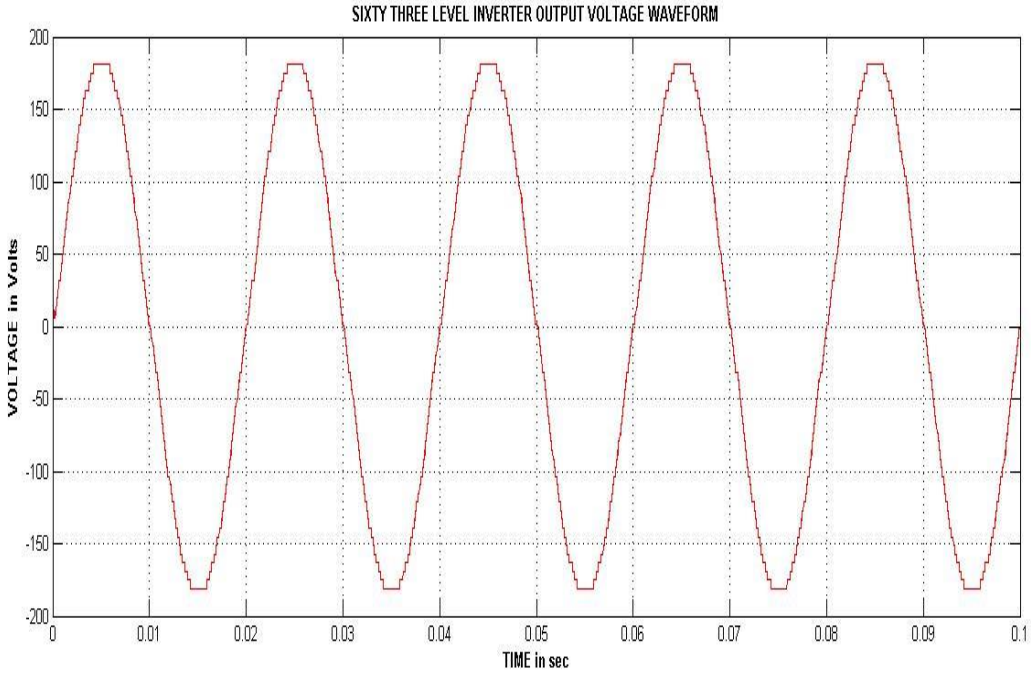

Figure 7 63 Output Voltage Levels of the Inverter

Figure 7 shows the result voltage levels of the proposed inverter geography. The result voltage is more like a sine wave, showing a lower THD. The result voltage is 183 volts and is result to the heap.

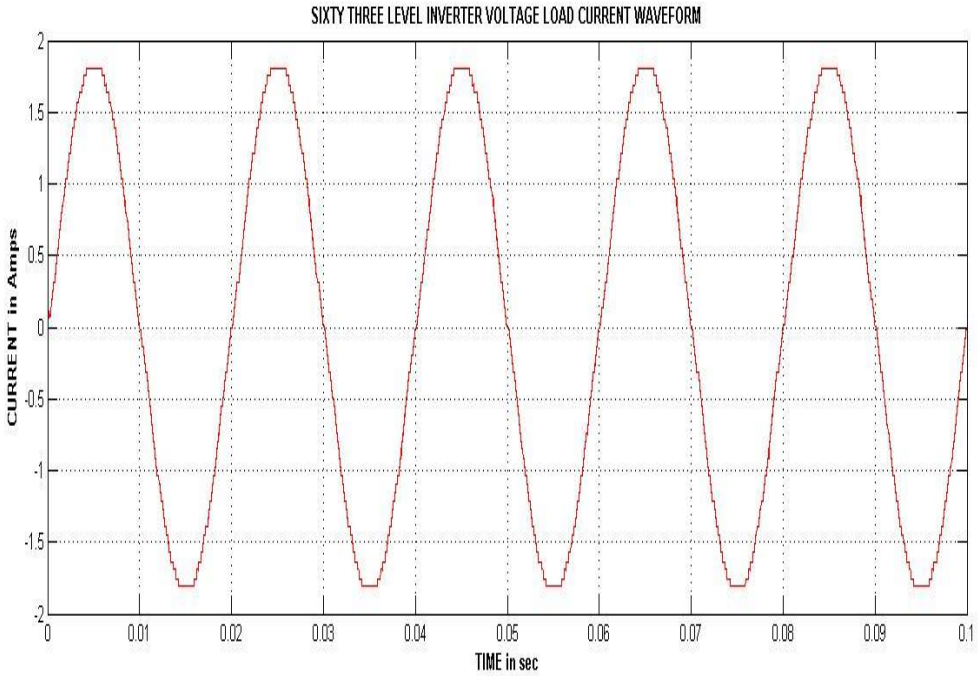

Figure 8 63 Levels of Inverter Output Current

Figure 8 shows 63 levels of voltage output current. Here the resistive load is 100 ohms and the load current is 1.83A.

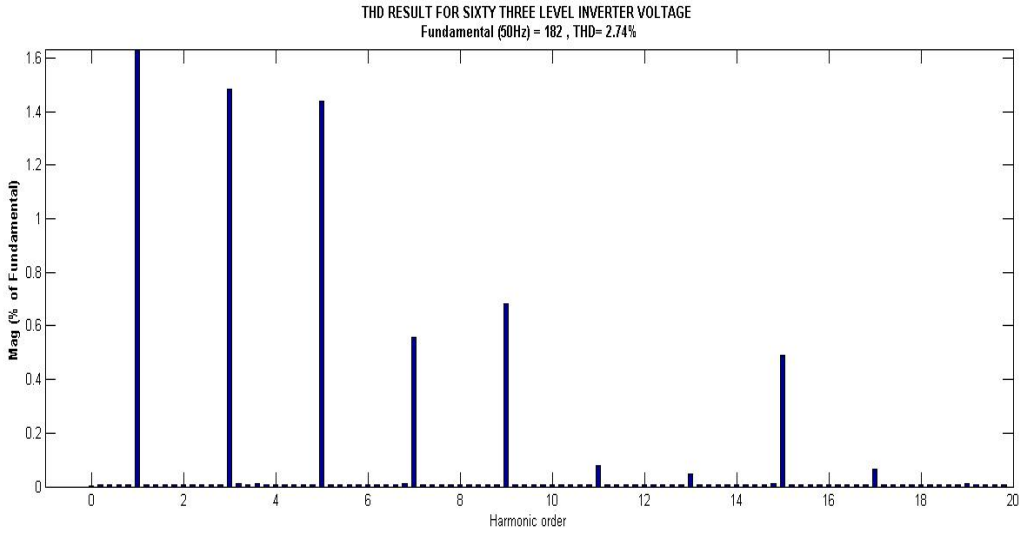

Figure 9 Sixty Three Level THD Inverter

Figure 9 shows the THD results of a proposed 63-level inverter with resistive load. Here the THD result is only 2.74% consistent with the IEEE harmonics standard.

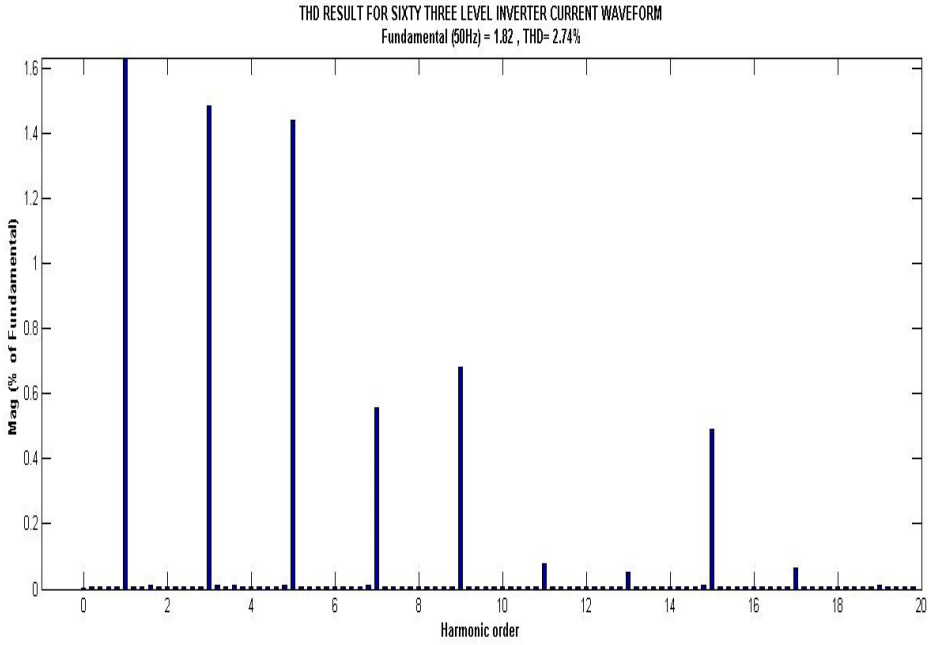

Figure 10 THD 63 Level Inverter Current

Figure 10 shows the THD aftereffect of resistive burden for the proposed 63 level inverter current bend shape. Here the THD result is just 2.74%. Agrees with IEEE consonant principles.

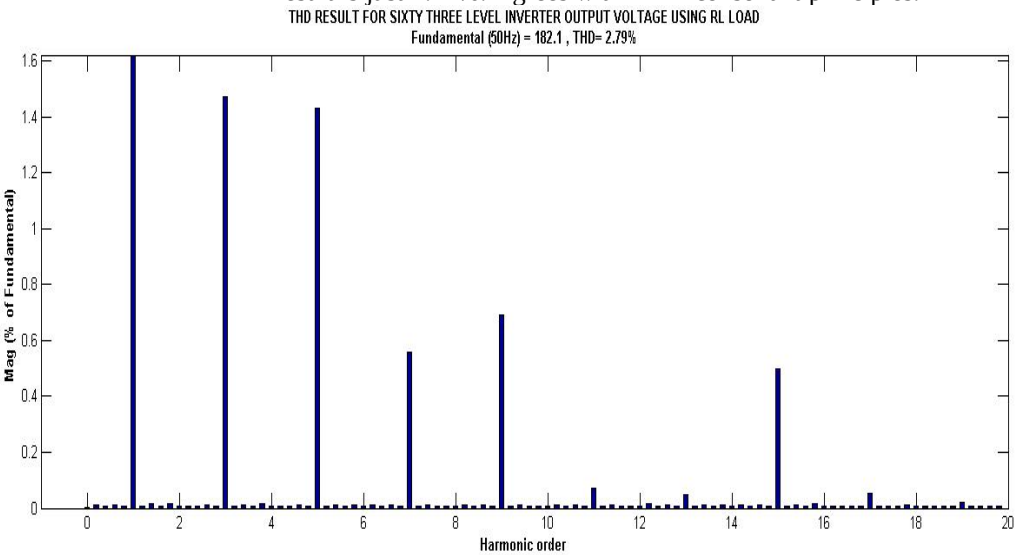

Figure 11 THD of a 63 Level Voltage Inverter with a RL

Load Figure 11 shows the THD consequences of a proposed 63 level voltage inverter waveform with a resistive inductive burden. Here the THD result is just 2.79% steady with the IEEE sounds standard.

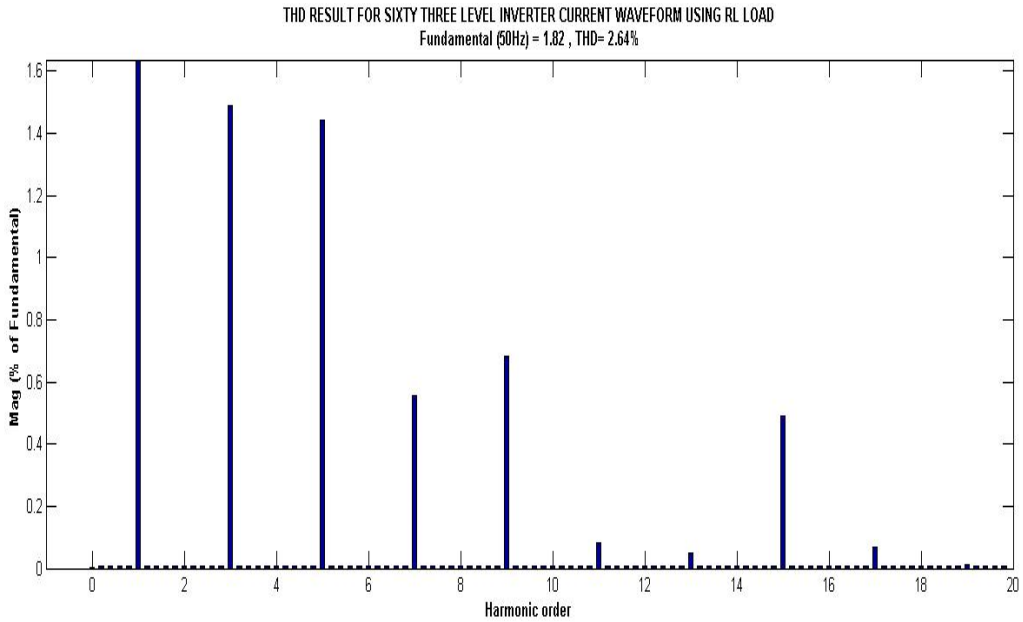

Figure 12 THD of 63 Current Levels of Inverter with RL

Load Figure 12 shows the THD consequences of the proposed 63 level current waveform of inverter with resistive inductive burden. Here the THD result is just 2.54% and follows the IEEE consonant norm.

IV. CONCLUSION

A simplified and fee powerful unmarried segment sixty 3 stage inverter has been proposed on this technique making use of fewer additives producing minimized voltage strain and harmonic distortion. Five one of a kind voltage stages are exploited and for this reason the configuration is called as uneven cascaded inverter. The sixty-3 stages of output voltage are finished with the aid of using manipulating the modulation index, and various DC voltage stages. The simulations are finished in MATLAB/SIMULINK are the acquired outcomes indicated decreased harmonics with minimized THD of 2.74% finally pleasant IEEE standards.

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