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# Implementation of Radiation-Hardened 14T SRAM 8 Bit Cell with Optimized speed for 45nm CMOS Technology

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***Abstract:*** Due to charge sharing across OFF-transistors, the use of a 14T SRAM bit cell for radiation hardening enhanced pliability to in a 65-nm CMOS technology, single-event upsets (SEUs) and single-event–multiple-node upsets (SEMNUs) were seen. The proposed RSP-14T design uses an 8-bit SRAM cell, which performs better per bit than the present RSP-14T architecture. In this system, the data is stored using CMOS transistors. When a heavy ion event occurs on a semiconductor material in a radiation environment, the particles become ionized. The device's sensitive nodes will collect these additional charges.

As a result, at certain nodes, a voltage perturbation will arise. The data stored in the SRAM bit cell may be swapped over when the amplitude of the voltage perturbation is big enough and above the inverter's logic threshold level. This 14T SRAM design idea will provide a superior outcome in terms of power, area, and latency than the current system. Finally, the suggested design was realized in the TANNER EDA at 45nm CMOS Technology with 0.9V input voltage, and the comparison was shown in terms of area power and latency.

***Index Terms* – SRAM, SEU, SEMNUs.**

## I. INTRODUCTION

Excessive radiation exposure is well known to inflict substantial injury to live animals, but high radiation levels may also injure non-living objects, notably electronics. Ionizing radiation, which includes both direct and indirect ionizing radiation, affects semiconductors, which are the backbone of all modern electronics. Direct ionizing radiation (DIAR) is a type of ionizing radiation that contains alpha and beta particles. Gamma rays and neutron radiation are examples of indirect ionizing radiation. Radiation impact causes irreversible harm to any devices that are consistently exposed to radiation.

Radiation hardened techniques are: Physical & Logical

One charged particle can cause irreversible physical injury in the form of radiation by interfering with thousands of electrons, causing damage to digital circuitry, signal noise, and irreversible physical harm in the form of radiation.

Electronics, of course, make the world go round, and without them, spacecraft, nuclear defense systems, satellites, military aircraft, and nuclear power plants would not function. These systems must be developed with long-lasting, nuclear-hardened electronics that can survive high amounts of radiation for long periods of time without failing. In this instance, radiation-hardened electronics can help. Manufacturers of radiation-hardened electronics perform testing as part of their product development procedures to ensure that these components are appropriately hardened. Incorporating radiation-tolerant electronics and components that can survive higher doses of ionizing radiation, such as cosmic outer space radiation, X-ray radiation used in medical or security contexts, and high-energy radiation utilized in nuclear power plants, is also part of radiation hardening. These components are referred to as radiation-hardened components since they do not need to be changed. Because high-energy radiation may disrupt atomic structures, it can have a range of effects on materials. When manufacturing components with higher radiation tolerance, manufacturers must evaluate the potential effects of radiation (to be tolerant of situations with high radiation levels, for example, in nuclear reactors or when exposed to ionizing radiation).

### About Memories:

Memory works similarly to the human brain in that it stores information. Memory is broken down into a large number of smaller portions known as cells. Each cell has a unique address, with the address range beginning at zero and ending with a size smaller than one.

For example, 64k memory contains 0 to 65535 locations or cells. Memory primarily divided into two types: Internal Memory & External Memory

Cache memory and primary/main memory are both found in internal memory External memory contains magnetic disk or optical disk.

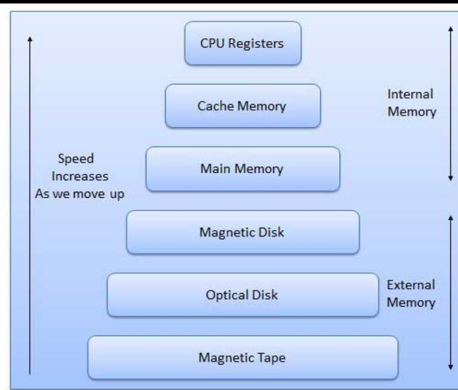


Figure 1: Memory Hierarchy

Memory can be divided into following types:

- Primary Memory
- Secondary Memory
- Cache memory

Primary memory is also divided into the following categories:

- RAM
- ROM

RAM further divided into SRAM and DRAM.

PROM, EPROM, EEPROM, OTP ROM, and FLASH MEMORY are all types of ROM.

Secondary memory contains following:

- HDD
- SSD
- COMPACT DISK
- FLOPPY DISK
- MAGENTIC TAPE/DISK

## II. Existing System:

SEU form of software-error and non-destructive single-event effect (SEEs). Within the environment of radiation, collisions of heavy/large ion with a semiconductor material, causes the particles in the circuit get ionized. The device's sensitive nodes will collect these additional charges. As a result, voltage disturbances will appear at particular nodes. The data stored in the SRAM bit cell may be switched over when the amplitude of the voltage perturbation is big enough and over the inverter's logic threshold level, resulting in a SEU, as shown in Fig. 4.

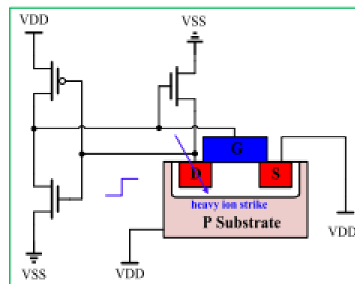


**Figure2: SRAM Memory with induced SEU**

As CMOS technology improves, the minimum spacing between transistors gets smaller. As a consequence, unlike previous procedures in which only one transistor was damaged, the charge deposited by a single particle assault affects a large number of transistors. Charge sharing causes single-event–multiple-node upsets (SEMNUs) in advancing nanometer CMOS technology, which is becoming the primary impact of particle assaults.

Furthermore, reducing the supply voltage makes circuits more vulnerable to radiation. As a result, the design of minimized radiation digital circuit technology is crucial. Because of its minimized node capacitance and maximum sensitivity volume per bit, SRAM is more robust to mild errors than its dynamic counterpart. As a result, the soft error ratio (SER) grows as technology goes down to the nanoscale level. To reduce the soft error rate, many alternatives to the standard 6T SRAM cell have been proposed. The most effective technique to provide circuit-level safety is to develop a unique architecture of transistor connections inside cells.

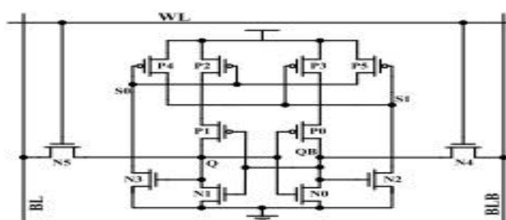


Figure 3: RHD-12T bit cell.

In addition to accepting a SEU on any of its internal single nodes, it can provide SEMNUs with some immunity. Unfortunately, because to the high power consumption and slow writing speed, it cannot be used. In addition to circuit strengthening, particular designing methodologies have been proposed as a supplementary strategy for increasing radiation tolerance. The LEAP-DICE sequential element was created using a unique layout method called as layout design through error-aware transistor placement (LEAP), according to the research. Raising the energy linear transfer upset threshold is effective, according to TCAD simulations.

To evaluate charge sharing, researchers used a Monte Carlo simulation platform called tool suite for radiation reliability assessment (TIARA). Based on the results of the TIARA simulations, the layout optimization of the most sensitive transistor pairs will be addressed.

Disadvantages:

- During the writing process, the feedback system will be readily disrupted.
- The charge transfer will be affected.

## III. Proposed System:

Due to charge transfer across powered off components, radiation hardening employing 14T SRAM 1 bit in a 65-nm CMOS technology enhanced pliability to single-event upset (SEU) as well as single-event–multiple-node upsets (SEMNUs). This suggested RSP-14T 8 bit design has a superior performance over the present RSP-14T 1 bit architecture. The data is stored using CMOS transistors in this suggested system. When a big ion strikes a semiconductor material in a radiation environment, the particles on the conductor get ionised. These extra charges will be gathered by the device's sensitive nodes.As a result, at certain nodes, a voltage perturbation will arise. When the amplitude of the voltage perturbation is large enough and surpasses the inverter's logic threshold level, the data stored in the SRAM bit cell may be switched over.By using this concept of 14T SRAM design will give the better result of power, area and delay than the existing system. Finally, the suggested design is realised in the TANNER tool using 45nm CMOS technology, and area power and delay are compared.

Read and Write Operation:Figure 15 depicts a schematic of the planned RSP-14T. The access transistors N4 and N5, which are controlled by a word line (WL), govern the connection between the bit lines (BL and BLB) and the storage nodes (Q and QB). The QB and Q nodes S0 and S1 are redundant nodes. The logic values at nodes S1, and S0,Q, QB are “1”, “0”, “1”, and “0” respectively.

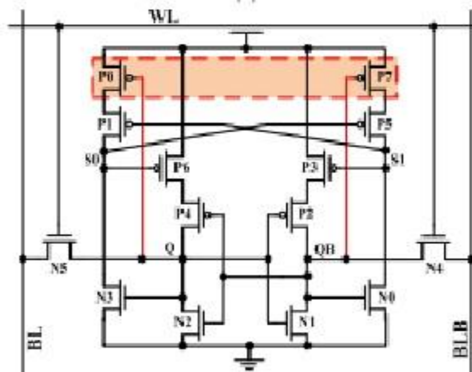


Figure 4: Proposed RSP-14T bit cell.

The functional study of this suggested RSP-14T is provided in a chronological order as: 1) write; 2) read; and 3) hold operation. In write operation, assume that QB = “0” and Q = “1” and the bit lines BLB and BL are set to “1” and “0” respectively. When the WL is activated, the value stored in QB and Q will be changed to “1” and “0” respectively. The updated state of that memory cell is then saved once WL is discharged to "0." The BLB and BL are pre-charged to "1" for read operation. The transistors N5 and N4 are switched on when the specified WL is enabled, and BLB is discharged through transistors N1 and N4. As a consequence, the BL and BLB differential voltages are formed and amplified by the sensing amplifier. WL is set to 0 in the hold operation, and the storage nodes are segregated from the BLs; thus, they maintain the initial state. Here, the transistors P7 and P0 are used to control the connection or cut-off between the power supply and transistors P5/P1, which is useful to improve the power consumption and write speed compared with RHD-12T.

According to the above-mentioned study and simulation findings, QB is the most vulnerable node (or Q, depending on whether the node contains "0"). As a result, strengthening it at the layout level is crucial. The vulnerable areas are the OFF-transistors' drains, as indicated in Fig. 5. When the drain of P2 (OFF-state) is activated, several holes will be poured into the n-well.

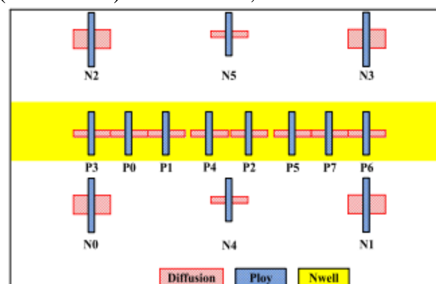


Figure 5: Transistor’s placement of the proposed RSP-14T.

because of the VDD's bipolar effect as a result, the hole collecting capacity of the drain will be increased. As a result, boosting SRAM SEU immunity requires minimizing the bipolar influence in the PMOS connecting the storage node. The recommended structure leverages the source isolation strategy to finish the node's strengthening, which has been demonstrated to be particularly effective in reducing p-hit SET.

On this assumption, the specialised design of stacking PMOS transistors is combined with layout-level optimization to further reduce the "0" to "1" upset (occurring on node QB). When the P2 drain is contacted, N2 and N0 are impacted, causing the SRAM cell to be disrupted, as seen in example 2.

The OFF-transistors N2 and N0 should be located far apart from the other OFF-PMOS transistors to avoid charge sharing. To prevent them from turning on at the same time, P3 and P2 should likewise be separated. The suggested RSP-14transistor T's position is shown in Fig.15 for layout-level optimization. With the above-mentioned circuit and layout-level optimization, the recommended RSP-14QB T's can be as powerful as possible. This deduction will be shown using the TCAD mixed-mode simulation.

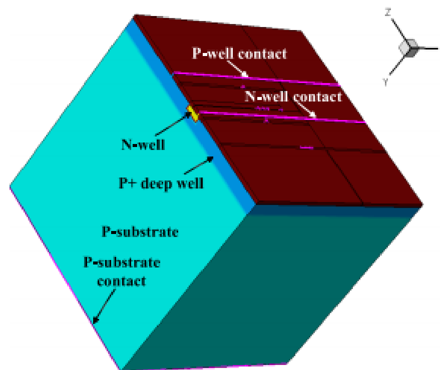


Figure 6: The projected RSP-14 T's TCAD model and top view.

Advantages:

- Reduces required input voltage.
- Delay decreases in terms of ns.
- Power consumption is less.
- Write speed is increases.

Disadvantages:

- MOSFET Count increases
- Area slightly increases
- During the writing process, the feedback system will be readily disrupted.
- The charge sharing between transistors will be neglected.

Applications:

- Used in Aero space sectors
- Used in Defense sectors
- Used in space applications

## IV. Results

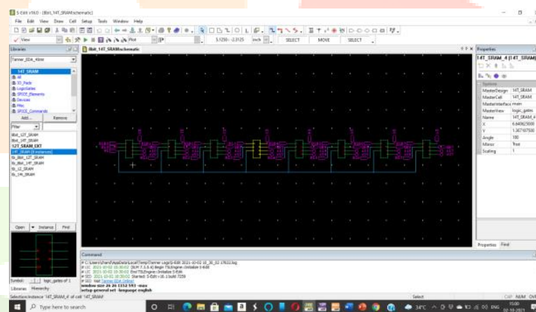

Fig 7: Proposed RSP-14T SRAM 8 bit

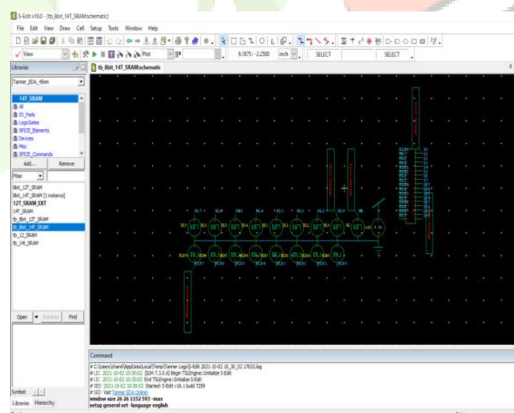

Fig 8 Test bench of Proposed RSP-14T SRAM 8 bit

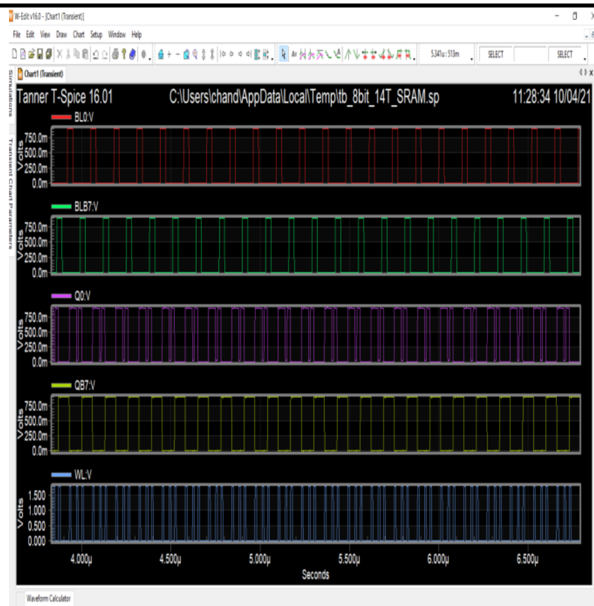


Fig 9: Proposed RSP-14T SRAM 8-bit 45nm

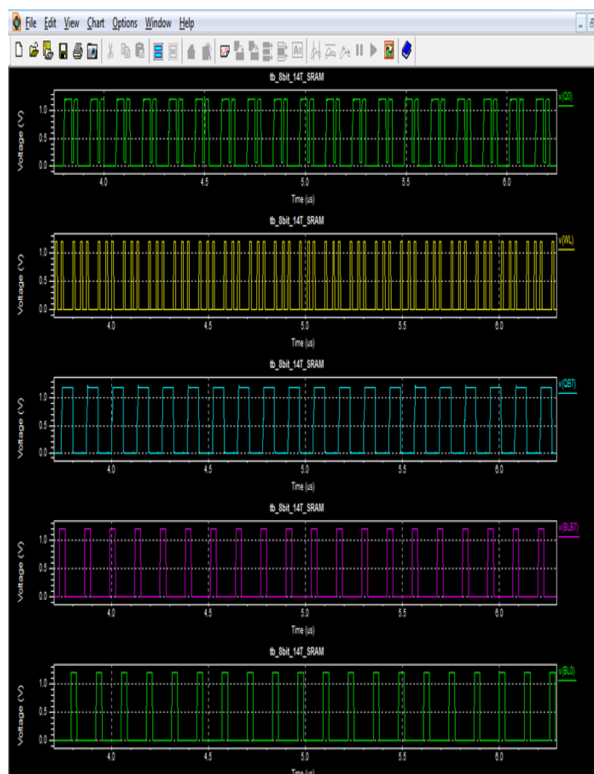


Fig 10: Proposed RSP-14T SRAM 8-bit 65nm

```
* BEGIN NON-GRAPHICAL DATA

Power Results
vvdd from time 0 to 1e-005
Average power consumed -> 3.650441e-005 watts
Max power 1.035707e-003 at time 9.65078e-006
Min power 8.042389e-011 at time 3.82e-007

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

DELAY = -1.0062e-007
   Trigger = 2.0062e-007
   Target  = 1.0000e-007

* END NON-GRAPHICAL DATA
*

* Parsing                    0.01 seconds
* Setup                      0.01 seconds
* DC operating point         0.00 seconds
* Transient Analysis         7.05 seconds
* Overhead                   1.41 seconds
* -----------------------------------------
* Total                      8.48 seconds

* Simulation completed  with  1 warning

* End of T-Spice output file
```

Fig 11: Power Result of Proposed RSP-14T SRAM 8-bit 45nm

```
* BEGIN NON-GRAPHICAL DATA

Power Results
vvdd from time 0 to 1e-005
Average power consumed -> 1.075512e-004 watts
Max power 1.417353e-003 at time 2.01e-007
Min power 1.167290e-010 at time 9.352e-006

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

DELAY = -3.3398e-008
   Trigger = 2.0100e-007
   Target  = 1.6760e-007

* END NON-GRAPHICAL DATA
*

* Parsing                   0.00 seconds
* Setup                     0.01 seconds
* DC operating point        0.00 seconds
* Transient Analysis        5.76 seconds
* Overhead                  1.24 seconds
* -----------------------------------------
* Total                     7.01 seconds

* Simulation completed  with  1 Warning

* End of T-Spice output file
```

Fig 12: Power Result of Proposed RSP-14T SRAM 8-bit 65nm

| | **RSP-14T SRAM (65nm)** | **RSP-14T SRAM (45nm)** | **RSP-14T SRAM for 8-bit cell (65nm)** | **RSP-14T SRAM for 8-bit cell (45nm)** |
|---|---|---|---|---|
| **Input Voltage (V)** | 1.2 | 0.9 | 1.2 | 0.9 |
| **MOSFET Count** | 14 | 14 | 112 | 112 |
| **Area (um)** | 0.910 | 0.630 | 7.280 | 5.040 |
| **Power (nW)** | 3647.07 | 1860.97 | 107551.2 | 36504.41 |
| **Delay(ns)** | 169.53 | 200 | 167.60 | **100** |

Table 1: Comparison

## IV. Conclusion

The source isolation approach is used to show the radiation-hardened 14T SRAM 8-bit cell with speed and power optimization (RSP-14T). Trigger delay is sufficient, which is higher than that recorded for RSP-14T, circuit and layout-level improvement. Meanwhile, its write speed is substantially faster than the RSP-14T 1 bit cell, but it consumes a lot of power. It takes up less room to implement, and the suggested RSP-14T 8-bit cell is more suited for space use. Even at a LET of 60 MeV-cm2/mg, which is greater than that of RHD-12T, the mixed-mode simulation findings demonstrate that it cannot only tolerate a SEU on any of its inner single nodes, but also has partial SEMNU immunity. It writes at a much quicker rate and consumes less power than the RHD12T. As a result, the projected RSP-14T cell's excepting area has increased somewhat, making it more suitable for space applications.

Single-event upsets (SEUs) and single-event–multiple-node upsets (SEMNUs) were seen in a 65-nm CMOS technology due to charge sharing between OFF-transistors and the adoption of a 14T SRAM bit cell for radiation hardening. The proposed RSP-14T architecture employs an 8-bit SRAM cell, which outperforms the current RSP-14T architecture per bit. The data is stored in this system utilising CMOS transistors. In terms of power, size, and latency, this 14T SRAM architecture concept will outperform the existing system. Finally, the proposed design was implemented in the TANNER EDA at 45nm CMOS Technology with 0.9V input voltage, and a comparison of area power and latency was shown.

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