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Two Stage CMOS Low Power Operational Amplifier with Cascoded Input and Cross-Coupled Output Stage

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Abstract— **This paper presents low power operational amplifier using cascoded input to get high input impedance, high bandwidth and high isolation amid input and the output stage. An operational amplifier with cross coupled output circuit provides same gain in both balanced as well as unbalanced conditions and also protects from having to drive a short. The amplifier is implemented with the proposed input,output stage and biasing circuits as core building blocks to give rail-to-rail output voltage range. The Operational amplifier is implemented in 0.25µm n- well CMOS process using 1-V power supply.**

Keywords— Bulk driven, low voltage design, cascode biasing, cross-coupled output stage amplifier.

I. INTRODUCTION

Reduced voltage supply, high input impedance, large bandwidth is the need of hours. The most effective way to reduce the power consumption is to reduce the voltage supply, although it is a challenging task for the analog designers [1]. The author compared different typologies suitable for low voltage supply and designed a device with standard 250 nm technology and highlighted the benefits and possible applications.

The operational trasconductance amplifier (OTA) is very much in demand and so become most common used block and thus a lot of work has been done on it. Therefore many circuit combinations are proposed by analog designers to full fill the requirements of DC gain, bandwidth and slew rate. Different architectures such as gate- driven amplifier, bulk-driven and self-cascode topology, hybrid-mode input stage and rail-to-rail amplifier with cross- coupled output stage was proposed by L. Zuo and S. K. Islam [2]. In this paper, a bulk driven amplifier input stage based on cascode configuration biasing with a cross coupled output stage, using the standard 250 nm CMOS technology is proposed.

Jasbir Kaur, Deepak Goel proposed a circuit using low threshold voltages for operation. To reduce supply voltages, low-voltage MOSTs, self-cascode MOSTs, floating-gate MOSTs (FG- MOST) using bulk-driven technique were implemented [3]. In this paper, abulk driven inverter is proposed and compared it with inverter using gate driven technique. D.K Shedge, et. al. compared different biasing techniques used in Op - Amps. The high resistance desirable for current mirrors was compared along with other parameters like transconductance etc. [4]. Rashmi Sharma et. al given comparative analysis of different types of current mirrors. In this paper, the DC analysis of simple, Wilson and cascode current mirror has been done and different parameters like power dissipation, threshold voltage, output impedance and transconductance have been compared[5].

Zhingang Quinet. al proposed a circuit where they used the cross coupled output stage and also simulated the circuit for common source amplifier and compared its working with a fully cross coupled output stage[6].

II. OVERVIEW OF TECHNIQUES USED IN PROPOSED CIRCUIT

- *Bulk-Driven Amplifier*

A bulk-driven amplifier proposed by J. Kaur and D. Goel, is a combination of an input differential pair, a current source,a common source stage and an active load. The gain of the bulk driven input stage is very low compared with gate driven input stage so the gain- bandwidth product is also low w.r.t the classical gate-driven amplifier. The gain of bulk driven is given by bulk transconductance (gmb) multiplied by the output resistance which is much lower than the gate transconductance (gm). In the bulk-driven Op Amp, the input signal is applied at the bulk of the differential pair and source, drain and gate provide the bias of the transistors. This technique has applications in biomedical, where the output of sensors is ultra low voltage. Moreover, the input stage of bulk-driven exhibits a better common mode input range compared to the gate-driven topology.

- *Cascode Current Mirror for biasing input stage*

One of the most desirable characteristics of current mirror is its high input resistance which keeps the output current constant regardless of load conditions which is achieved by cascode biasing [7]. The common application of current mirror is as biasing element, active loads and current amplifiers. Gain of cascode bulk driven operational amplifier can be increased further by employing common source as second stage. The cascode stage has high input impedance, higher output impedance, high bandwidth and higher gain.

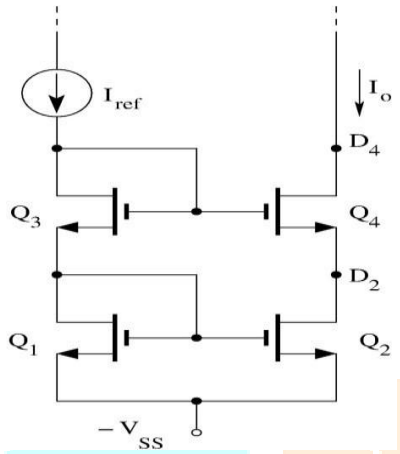


Fig. 1: Cascode current mirror

- Amplifier with Cross-Coupled Output Stage

Operational amplifier employing complementary input stage and a novel cross-coupled output stage is best suited for ultra-low-power and rail-to-rail operation. In this two-stage architecture, the cross-coupled output stage increases the transconductance of the output stage without occupying additional chip area. Hence, overall gain of the amplifier increased and drivability for a capacitive load also.

III. PROPOSED METHODOLOGY

The proposed two stage operational amplifier consists of bulk driven amplifier at input stage with cascode biasing at a cross coupled output stage. The main focus is on the operation of devices at lower threshold voltage for which the bulk driven amplifier is used. Further a cascode current mirror is used to counter the effect of bulk driven mosfets by improving the transconductance of input stage. Lastly the cross coupled output stage is added to enhance the gain and UGBW.

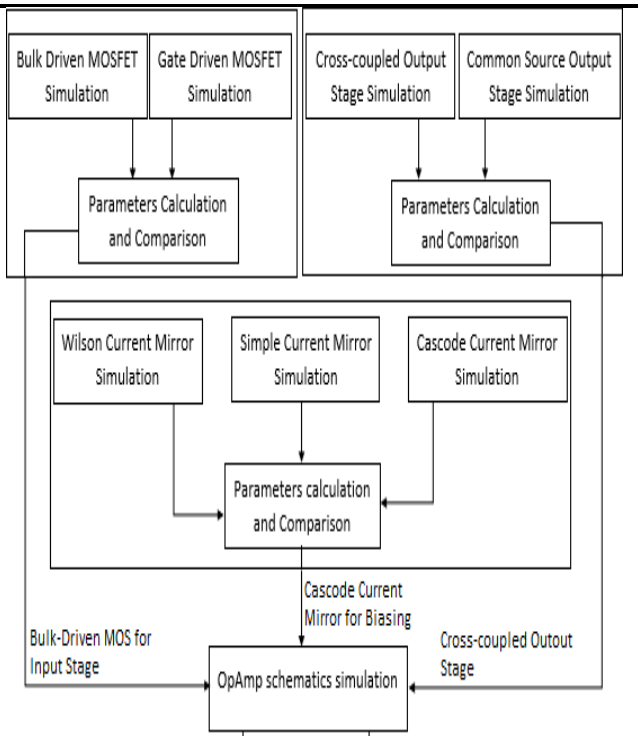


Fig 2: Block diagram for proposed methodology

A bulk- driven MOSFET has been used to reduce the threshold voltage. The reverse bias voltage on the well-source junction will cause to increase the threshold voltage. Similarly, a forward bias on well- source junction decreases the threshold voltage. The bulk-driven transistor technique is a better solution to reduce the limitation of threshold voltage. Because the bulk- driven transistor works like a depletion type device, it can operate under zero, negative or even slightly positive biasing condition.

$$Vt = Vto + \gamma \left(\sqrt{(2|\phi F| + VSB)} - \sqrt{2|\phi F|} \right)$$

Where, Vto is the threshold voltage at zero bulk source voltage, ϕF is the Fermi potential, γ is the body effect coefficient.

Fig. 3(b) shows cross-coupled output stage. Essentially, the PMOS transistor MP3 in Fig. 3(a) is divided in half and shown in Fig. 3(b) as MP3a and MP3b. Both MP3a and MP3b comprise five unit transistors in parallel. Similarly, NMOS transistor MN3 in Fig. 3(a) is also divided in half, as shown in Fig. 3(b) as MN3a and MN3b. Both MN3a and MN3b comprise five unit transistors in parallel.

The cross-coupled output stage shown in Fig. 3(b) is the most useful because it increases the transconductance of MOSFETs of the output stage and enhances the gain of the op-amp.

Fig.4 shows the schematic capture of the proposed two stage Operational Amplifier. It consists of twelve MOSFETS transistors and the two resistive elements. It has three stages of operation.

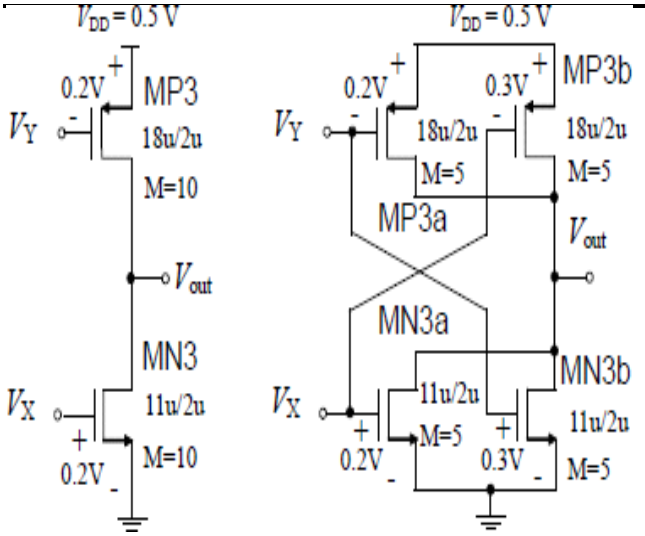


Fig 3(a): Common source output stage (b): Cross coupled output stage

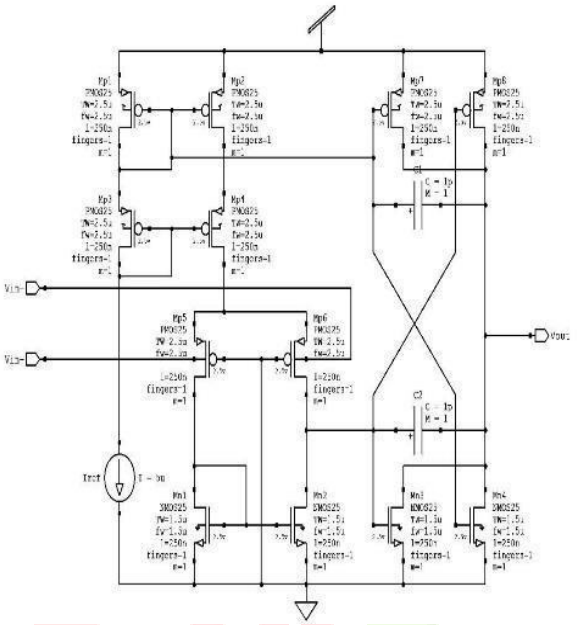
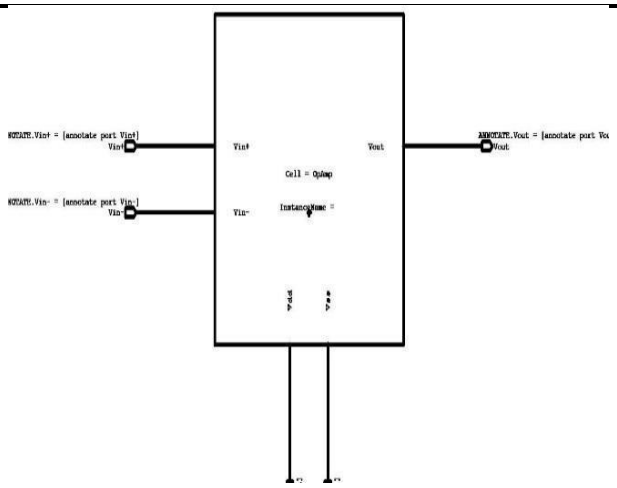


Fig 5: Schematic capture of proposed Op Amp

Initially a differential amplifier making use of bulk driven MOSFETs Mp5, Mp6 and Mn1 and Mn2. The MOSFETs Mp5 and Mp6 are given Vin- and Vin+ respectively at its body terminal, while the configuration of Mn1 and Mn2 has its bulk terminal grounded. The differential amplifier at input stage is bias with the help of Cascode current mirror. The current mirror has four p-type MOSFETs Mp1, Mp2, Mp3 and Mp4. The current IREF is the input supply of the current mirror which mirrors the same current at its output which is connected to source terminal of p-type MOSFETs of differential amplifier. The output of first stage is fed into the cross-coupling output stage. In this stage the coupling capacitance C1 and C2 of 1pf is present. The stage consists of four transistors Mp7, Mp8 and Mn3, Mn4 performing cross coupling action, two of which also acts as inverter. The voltage supply used is of 1V. The differential stage with bulk driven mosfet is given the supply of +Vin and -Vin to the bulk or body of the differential amplifier.



IV. SIMULATION RESULTS

Before moving to the results of proposed circuit, a DC sweep analysis is performed to show operation of bulk driven at lower threshold voltage in comparison to gate driven technique. The better transconductance of the cascode current mirror and its high input impedance is shown through AC analysis. The DC sweep analysis of the three types of current mirrors is done to show the mirroring capacity of current mirror in which cascode proved better. After the text edit has been completed, the paper is ready for the template. Duplicate the template file by using the Save As command, and use the naming convention prescribed by your conference for the name of your paper. In this newly created file, highlight all of the contents and import your prepared text file. You are now ready to style your paper; use the scroll down window on the left of the MS Word Formatting toolbar.

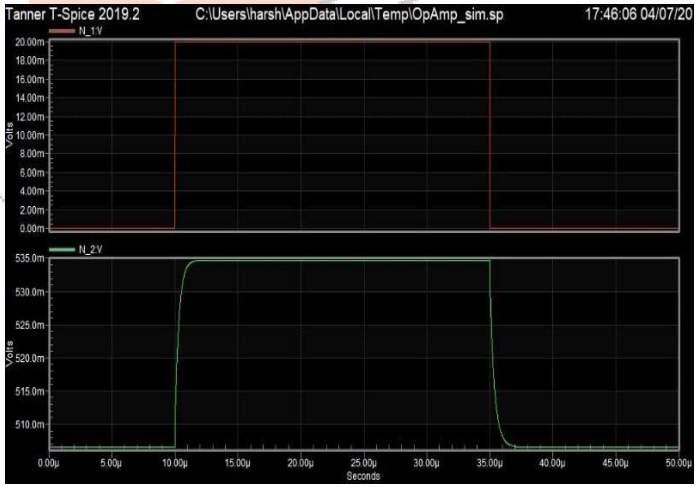


Fig 7: Simulation for SR and DC gain (ADC)

TSPICE simulation for the proposed circuit using parameters of standard 0.25µm CMOS process with a supply voltage of 1 Vis done and also the slew rate of the circuit is calculated from the transient analysis of the circuit. The transient analysis of the circuit is performed to calculate Slew Rate. A square wave input is given to the Op Amp. The SR of the Op Amp is 0.02V/µs.

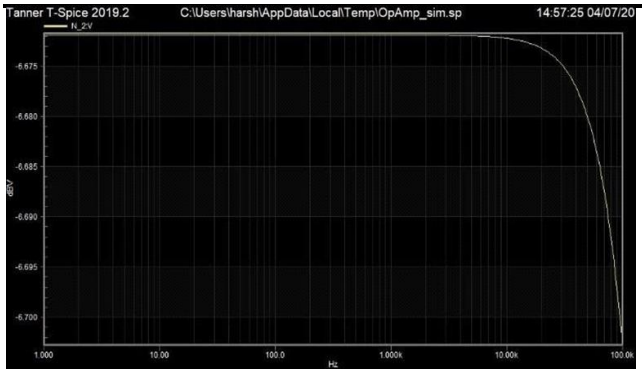


Fig 8: Simulation for ACM (Mag. of AC source is kept unity for ease of calculation)

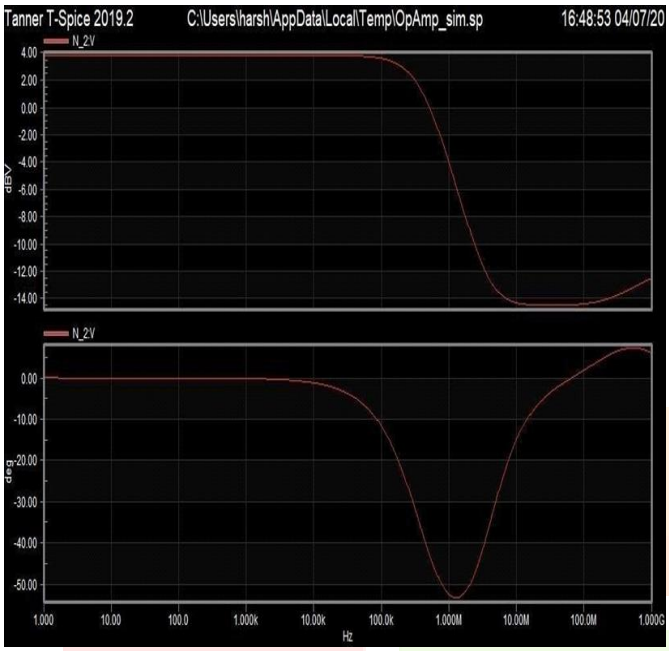
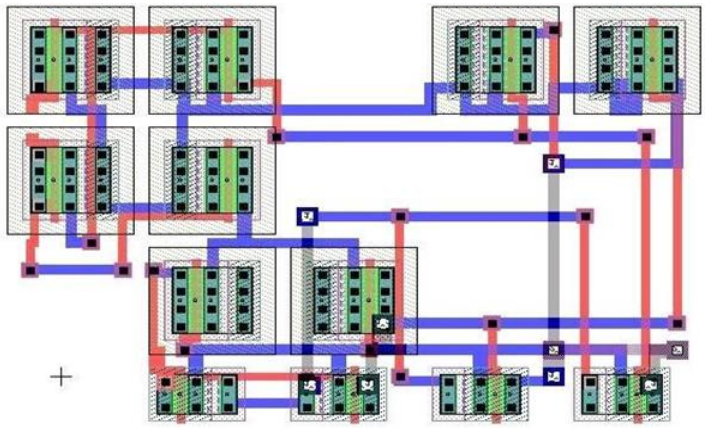


Fig 9: Simulation for UGBW and PM

Fig. 8 shows the open-loop frequency response at a common-mode input voltage of 0.5 V (half VDD). The AC analysis of the circuit is shown in fig. 9 to find out the common mode gain (Acm) and CMRR (CMRR=(ADC/ACM)). The DC gain of the proposed op-amp is 33 dB, the unity-gain frequency 520 kHz and the phase margin 137 degree. Layout design of Proposed Op Amp is shown in fig.10.



V. SIMULATION RESULTS

A two stage low power bulk driven op amp with cascoded input stage and cross coupled output stage is proposed. As the transconductance of structure is improved, the performance parameters of the Operational Amplifier such as D. C. gain, Unity Gain Bandwidth, open loop gain are all enhanced. The circuit has been implemented using 0.25µm standard CMOS process to achieve a low power Op Amp which could be effective at operation for low voltage applications. The DC gain of the proposed Op-Amp is 33 dB, the unity-gain frequency 520 kHz and the phase margin is 137 degrees. Slew Rate of 0.02V/µs and CMRR of 39 dB is achieved. The most important and the desirable result i.e the power consumption for the Op Amp is 19.7µw. Thus this result of power consumed makes our motive for low power applications achieved.

Table 1. Summary of Results As Compared to Previous Works

PARAMETERS	Proposed Work	Ref [2]	Ref [3]
SUPPLY	1V	0.5V	1V
TECHNOLOGY	0.25µm	0.18µm	0.35µm
GAIN	33dB	77dB	88dB
POWER (µw)	20	0.07	197
UNITY GAIN FREQUENCY	520KHZ	4KHZ	11670KHZ

REFERENCES

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