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DESIGN OF 10T SRAM MEMORY CELL

Mansi Jain*, Dr. R.S Gamad**, Mr. D.S Ajnar ***

*(Department of electronics and instrumentation, SGSITS , Indore (M.P))

** (Department of electronics and instrumentation, SGSITS , Indore (M.P))

***(Department of electronics and instrumentation, SGSITS , Indore (M.P))

ABSTRACT:

This paper examines and analyses a 10T SRAM (static random access memory) cell, as well as comparing it to a normal 6T SRAM. Because memories are integrated parts of digital circuits, the proposed design is used as a part of memory with single purpose devices that demand low power consumption and reliability. authors have reported simulation based result and improvement is obtained in the present result as compared to the earlier reported work.

Keywords - Delay, power, Read ability , Write ability, 10TSRAM

1. Introduction

Microelectronics are used in a wide range of gadgets in today's society. A review of new technology has been spurred as a result of the fast proliferation of electronic devices worldwide, with a special focus on memory. Memories are increasingly being used in biological, wireless, and implementable devices. Individual parts of memory are organised in modern VLSI systems. Semiconductor memories are an integral part of the VLSI architecture. There are two forms of RAM (random access memory): SRAM (static random-access memory) and DRAM (dynamic random-access memory)[2]. The dynamic word signifies that the charge of ideal storing capacitors must be refreshed on a regular basis, which is why DRAMs are rarely used. Many SRAM Cell designs have been proposed to improve stability and power consumption, but the conventional 6T cell still provides a good balance of size and performance because the conventional 6T cell has a very compact and simple structure, but its operation of voltage is minimal and limited by conflicting read and write stability requirements, so it is not used for ultra-low voltage operation. There are several proposed designs for memory cells to enhance speed and power, with one technique focusing on improving SNM low power (other memory configurations (7T, 8T, 9T) have their own advantages and disadvantages)[1]. Six MOSFETs make up a typical SRAM cell. Four transistors (PM0, PM1, NM0, and NM1) store one bit and form two cross-coupled inverters. There are two stable states, indicated by the numbers 0 and 1. The conventional 6T cell is simple, but it has poor stability at low voltage, therefore we strive to improve its read and write stability by using various approaches, such as dual rail power supply, negative bit line, single bit line with dynamic feedback management, and so on. However, for proper operation, the 6T SRAM's

power supply must be decreased below 0.6[2]

2. CONVENTIONAL 6T SRAM

A traditional 6T cell contains two consecutive CMOS inverters. The output of an inverter is connected to another inverter as an input. 6T SRAM cell operating process: During the write process, the BL (bitline) is loaded to "1" or lowered to "0", depending on how the data is stored, and the BLB (bitline bar) is BL (bitline bar). Bitline bar is complemented and loaded. Figure 1

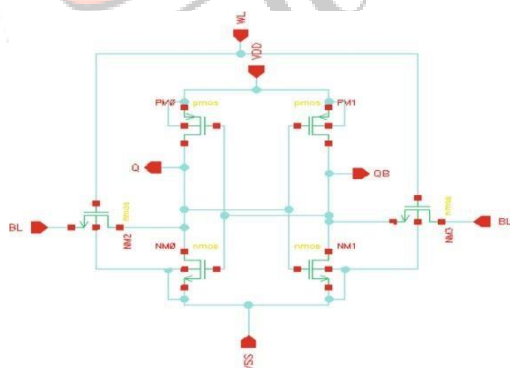


Fig. 1 conventional 6T SRAM Cell

To write '1', BL will be charged to VDD, BLB will be lowered to '0,' and WWL will be charged to VDD with value and complementing value being saved at terminal Q. For read operation, charge BL and BL B to VDD and WL to '1'. This creates a route from BL to ground via NM2 and NM3, indicating that a cell contains a '1' at the Q terminal and a positive value at the QB. This conventional 6T SRAM cell has a low read noise margin (RNM). To improve RNM, the width of the pull-down transistors (NM0 and NM1) must be increased. However, this increases the area of the SRAM, which increases leakage currents. As per

requirement of less power consumption during active condition of circuit require slow supply voltage, due to voltage scaling reliability of circuit is reduced [2,3]. At lower voltages, SRAM reliability is more dubious. The minimal supply voltage for read and write stability in an SRAM is $V_{DD\ min}$. As a result, read/write stability analysis is critical for lowpower SRAMs [3, 4].

3. Proposed design of 10T SRAM Cell

Figure 2 shows a schematic of the 10T SRAM Cell presented in this study, which contains 10T transistors in which PM1, PM2, NM3, NM4 form

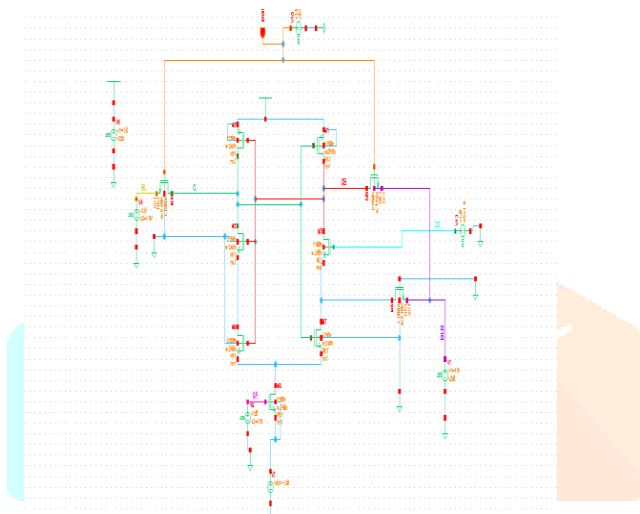


Fig 2. Proposed 10 T SRAM Cell

cross-coupled inverters and operate as a storage cell, with PM1, PM2 acting as pull-up transistors and NM3, N4 acting as pull down transistors. The BL includes data that we want to write, and for '1' it will be charged to V_{DD} , while for '0' it will be decreased to '0,' with BLB acting as a complement. The NM1 transistor is cascaded with the NM3 and NM8 transistors in the ground path, resulting in a cascading effect that reduces power consumption. The NM2 transistor is utilised for the control signal during read operations, and it offers isolation between the V_{DD} and ground paths, allowing for interrupt-free reading and a good RNM (read noise margin). Transistor NM7 offers an access path for read operation, while NM8 provides a sleep transistor and stacking effect during hold operation, resulting in a low leakage current and lower power consumption for the proposed cell design [5, 6].

4. Operation of proposed 10T SRAM

Proposed design can be operated in two mode that is Write operation and read operation.

4.1 write operation

Figure 2 shows the situation. When we write a '0' in the proposed SRAM Cell, WWL is kept high to get

an access transistor to provide a connection between the bit line and the cell, RWL makes a '0' because it is a write operation, CS is kept high to provide a path from the access transistor to ground, and GP is kept to provide a grounding path. Because of the write '0' operation, BL is kept low or connected to the ground channel, while BLB is made high as a complement to BL. When BL is set to '0' and WWL is set to high, NM5, NM6, and NM7 will be in conducting mode, while NM7 will be in the 'off' state. As a result, the logic is written through the path QB, NM6, BLB, where QB reaches 90% of V_{DD} and Q becomes 10% of V_{DD} through the path BL, NM5, Q. Similarly, with the write '1' action (shown in Fig. 2), WWL and BL will remain high due to the write '1' operation, and BLB is just a complement of BL. The logic 1 is stored at node Q through the BLNM5Q channel for write '1' operations, and write time is monitored when 'Q' hits 90% of V_{DD} and signal WWL is high.

4.2 Read Operation

In read operation both BLB and BL are precharged to V_{DD} before the read operation. Because read operation, RWL (read word line) is kept high, CS (control signal) is kept low, and GP (ground path) is kept high to provide a grounding channel, WWL (write word line) will be '0' for read operation, as illustrated in Fig. For read '1' ($Q = 1$), logic 1 is stored at node Q, which turns on NM7 and provides a discharge channel from BLB, NM7, NM4, NM8, and a voltage difference is formed between BL and BLB, which is sensed by the sensing amplifier, which makes a decision. The read time is calculated by discharging BLB from 90% to 10% of V_{DD} through the discharging route.

Table 1. Table for various operation performed by 10T SRAM CELL

	Data stored			
	Write 1	Write 0	Read	Hold
WWL	1	1	0	0
BL	1	0	1	0
BLB	0	1	"Discharge"	0
RWL	0	0	1	0
CS	1	1	0	1
GP	1	1	1	0

5. Simulation Results and Discussion

Cadence Tool is used to evaluate the proposed 10T SRAM cell. Cadence's SPECTRE simulator generates waveforms. In this article, a comparison of 6T and 10T SRAM cells in 180 nm (UMC) technology has been made in terms of average power, total power consumption, write margin (WM), and RSNM of proposed 10T and traditional 6T SRAM cells. 6T read and write operations for transient analysis are done. The write and read operations of the proposed

10T SRAM are depicted in Figures 3 and 4, respectively, while Figures 5 and 6 show the write and read operations of the proposed 10 SRAM.

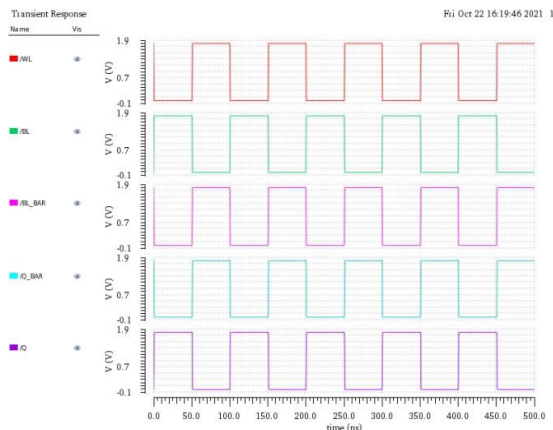


Fig.3 write operation of 6T SRAM Cell

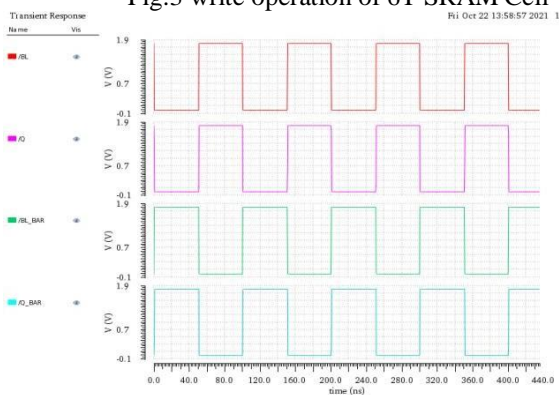


Fig.4. Read operation of 6T SRAM Cell

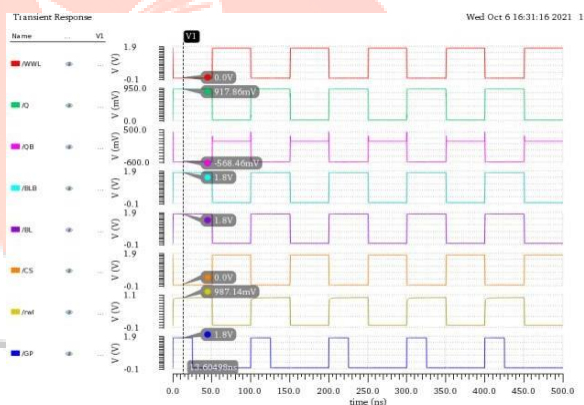
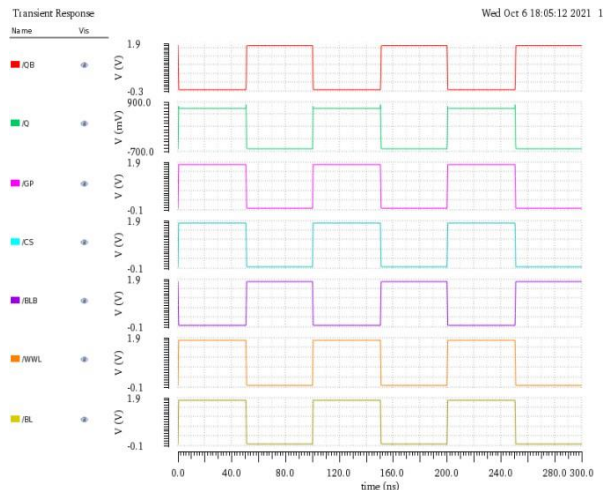
Fig.5 write operation of 10 T SRAM Cell

Fig. 6 Read operation of 10T SRAM Cell

5.1 Power Consumption

In today's digital world, portable devices are employed, and low power consumption is more useful for that purpose, power dissipation is an important element in VLSI design. people always need a gadget that uses extremely little power, and there are several circuit design strategies for reducing

leakage power in circuits. Short circuit, switching, and leakage power dissipation are all common



sources of circuit power dissipation in VLSI circuit designs using CMOS technology. In CMOS, there are primarily two types of power dissipation: dynamic and static power dissipation. Static power consumption occurs when the circuit is in a static state with no input/output changes. Dynamic power consumption is also known as active power or charging and discharging capacitors [7, 8]. Static power is also known as DC power. The sum of dynamic and static power is used to compute total power. Fig 7 depicts the total power versus VDD graph for both the proposed 10T and the conventional 6T. Fig 8 represents the layout design of 10T SRAM CELL of the proposed design.

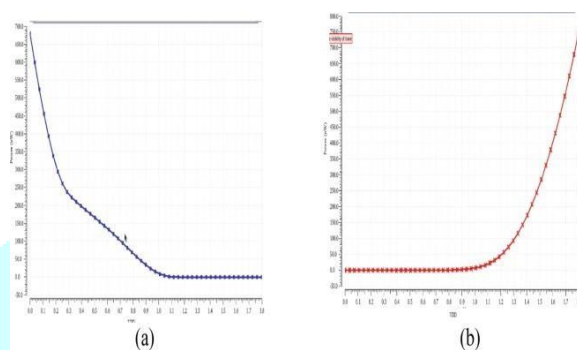


Fig.7 Power versus VDD graph for SRAM cell (a)proposed 10T SRAM cell (b)conventional 6T SRAM cell

Table 2. Result for different SRAM Cells

SRAM cells	Parameters					
	Technology	Power supply	power		Delay	
			Write	Read	Write	Read
6T	180 nm	1.8	751uw	759uw	192.2	201.5
10T	180 nm	1.8	0.642mw	15.25mw	50.6N W	175.6N W

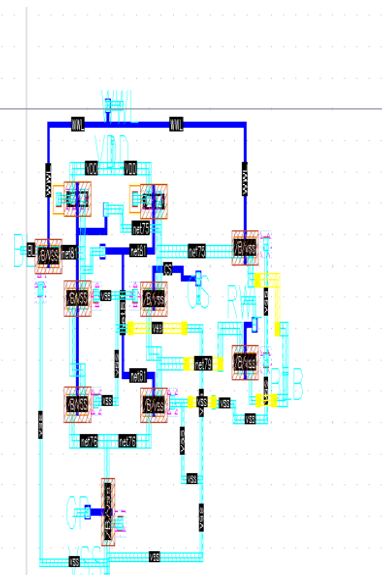


Fig.8 layout design of 10T SRAM cell

6. Acknowledgements

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7. Conclusion

Author have compared the result with conventional 6T SRAM Cell and concluded that represented result are improved .this design have achived 1.5X and 1.52X WM Respectively at 1.8V supply voltage .

REFERENCES

[1] Shivaprakash, G., Suresh, D.S.: Design of low power 6T-SRAM cell and analysis for high speed application. Indian J. Sci. Technol. 9(46) (2016).
 [2] H., Agarwal, D.: Single bit line 10T SRAM cell for low power and high SNM. In: Proceeding International Conference on Recent Innovations in Signal Processing and Embedded Systems (RISE - 2017) 27-29 October 2017
 [3] Priya, S., Gavaskar, K.: Design of efficient low power 9T SRAM cell. Int. J. Eng. Res. Technol. (IJERT) 2(1) (2013)
 [4] Rukkumani, V., Saravanakumar, M., Srinivasan, K.: Design and analysis of SRAM cells for power reduction using low power techniques. 978-1-5090-2597-8/16/\$31.00. IEEE (2016)
 [5] Upadhyay, P., Kar, R., Mandal, D., Ghoshal, S.P.: A novel IOT SRAM cell for low power circuits. 978-1-4799-3358-7/14/\$31.00. IEEE (2014)
 [6] Yan, H., Wang, D., Hou, C.: The design

of low leakage SRAM cell with high SNM. 978-1-61284-193-9/11/\$26.00. IEEE (2011)

[7] Singh, P., Vishvakarma, S.K.: Ultra-low power high stability 8T SRAM for application in object tracking system. 216-3536 (2017)

[8] Manav Bansal, Ankur kumar, Priyanka Singh and R.K Nagaria A Novel 10T SRAM cell for Low Power Applications (2018) IEEE Uttar Pradesh

