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DESIGN AND IMPLEMENTATION OF SEQUENTIAL CIRCUITS USING REVERSIBLE LOGIC CIRCUIT TECHNOLOGY

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ABSTRACT

Quantum computing, nanotechnology, optical computing, DNA computing, digital signal processing (DSP), quantum dot cell automata (QCA), communication, and computer graphics all use reversible logic. To achieve quantum computing, the introduction of reversible logic is needed. Reversible logic can reduce quantum costs, circuit depth, and the number of trash outputs. As these circuits may generate separate responses from specific inputs and vice versa, no information is lost. CMOS architecture can be used for a wide range of applications, including optical information processing, quantum cryptography, quantum computation, and nanotechnology. Design of a Flip-Flop Flip-Flop Counter and Universal Shift Register is presented in this paper. In the sequential circuit family, the universal shift register is essential. This research presents a universal shift register that is optimised in terms of quantum cost, delay, and garbage outputs.

1. INTRODUCTION

VLSI design requires careful consideration of energy dissipation. Reversible logic and energy dissipation were first linked by Landauer, who claimed that information loss caused by function irreversibility results in a loss of energy. – Landauer Only reversible gates, in Bennett's opinion, can guarantee zero energy loss in a circuit. If the input vector cannot be uniquely reconstructed from the output vectors, then information is lost. Because each input vector can be recovered from its output vectors in reversible logic circuits, heating is avoided. It is only possible to achieve zero energy dissipation if the network is made up of reversible gates. To put it another way, circuit design in the future will require reversibility as a fundamental quality. The loss of bits of information in reversible circuits entails energy loss. Younis and Knight demonstrated that allowing a circuit's delay to be arbitrarily large can result in asymptotically energy-loss-free reversible circuits. However, there are two issues with reversible logic. Reversible gates can't be built because there aren't enough technologies available to do so. It's safe to say that progress is being made in this area. A second issue is that, while reversible logic is a hot topic for designing combinational circuits, little work has been done on implementing it sequentially. A sequential computer can be built using invertible logic gates with minimal internal power dissipation since reversible logic has no fundamental limitation that prevents it from being designed. The concept of reversible logic has been around since 1980, when Tommaso Toffoli published Reversible Computing.

Conservative logic, which is a form of logic, has an equal number of 1s in its output and inputs. It's all about the degree of reversibility in conservative logic. As a result of conservative logic, this proposed approach has no internal power dissipation, which is an additional benefit. As long as the input and output vectors are constantly mapped one to one, this trait is known as reversibility and may always be used to rebuild the vector of input states. Fanout is not possible with reversible logic, which ensures that an output is provided for every input. Reversible logic, which makes testing simple, rigorously limits the number of outputs that can be generated from a single input. The term "reversible conservative logic" refers to conservative logic in which the input and output vectors have a one-to-one mapping and the outputs have the same number of 1's as the inputs. Heat dissipation occurs when a circuit is built in an irreversible fashion, which means that some information is lost. There are many dead ends in traditional models, but conservative logic avoids them and offers new perspectives.

Numerous applications for quantum computers include low-power CMOS architecture as well as nanotechnology and DNA computations. The system must have reversible gates to do reversible computation. To be reversible, an input and output vector must be unique and have a direct one-to-one link. These are the most challenging challenges to overcome while designing reversible circuits. We were able to reduce the quantum cost and trash outputs by designing the universal shift register.

2. LITERATURE REVIEW

S Ankur Sarker et al. presented a design for addition and subtraction using reversible gates several years ago. Additionally, the quantum and trash outputs are reduced by this circuit's reduced number of logic gates as well as its reduced quantum cost. The presented architecture improved trash output by 33.33 percent, quantum cost by 26.66 percent, and gate count by 50 percent.

Two Feynman gates and two Fredkin gates were used by Sayyad Khaja Moinuddin and colleagues in 2015 to create a 2:4 reversible decoder. Depending on the number of lines you want to decode, the reversible decoder we recommend lets you choose between a high or low active mode. This device can be scaled to 3:8 decoders because of its low quantum cost.

It was reported in 2015 that Md. Samiur Rahman and et.al have developed an improved full-subtractor design that made use of new SRG reversible logic gates and VHDL simulations. A Full-subtract circuit was created by using the SRG gate alone. Large reversible systems based on nanotechnology can be designed using the methods outlined in this proposal.

An online testable ripple carry adder was developed by Avishek Bose et al. in 2015. The most important feature of this design is that no input line has any influence on any other input line. In comparison to the previous design, this one reduces the number of gates by 25%, the quantum cost by 42.30%, and the number of constant inputs by 50%.

Reversible logic gates' performance was evaluated in a research published in 2016 by Umesh Kumar et.al. A comparison of classical and quantum gates is made in this study. Toffoli, Fredkin, and Peres gates are just a few of the reversible logic gates that can be employed to cut down on power usage and heat generation.

A reversible 8-bit ALU was developed in 2016 using cascading 1-bit ALUs. Control and adder units were essential in the design of 1-bit ALUs. The control and adder units have been implemented using the COG and HNG, respectively. The proposed design is less susceptible to propagation delays when compared to the previous design.

Researchers in 2017 suggested a new design for the Reversible floating-point square root, which uses an algorithm that is modified non-restoring. In each stage, the non-restoring technique used a less number of logical resources than the restoring method. This floating-point square root has been

lowered in size and power usage by using the GST algorithm. Many different designs have been compared, however this one has a lower total number of reversible gates and a lower overall quantum cost.

Quantum Cellular Automaton (QCA) was utilised to test a design for an Arithmetic Logic Unit (ALU) in 2017. It is possible to use this Arithmetic Logic Unit in low-power applications. This architecture reduces both quantum costs and garbage emissions. It has improved by 50% in terms of constant inputs, gate counts, and cells.

Dhoumendra Mandal et al. suggested a reversible logic gate-based all-optical one-bit binary comparator in 2017. This architecture's one-bit comparator was built utilising reversible logic gates that encoded data in frequency. All optical ALUs can be proposed using this comparator circuit.

3. REVERSIBLE EQVIVALENT GATES USED FOR DESIGNING SEQUENTIAL CIRCUITS

3.1 Basic Definitions pertaining to reversible logic

Reversible logic gate :

In reversible gates, one-to-one matching of inputs and outputs enables circuit reversal. There are many ways in which it can be used, but it is most useful for determining outputs from their respective sources.

Constant inputs:

The input count is the number of inputs that must remain at 0 or 1 when synthesising a logical function.

Garbage outputs:

As long as there is an equal number of inputs and outputs, it is possible to add additional components. It's also taken into account here how many outputs aren't used in the synthesis of a certain function To reverse an n-input, k-output function, the number of outputs that must be added is known as "trash". Introducing reversible constant inputs into a (n:k) function is known as "constant inputs." Garbage outputs are shown in this simple formula. Adding consistent input to a steady stream of input results in an inefficient outcome.

3.2 Eqvivalent gates used for designing sequential circuits

Sequential circuits' typical logic gates are designed using reversible gates. Reversible gates and trash outputs are minimised by designing the classical logic with this in mind. Fredkin gate-based design for the AND function is shown in Fig. 1.

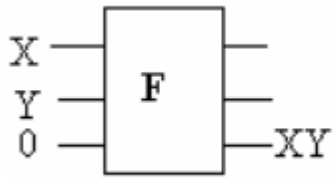

Figure 1. Fredkin Gate as AND Gate

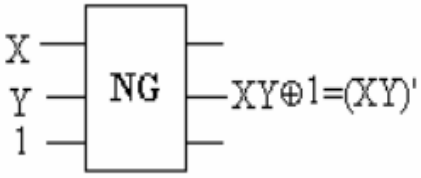

Figure 2. New Gate As NAND Gate

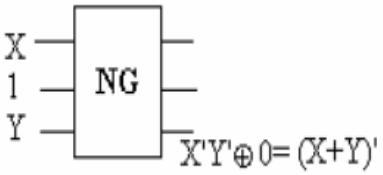

Figure 3. New Gate As NOR Gate

Figures 2 and 3 show the New Gate-designed NAND and NOR operations. In reversible logic, the fan out problem can be avoided using Feynman Gates. As long as the second input is set to a value of zero, the Feynman gate replicates the first input into both output ports. For a single copy of a bit, Feynman gates are the best option because they do not produce any garbage.

4. METHODOLOGY

The BME gate is a novel four-by-four reversible logic gate that we've developed. O is the output vector for the input vector I(A,B,C,D) (P,Q,R,S). S = ABCD. The output is specified by the values of P (A), Q (AB), R (AD), and S (AB). Figure 4 is a block schematic of a BME gate.

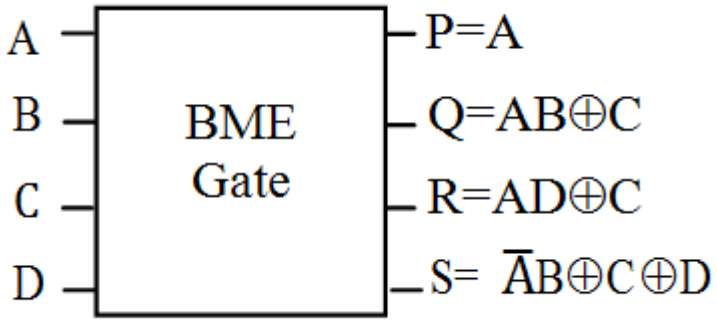

Figure 4: Block diagram of a new reversible BME gate.

Table 1: Truth Table of New Reversible BME Gate

A	B	C	D	A	AB⊕C	AD⊕C	A B⊕C⊕D
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	0
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	0
1	1	0	1	1	1	1	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	0	0

When we use our BME gate's truth table, we can verify its reversibility by comparing the output and input vectors. Table 1 has 16 separate input and output vectors, each of which has a one-to-one mapping. The BME gate is reversible, hence it fits the criterion.

Design of reversible universal shift register

A. Proposed Universal Shift Register 1

Using a clock signal, universal shift registers can be shifted to the left or right. All modes of operation, including SISO and PIPO, are activated as soon as a clock signal is received. Figure 5 shows our universal shift register, which consists of a 1 to 4 demultiplexer and four D flipflop blocks.

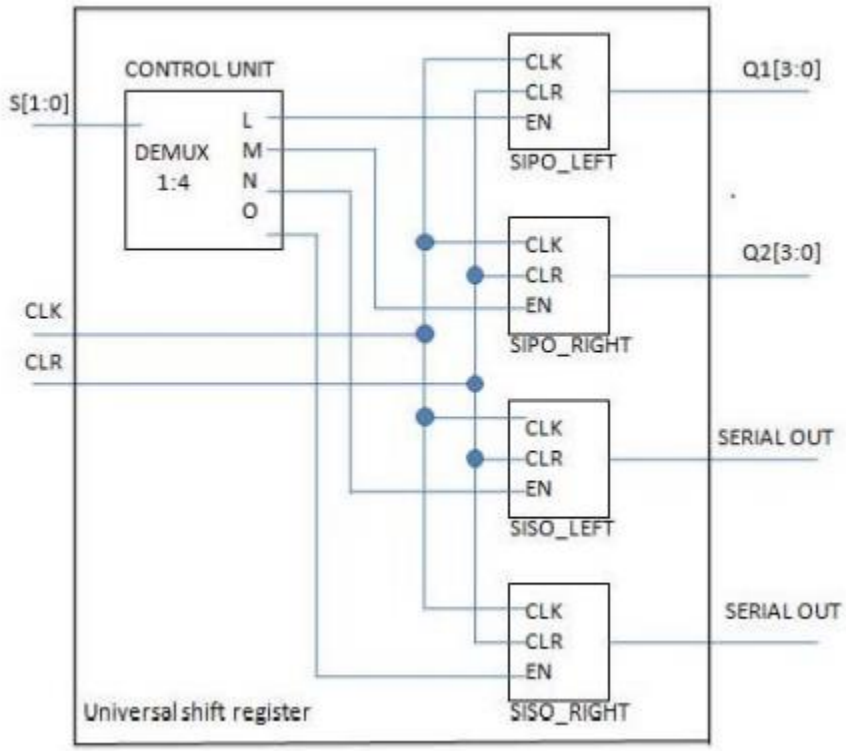

Fig.5. Block diagram of Universal shift register1

The multiplexer accepts S1 and S0 as inputs. This register value is applied to the D inputs of the flip flop when SIPO-LEFT is 10. Current register value is applied to the flip flop D inputs when SIPO-LEFT is equal to 11. It is possible to feed the output of one flip-flop back into the input of another flip-flop, and so on, when this condition is met.

B. Proposed Universal Shift Register 2

To shift the data stored in universal shift registers, a clock signal is required. Timer events can be used to accomplish all operations, including SIPO, PIPO, and PISO, as well as SISO (serial-serial output), PISO (parallelin-serial output), and PIPO (parallel-in-parallel output).

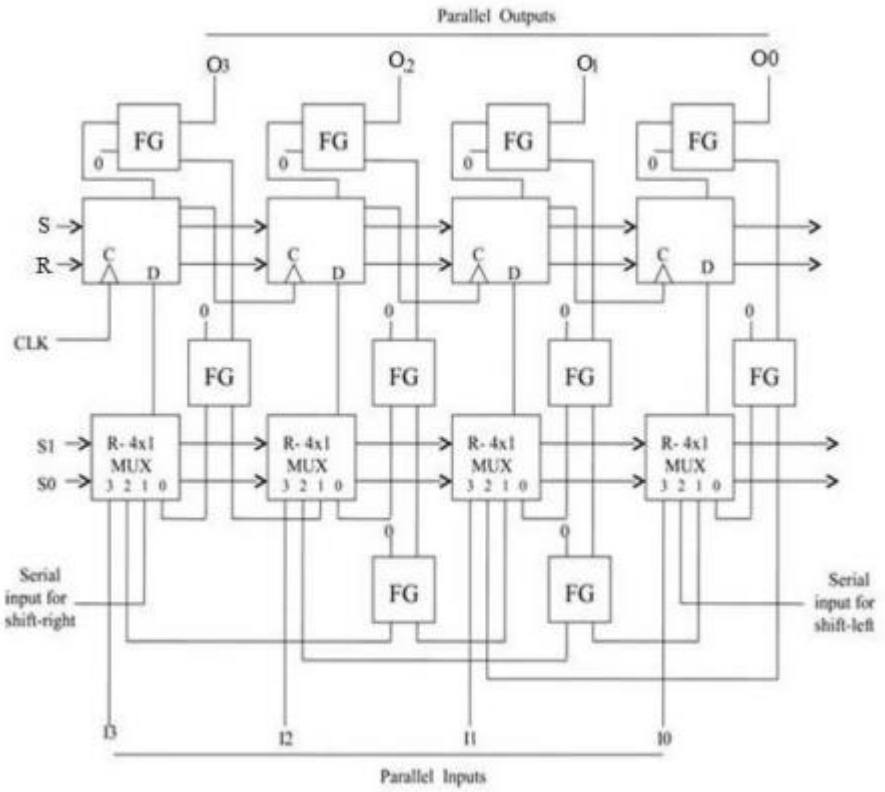

Fig.6. Block diagram of Universal shift register2

Fig. 6 shows a proposed architecture for a Universal Shift Register that includes flip-flop blocks employing Master Slave D FF, D FF, and 4:1 Multiplexers, depending on whether the set/rest is done synchronously or asynchronously.

4. RESULTS AND DISCUSSION

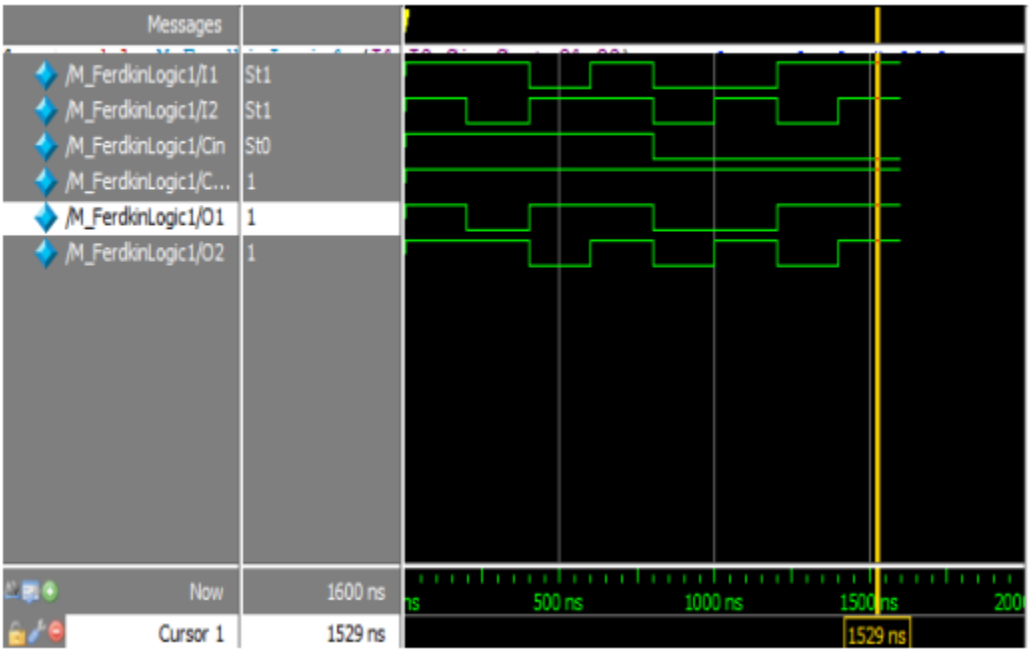

Fig.7 Fredkin gate.

Figure 7 depicts the simulation results obtained with the Xilinx ISE simulator. A control signal of 1 results in equal outputs and inputs when the control signal is applied. By way of illustration, the identical outcome may be obtained by setting the control signal to 0 and then swapping the two outputs.

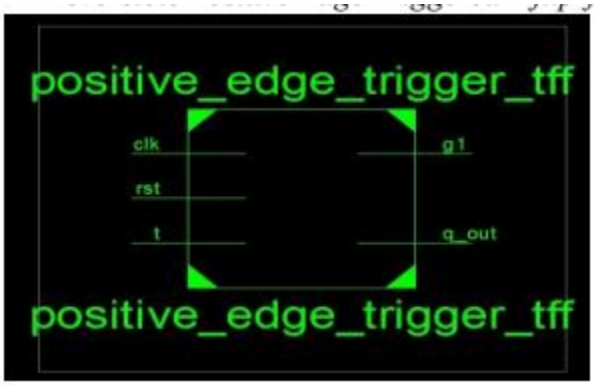

Fig 8 Reversible Positive Edge Triggered T flip-flop.

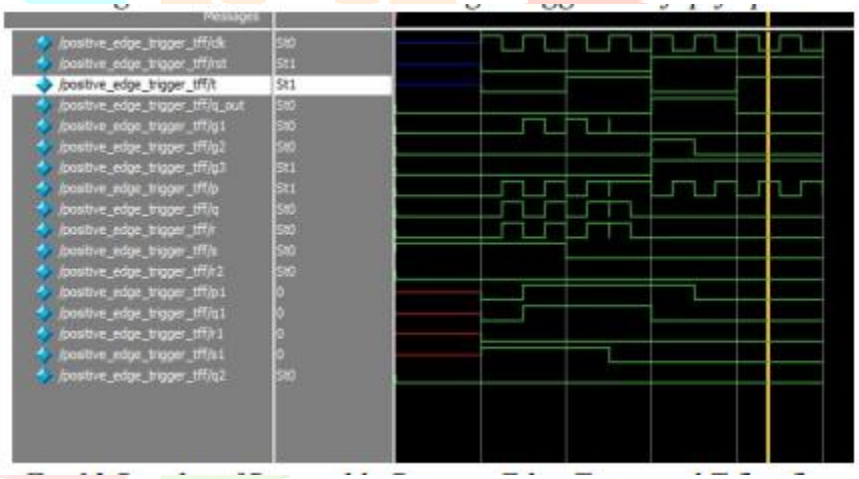

Fig 9 Results of Reversible Positive Edge Triggered T flip-flop

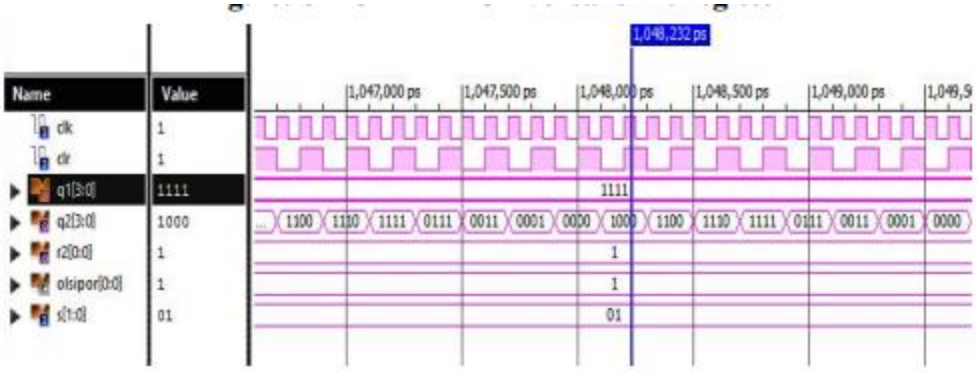

Fig.10. SIPO-RIGHT Universal shift register.

This means that when the clock is struck, all modes of operation, such as SISO and PIPO, can be performed. Figure 10 shows our universal shift register, which consists of four 4-to-1 Demultiplexer blocks and four D flip flop blocks.

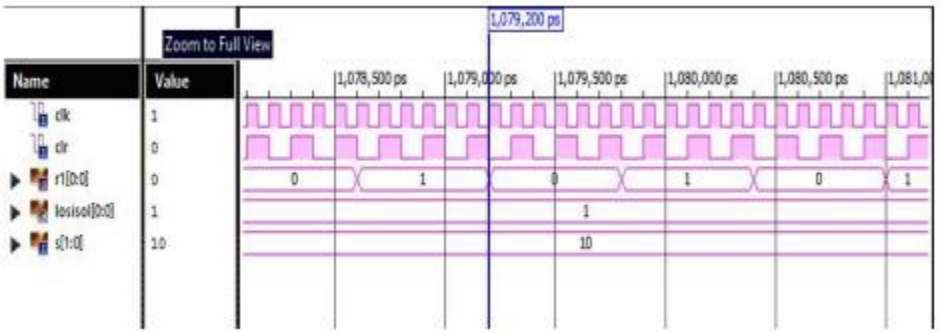

Fig.11. SISO-LEFT Universal shift register.

S1 and S0 are both common inputs for the multiplexer. When SIPOLEFT is 00, SIPO-RIGHT is 01, SIPO-LEFT is 10, and SIPO-RIGHT is 11, each flip flop has its D inputs applied to its D inputs. In this mode of operation, the output is recalculated to the input if the flip flop output is connected to it.

CONCLUSION

In this paper, latches, flip-flops, and counters are explored in detail. Because of the fewer gates, garbage outputs, and constant inputs, it's a simpler counter. A comparison of prior designs has also been done. The asynchronous and synchronous counters reversible sequential circuit design presented here is efficient and optimised. To develop quantum computers with huge and complicated reversible sequential circuits, this research is critical. Reversible counters and reversible controllers could be the focus of future research. There is no inherent support for testability in the sequential circuits developed using standard classic gate circuits. In order to test a traditional sequential circuit, the original circuitry must be altered. Increasing the complexity of a sequential circuit also increases the number of test vectors required to test it. The same sequential circuit can be checked with only two test vectors, all 0s and all 1s, if it is built using proposed reversible sequential building blocks, however thousands of test vectors are required to test all stuck-atfaults in a complex sequential circuit.

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