IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Design Technique and Implementation of a Novel Multilevel DC–AC Inverter

[1]Ms. Pratibha Patil, [2]Dr.S.N.Patil, [3] Prof.A.P.Kinge

[1] PG Student, [2] Professor, [3]Professor

[1]Electrical Engineering Department,

[1]TSSM's Bhivarabai Sawant College of Engineering and Research,Narhe, Pune, Maharashtra, India

Abstract: Multilevel inverters have been widely accepted for high-power high-voltage applications though the multilevel inverters hold attractive features, usage of more switches in the conventional configuration poses a limitation to its wide range application. Therefore, 7-level inverter topology is introduced using less number of switches and gate trigger circuitry, thereby ensuring the minimum switching losses, reducing size and installation cost. Multilevel inverter (MLI) plays a vital role in the field of power electronics and being widely used in many industrial and commercial applications. The multilevel inverter topology is the proper option from the point of view of modularity and simplicity of control.

Index Terms - **Multilevel DC to AC inverter, PIC Microcontroller, SPWM.**

I. INTRODUCTION

High power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms.

One of the power converters which can transform dc–ac is called inverter. Inverter is the inter medium which transmits power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid composed of renewable energy shown in Fig. 1. To satisfy different demands and characteristic of loads, the output Frequency and voltage have to change with different loads. In recent years; the amount of power equipment is increasing. Therefore, the harmonic pollution of power system becomes more serious. Several standards and regulations have been formulated to limit quality of harmonics and power factor of electric equipment.

Furthermore, in order to meet the industry requirements for high power applications, the voltage stress of the power Device also increases. Although an insulated gate bipolar transistor (IGBT) has features of high power rating and high voltage stress, it cannot operate at high frequency. And the design of IGBT gate driver is complicated. AMOSFET is the appropriate Component to operate at high frequency, but power rating is not as good as IGBT. To solve the problem, many different topologies of multilevel use low rating component at high-power application.

The purpose of the multilevel topology is to reduce the voltage rating of the power switch. Therefore, it usually is used at High-power application. By combining output voltages in multilevel form, it has advantages of low dv/dt, low input current distortion, and lower switching frequency. As a result of advantages of multilevel topology, several topologies have emerged in recent years. A novel multilevel inverter is designed and implemented in this paper. The major feature of the proposed topology is the reduction of power components.

II. LITERATURE REVIEW

Important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses.[1]

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower Voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected Percentage of THD for R, RL, RLC load [2]

A multilevel concept is usually a unique alternative because it is based on low-frequency switching and provides voltage and/or current sharing between the power semiconductors. For low power systems multilevel converters have been competing with high-frequency pulse width-modulation converters in applications where high efficiency is of major importance [7]

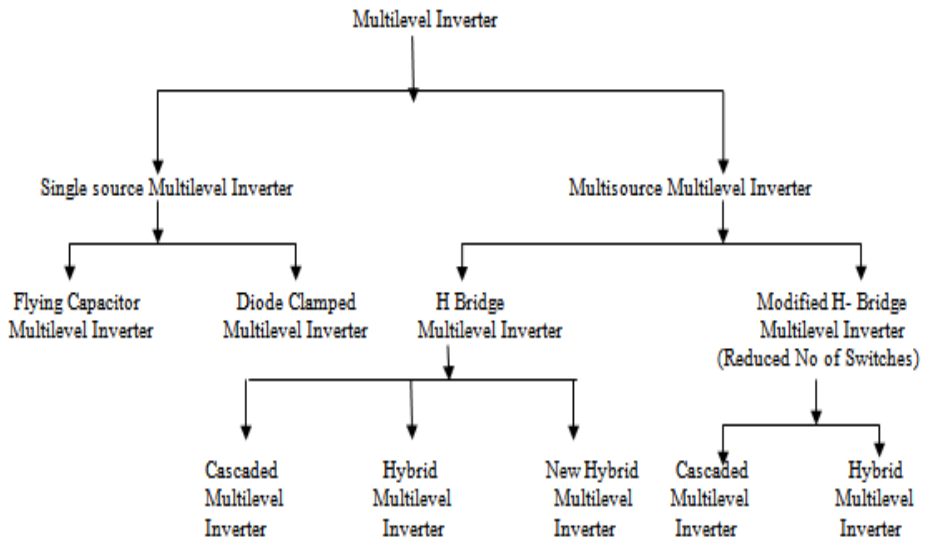
As we know multilevel power conversion has become increasingly popular in recent years due to compatibility, and can supply high voltage as compared to the value of dc supply. However, as we increase the levels of output waveform the number of switches in the system also increases and to control these switching devices the number of other components also increases and this lead us towards complexity as well as higher system cost.

Multilevel inverters have been mainly used in medium or high power system applications, such as static reactive power compensation and adjustable-speed drives. Multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application.[9]

Multilevel inverters have received more and more attention because of their capability of high voltage operation, high efficiency and low electromagnetic interference (EMI). The desired output of a multilevel inverter is synthesized by several sources of DC voltages. With an increasing number of DC voltage-sources, the inverter voltage output waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. This results in low switching losses, and because of several DC sources, the switches experience lower voltage stresses.[10]

Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique[11].

III. CLASSIFICATION OF MULTILEVEL INVERTER



IV. POWER STAGE

a. Circuit Configuration

Fig. 2 shows the proposed novel topology used in the seven level inverter. An input voltage divider is composed of three series capacitors $C1$, $C2$, and $C3$. The divided voltage is transmitted to H-bridge by four MOSFETs, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design

b. *Operating Principles*

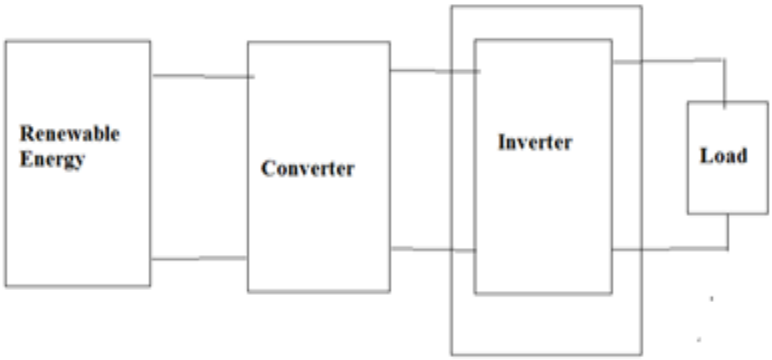


Fig 1. Block diagram of Renewable system

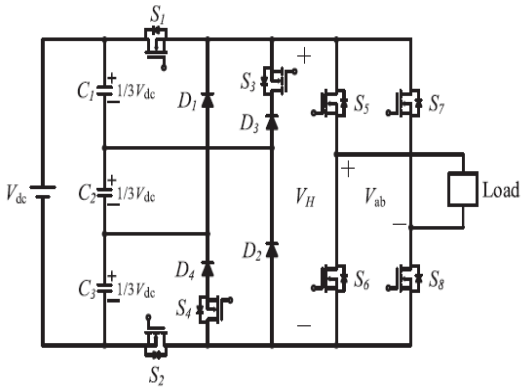


Fig.2. Proposed seven-level inverter topology

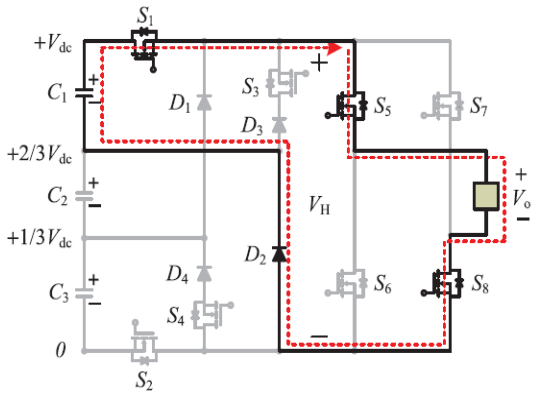


Fig. 3. Switching combination of output voltage level 1/3V_{dc}

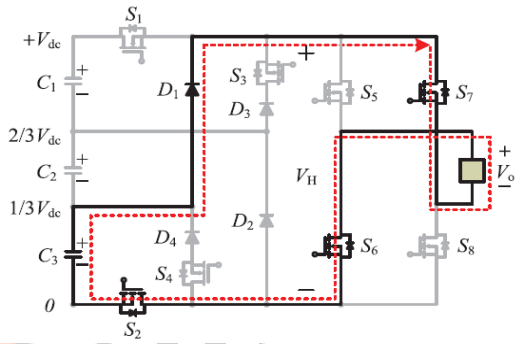


Fig. 6.Switching combination of output voltage level -1/3V_{dc}.

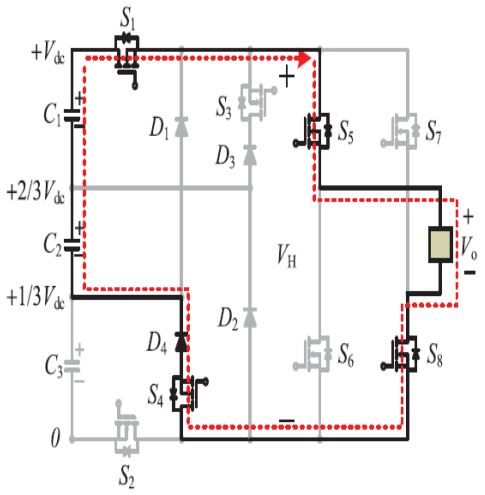


Fig 4. Switching combination of output voltage level 2/3V_{dc}

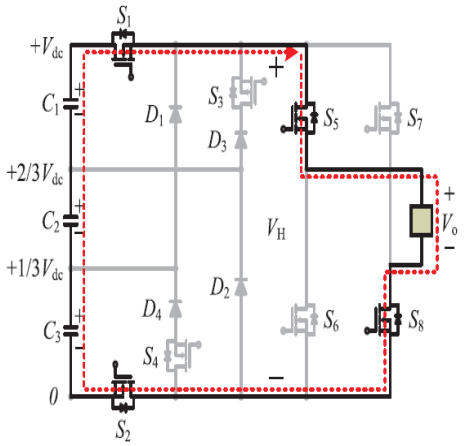


Fig 5. Switching combination of output voltage level V_{dc}.

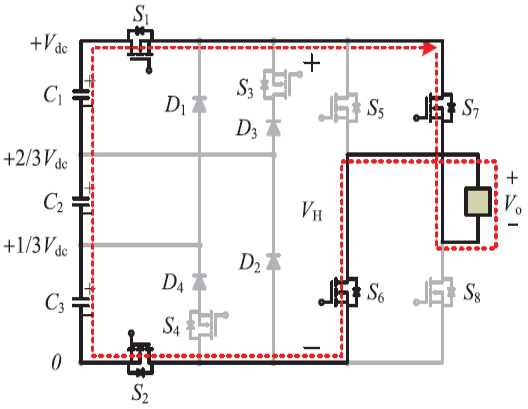


Fig. 8.Switching combination of output voltage level -V_{dc}.

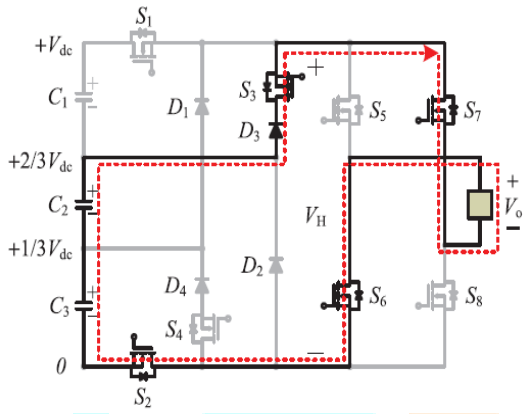


Fig. 7.Switching combination of output voltage level -2/3V_{dc}.

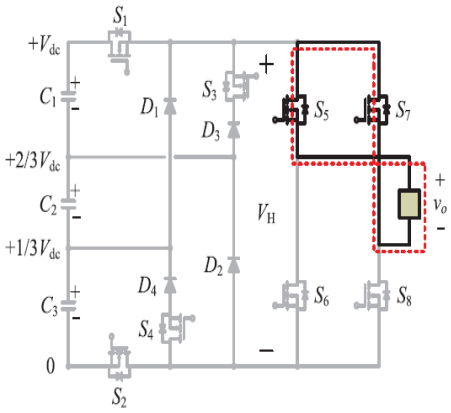


Fig. 9.Switching combination of output voltage level 0.

The required seven voltage output levels ($\pm 1/3Vdc$, $\pm 2/3Vdc$, $\pm Vdc$, 0) are generated as follows.

1) To generate a voltage level V0 = $1/3Vdc$, $S1$ is turned on at the positive half cycle. Energy is provided by the capacitor $C1$ and the voltage across H-bridge is 1/3Vdc. S5 and S8 are turned on, and the voltage applied to the load terminals is $1/3Vdc$. Fig. 3 shows the current path at this mode.

2) To generate a voltage level Vo= $2/3Vdc$, $S1$ and $S4$ are turned on. Energy is provided by the capacitor $C1$ and $C2$. The voltage across H-bridge is $2/3Vdc$. $S5$ and $S8$ are turned on, and the voltage applied to the load terminals is 2/3Vdc. Fig. 4 shows the current path at this mode.

3) To generate a voltage level $V0 = Vdc$, S1 and S2 are turned on. Energy is provided by the capacitor C1, C2, and C3. The voltage across H-bridge is Vdc. S5 and S8 are turned on, and the voltage applied to the load terminals is Vdc. Fig. 5 shows the current path at this mode.

4)To generate a voltage level V_o= $-1/3V_{dc}$, S_2 is turned on at the negative half cycle. Energy is provided by the capacitor C_3, and the voltage across H-bridge is $1/3V_{dc}$.S_6 and S_7 are turned on, and the voltage applied to the load terminals is $-1/3V_{dc}$. Fig. 6 shows the current path at this mode.

5)To generate a voltage level V_o= $-2/3V_{dc}$, S_2 and S_3 areturned on. Energy is provided by the capacitor C_2 andC_3. The voltage across H-bridge is $2/3V_{dc}$. S_6 and S_7 areturned on, and the voltage applied to the load terminals is$-2/3V_{dc}$. Fig. 7 shows the current path at this mode.

6) To generate a voltage level V_o=$-V_{dc}$, S_1 and S_2 are turned on. Energy is provided by the capacitor C_1, C_2, and C_3, the voltage across H-bridge is V_{dc}. S_6 and S_7 is turned on, the voltage applied to the load terminals is $-V_{dc}$. Fig. 8 shows the current path at this mode.

7) To generate a voltage level V_o= 0, S_5 and S_7 are turnedon. The voltage applied to the load terminals is zero.Fig. 9 shows the current path at this mode.

c. Topology Comparison

TABLE I: SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

TABLE II : COMPONENTS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

TABLE III : VOLTAGE STRESS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

Table II presents the number of components required to implement a seven-level inverter using the proposed topologyand three previously ones [9], [10] that can be considered as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multicellular inverter.
Table II shows that the new topology achieves the reductionin the number of power devices.
Table III shows the voltagestress comparison between different type inverters.

V. CONTROL TECHNIQUE

The main aim of the modulation strategy of multilevel inverters is to synthesize theoutput voltage as close as possible to the sinusoidal waveform. Many modulationtechniques have been developed for harmonic reduction and switching loss minimization.The modulation methods used in multilevel inverters can be classified according toswitching frequency. Methods that work with high switching frequencies have manycommutations for the power semiconductors in one period of the fundamental outputvoltage. Output voltage from an inverter can also be adjusted by exercising a controlwithin the inverter itself. The most efficient method of doing this is by pulse widthmodulation control used within an inverter. In this method, a fixed dc input voltage isgiven to the inverter and a controlled ac output voltage is obtained by adjusting the ONand OFF periods of the inverter components. This is the most popular method ofcontrolling the output voltage and this method is termed as Pulse-Width Modulation (PWM) Control.

Mainly the power electronic converters are operated in the switched mode. This means the switches within the converter are always in either one of the two states -turned off or turned on. Any operation in the linear region, other than for the unavoidabletransition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states. This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average orfilter the switched signal. The switched component is attenuated and the desired dc or low frequency ac component is retained. This process is called Pulse Width Modulation, since the desired average value is controlled by modulating the width of the pulses.

VI. Advantages of PWM technique

The advantages possessed by PWM techniques are as under:

- The output voltage control can be obtained without any additional components.
- The lower order harmonics can be eliminated or minimized along with its output voltage control.
- The filtering requirements can be minimized as higher order harmonics can be filtered easily

VII.Sinusoidal Pulse Width Modulations

In this type of modulation the width of each pulse is varied in proportion to theamplitude of sine wave evaluated at the centreof the same pulse. The gating signal isprovided by comparing a sinusoidal reference signal with a triangular carrier signal. The frequency of the reference signal determines the output frequency of the inverter and itspeak amplitude Ar controls the modulation index.As mentioned earlier, it is desired that the ac output voltage Vo=Vao follow agiven waveform.(e.g., sinusoidal) on a continuous basis by properly switching the powervalues. The carrier based PWM technique fulfils such a requirement as it defines the ONand OFF states of the switches of one leg of a VSI by comparing a modulating signal Vr(desired ac output voltage) and a triangular waveform Vc (Carrier Signal). In practice, from Fig, when Vr>Vc the switch S+ is on and the switch S- is off; similarly, when Vr<Vcthe switch S+ is off and the switch S- is on. A special case is when the modulating signal Vr is sinusoidal at frequency Fr and amplitude Ar and the triangular signal Vc is at afrequency fc and amplitude Ac. This is the Sinusoidal PWM (SPWM) scheme. In this case,the modulation index ma (also known as the amplitude-modulation ratio) is defined as

$$ma = Ar/Ac \quad (4.1)$$

and the normalized carrier frequency mf (also known as the frequency-modulation ratio) is

$$mf = fc/fr \quad (4.2)$$

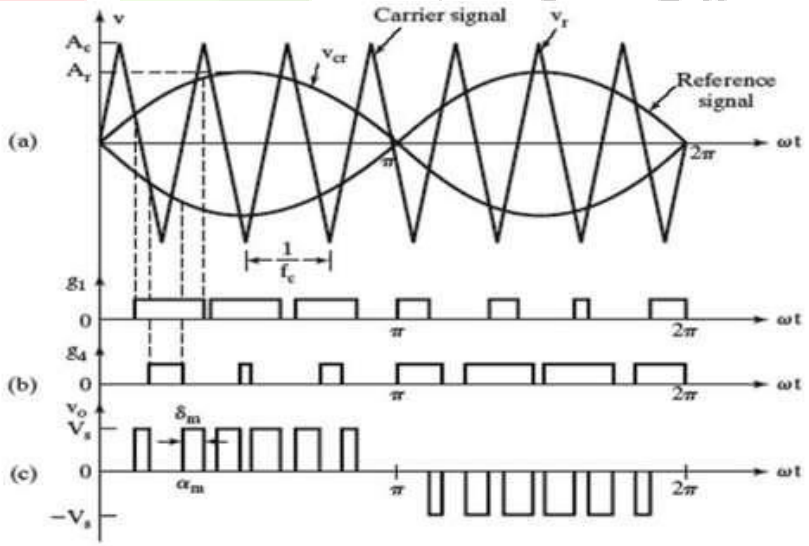


Fig.13 Sinusoidal Pulse Width Modulation

V. PI CONTROL USED IN MODIFIED SPWM

Modified SPWM based on PI control is used in this paper [18], [19]. Fig. 14 shows the block diagram of PI control. Theblock diagram can be expressed in S domain as

$$u(s) = \left[K_p + \frac{K_i}{s}\right] e(s). \quad (3)$$

From (3), the equation can be transformed in the Z domain as

$$u(z) = \left[K_p + \frac{K_i}{1 - z^{-1}}\right] e(z). \quad (4)$$

Then, transform (4) becomes a difference equation isexpressed as

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1] \quad (5)$$

Fig. 15 shows system configuration and control block.System detects output voltage first and compares this signalwith a built-in reference. Then, the system feedbacks an error toPI controller. Finally, the PI controller exports a control signalto gate driver.
The main idea of modified SPWM is to record the previouserror of output voltage and generate a suitable correction at thelatest cycle. Because the frequency of carrier is 18 kHz and thefrequency of output sine wave is 60 Hz, the number of times ofswitching is 300 times. Fig. 16 shows the schematic of modified .SPWM.$v_{ref}[n]$ is defined as the reference output voltage, $v_o[n]$ is thefeedback of output voltage, and $e[n]$ is error between referenceoutput and feedback output which is expressed as

$$e[n] = v_{ref}[n] - v_o[n] \quad (6)$$

Let$K_1 = K_p + K_i, K_2 = K_p$, then $e[n]$ is multiplied by$K_1$and $e[n-300]$ multiplied by K_2. Then, add the previous outputsignal $u\_[n-300]$. Finally, it can obtain the output of PIcontroller after the process by the anti-windup.

$$u'[n] = K_1 \cdot e[n] - K_2 \cdot e[n-300] + u'[n-300]. \quad (7)$$

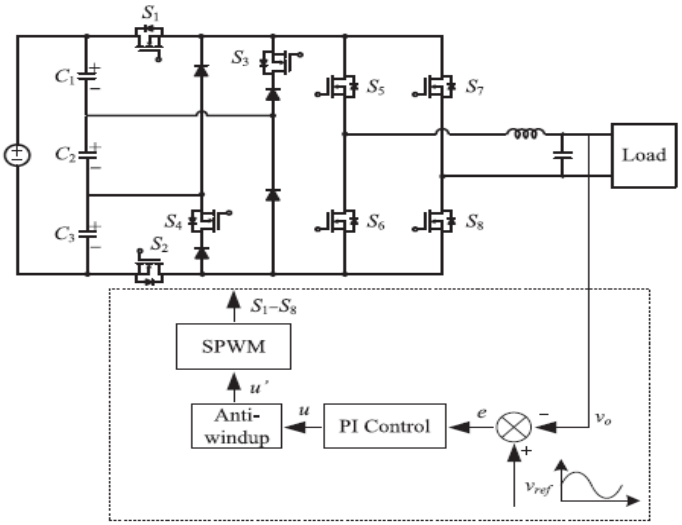


Fig. 15.Seven-level inverter with control algorithm.

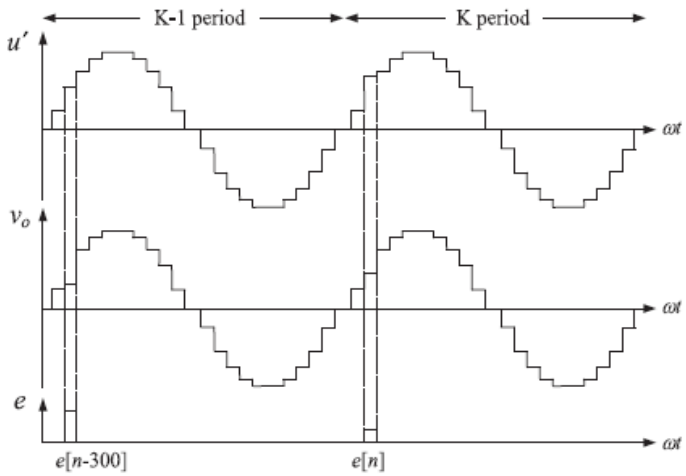


Fig. 16.Schematic of modified SPWM.

TABLE IV
Specifications of the proposed inverter

Input Voltage Vdc	18 V
Output Voltage Vo	Vp=18V,Vrms=12
Rated Output Power Po	30 W
Switching Frequency	10 Khz

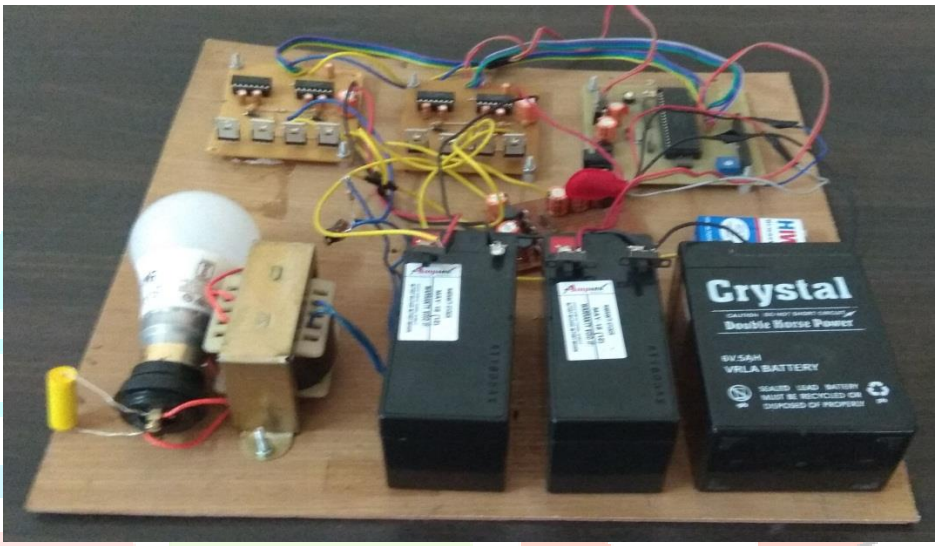
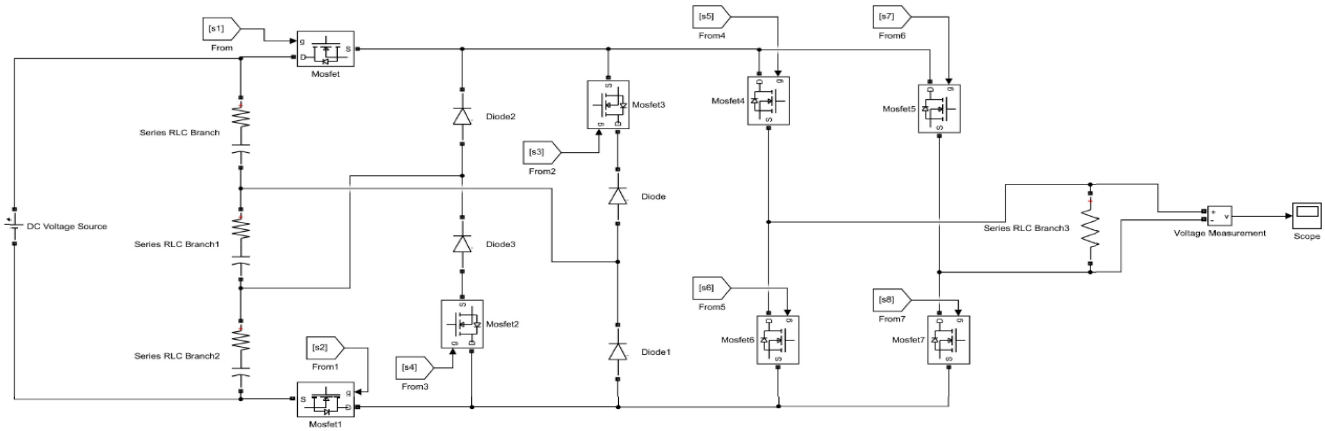


Fig.17 Experimental Setup

VII. **SIMULATION RESULTS**



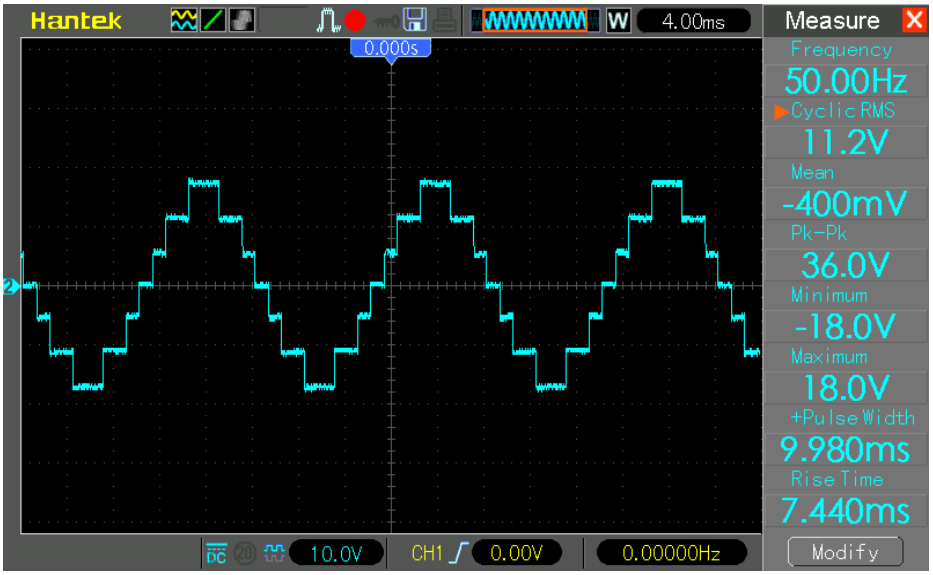


Fig.18 Output Waveform

VI. CONCLUSION

Seven level multi-string inverters is the best suited topology for the dc to ac conversion and gives better output in space vector modulation. In seven level multi-string inverters due to the better ac to dc conversion the harmonic losses will be totally reduced. Hence we require small size filter in proposed method. So it is better to prefer, seven levels multi-string inverter for industrial drives to get low cost, easy operation, high efficiency.

A novel seven-level inverter was designed and implemented with PIC controller in this paper. The main idea of the proposed configuration is to reduce the number of power device. The reduction of power device is proved by comparing with traditional structures. Finally, a laboratory prototype of seven-level inverter with 18V input voltage and output 12 V_{rms}/30W is implemented.

VII. REFERENCES

[1] " Design and Implementation of a New Multilevel Inverter Topology"
IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 59, NO. 11, NOVEMBER 2012 EhsanNajafi, Member, IEEE, and Abdul Halim Mohamed Yatim, Senior Member, IEEE

[2] "Design and SIMULATION Analysis of Seven level Cascaded grid connected inverter for PV system"
NOVATEUR PUBLICATIONS INTERNATIONAL JOURNAL OF INNOVATIONS IN ENGINEERING ESEARCH AND TECHNOLOGY [IJIERT] ISSN: 2394-3696 VOLUME 2, ISSUE 10, OCT.-2015

[3] Hani Vahedi, Student, IEEE, Kamal Al-Haddad, Fellow, IEEE "Real-Time Implementation of a Packed U-Cell Seven-Level Inverter with Low Switching Frequency Voltage Regulator"

[4] "A Simple Approach to Hardware Implementation of Seven Level Cascaded Multilevel Inverter"
International Journal of Electronics, Electrical and Computational System IJEECS, ISSN 2348-117X Volume 4, Issue 5 May 2015

[5] "Design and Implementation of Seven Level Cascaded H-Bridge Inverter Using Low frequency transformer with Single DC Source" T. Singaravelu et.al / International Journal of Engineering and Technology (IJET) ISSN : 0975-4024 Vol 5 No 3 Jun-Jul 2013.

[6] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter,"IEEE Trans. on Industrial Electronics, vol. 55, no. 7, pp. 2694-2702, 2008.

.

[7] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel Inverter Topologies for Stand-Alone PV Systems," IEEE Trans. on Industrial Electronics, vol. 55, no. 7, pp. 2703- 2712, 2008.

[8] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High- Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic NonisolatedACModule Applications," IEEE Trans. on Power Electronics, vol. 26, no. 4, pp. 1253-1260, 2011.

[9] R. A. Ahmed, S. Mekhilef, and W. P. Hew, "New multilevel inverter topology with minimum number of switches," in Proc.IEEE TENCON, pp. 1862-1867, 2010.

[10] M. R. Banaei and E. Salary, "New Multilevel Inverter with Reduction of Switches and Gate Driver," in Proc. IEEE IECC,pp. 784-789, 2010.

[11] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single- Phase Seven-Level Grid-Connected Inverter for Photovoltaic System,"IEEE Trans. on Industrial Electronics, vol. 58, no. 6, pp. 2435-2443, 2011.