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"FPGA Implementation and Comparative Analysis of an Efficient Multiplier"

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Abstract

This a new architecture for performing design-efficient multipliers using Kogge Stone Adders with Mux and Vedic Multiplication. design of an efficient 32x32 bit Vedic multiplier using the UrdhvaTriyakabhyam (UT) sutra of Vedic mathematics. Vedic mathematics is based on 16 formulae constructed by Sri Bharati Krishna Tirthaji. Multiplication operation is the most vital operation in many numeric computations.The Adder whichis used to implement the Kogge Stone Adder, which utilizes MUX, a parallel prefix form of the Carry Look Ahead Adder, and it is a widely used adder in today's industry. One of the most reliable Vedic mathematics scriptures, UrdhvaTriyakbhyam, makes a difference in the process of actual multiplication. The adder used iswidely known for designing the fastest adder possible because it produces a carry signal in O (logn) time. Offering Kogge Stone Adders using MUX offers fewer components with less path delays and better rates thanother existing Kogge Stone Adders and other Adders. In this study, we have used KSA in Mux and Vedic Multiplication. This tentative procedure estimates the performance of the proposed design in terms of logic and route delay. Experimental results show that multipliers using the kogge stone adder and Vedic Multiplication perform faster than other adders. The proposed algorithm was developed via verilog HDL. Theimplementation was done using Xilinx ise 12.3.

Keyword: Vedic multiplier, kogge stone ,Urdhva Triyakbhyam, Xilinx ISE12.3

1. Introduction

Multipliers play an important role in today's digital signal processing and various other applications. Essential design targets of multiplier include high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier are required thereby making them suitable for various VLSI implementations[1]. The multipliers are the heart of any high-speed computational devices.A configurable multiplier designed for single 32-bit multiplication operations, either single 16-bit multiplication or twin parallel16-bit multiplication. for low power consumption and high speed operation, Therefore, the proposed multiplier surpasses existing multipliers in terms of speed and power efficiency. The basic tasks associated with Digital Signal Processing systems are Multiplication, Addition and Accumulation. Additions are an integral part of a Digital, DSP or control system. Therefore, the accurate and fast operations of digital systems rely on the performance of the adders. Therefore ,improving adder performance is a major area of research in VLSI system design. Because multiplication plays an important role in digital signal processing (DSP) and various other applications, we have described the vedic multiplication algorithm for digital multiplication. With the update of technological advances, many researchers and scholars are attempting to design, develop, or implement multipliers that provide either high speed, low power consumption, regularity of layout, and thus reduction in area, or a combination thereof. multiplier. It'll be utilised to create a variety of high-speed, low-power, miniatureVLSI circuits.

2. Objectives

The main aim of this project is to implement one of the fastest adder architectures using VLSI technology, which is the Kogge-Stone adder, and validate its performance, power, and area as compared to other adder architectures, including the ripple carry adder, carry look ahead adder, and the default adder from the standard cell library.The objective is to have a fast VLSI adder that can be integrated into larger systems and improve its performance. Some of the works that implement the KSA include where an adaptive power gating is applied ona 32-bit KSA design.

3. UrdhvaTiryakbhayam

UrdhvaTiryakbhayam (UT) sutra is a Vedic multiplication formula in ancient Vedic mathematics, suitable for hexadecimal, decimal and binary multiplication. The UT algorithm has features compatible with digital systems, and the partial product and its sum are calculated in parallel, providing a simple calculation. Urdhav is a Sanskrit word meaning vertical, "Tiryagbhyam" means "diagonally" in English, and the UT vedic algorithm calculates the cross and vertical operation of the two specified numbers. This customised method improves multiplication speed and performance, based on the theory of performing partial product generation and addition at the same time.**Vedic Multiplier**

The multiplication of two numbers is done by using UrdhwaTriyakbhyam. Here first the least significant bits of the two digits are multiplied. Then the intermediate digits are cross multi-plied and added together. After this the most significant digits are multiplied. For the 16X16 bit multiplication small block of 2X2 or 4X4 or 8X8 or 16x16 or 32x32 multiplier were used in parallel to make the process easy and efficient.It generates the carry signals , and is widely considered to be fastest adder in the industry. An illustration of 4-bit kogge stone adder by taking two 4 bit inputs .Kogge stone adder is comprised with three units such as preprocessing, carry generator and post processing unit.

16x16 bit Vedic multiplier

To design 16x16 bit Vedic multiplier, we use the four 8x8 multipliers of fig – 1 and three 16-bit ripple carry adders which are modified as per the length of inputs. The 16 bit adders are designed in the same way in similar to the 8 bit adders[2].

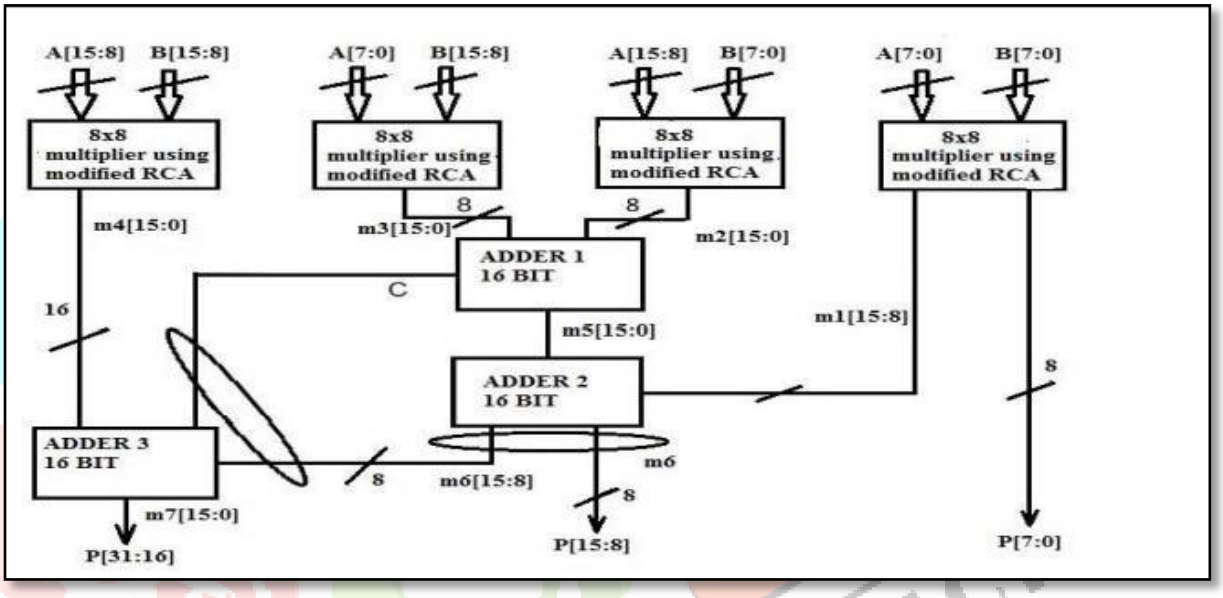

Fig.1 16x16 Bit Vedic Multiplier

32x32 Vedic multiplier

32x32 Vedic multiplier module is implemented easily by using four 16x16 Vedic multiplier modules. The outputs of 16x16 bit multipliers are added accordingly to obtain the final product. Here total two 48 bit and one 32 bit Ripple- Carry Adders are required as shown in Fig.3.1.

The 32x32bit Vedic multiplier is designed using the above 16x16 bit multipliers modules and Kogge Stone Adders(KSA) as shown in the fig-3.1. Since for higher order bit addition, the ripple carry adder consumes more powerand more area on the chip and the delay is more, it is better to use here the Kogge Stone Adder (KSA) which is efficient adder for higher order addition. The first kogge stone adder adds the outputs of second and third multipliers with the first two higher bytes of the first multiplier. The second adder performs the addition of the output of fourth multiplier and the higher bytes of the first adder.

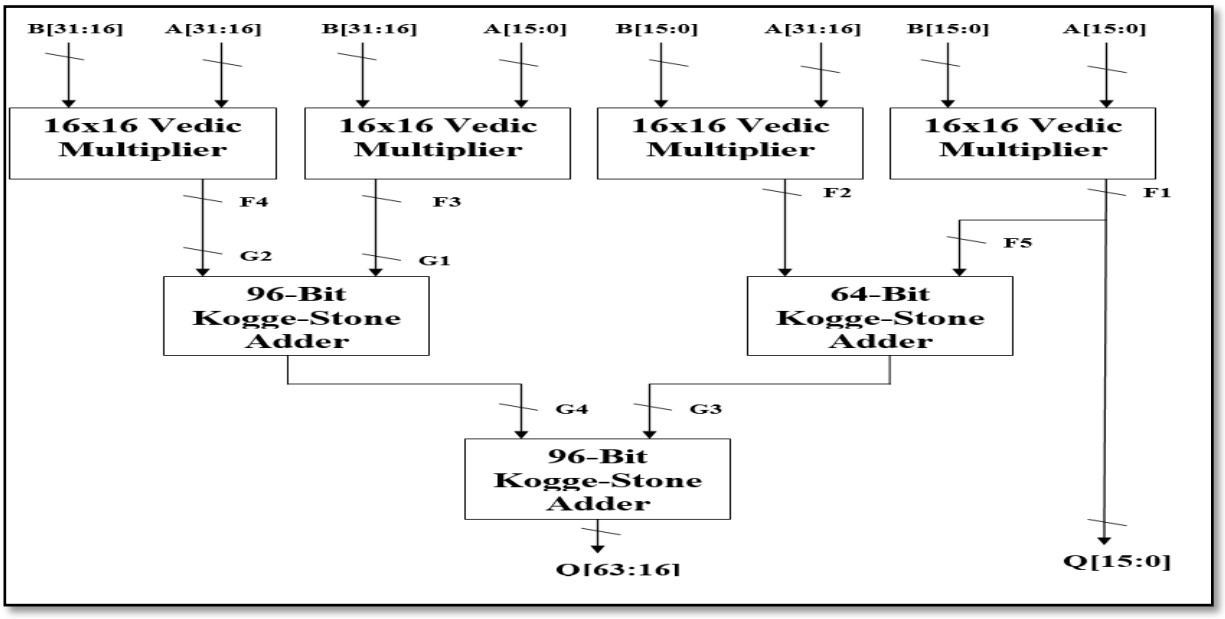

Fig.2 Block diagram of 32x32 Vedic multiplier

4. Kogge StoneAdder

Kogge-Stone Adder is a special and quick adder. It is an adder from the parallel prefixform Carry Look ahead adder. It produces a carry signal in O (logn) time and is widely known as the fastest adder in the industry. showsa diagram of 4-bit kogge stone addition with two 4-bit inputs. Kogge stone adder have three units such as preprocessing, carry generator and post processing unit.

The working procedure of KSA can be easily explained as follows.

1. Pre-processing: In this step, the Generate and Propagate signals for each pair of bits in a and b are computed. Below equations will represent this step.
   P=Ai xor Bi.G=Ai and BiCi=Gi
2. Carry Look ahead network: This block makes the KSA distinct from the other adders and is the key blockbehind its high performance. In this step intermediate carries are computed and represented by the following equations.
   P= Pi and Pprev.
   G= (Pi and Giprev) or Gi.

.Post-Processing: In this final step the sum bits are computed as given by the following equation.Si= $Si = PixorCi-1$

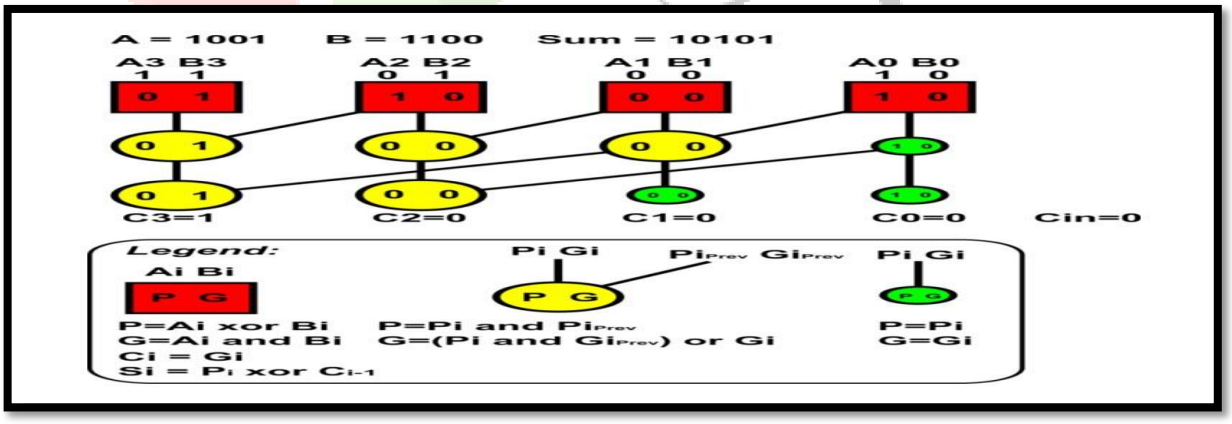

Fig.3 4-bit kogge stone

16-bit Kogge Stone adder

Implementations require more space, but less fan-out. Generates and propagates signals. This is considered the fastest adder. Due to its high performance, it is widely used in industry. This adder uses various components such as black cell gray cell generation and propagation block buffer. It is used in the calculation of the generation and propagation of the black cell signal. Gray cells are used for calculation of signal generation. Buffers are used to balance load effects.

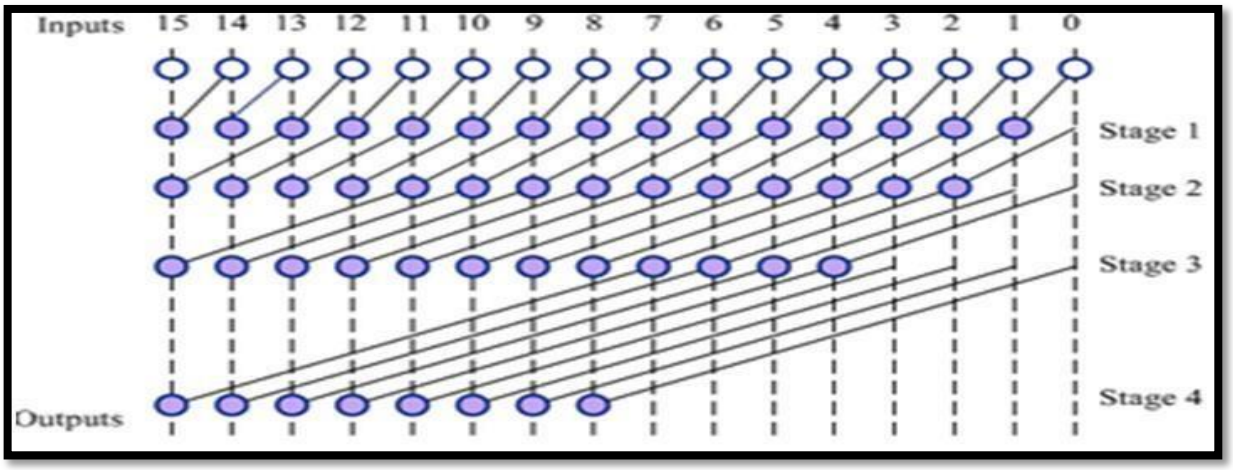

Fig.4 16 bit kogge Stone Adder

6. Result

Shows the simulation results for 32x32 bit Vedic multipliers. Let the inputs be a =4294967295 b=4294967295 i.e. the maximum value of 2^32 and then the output becomes s=18446744065119617025

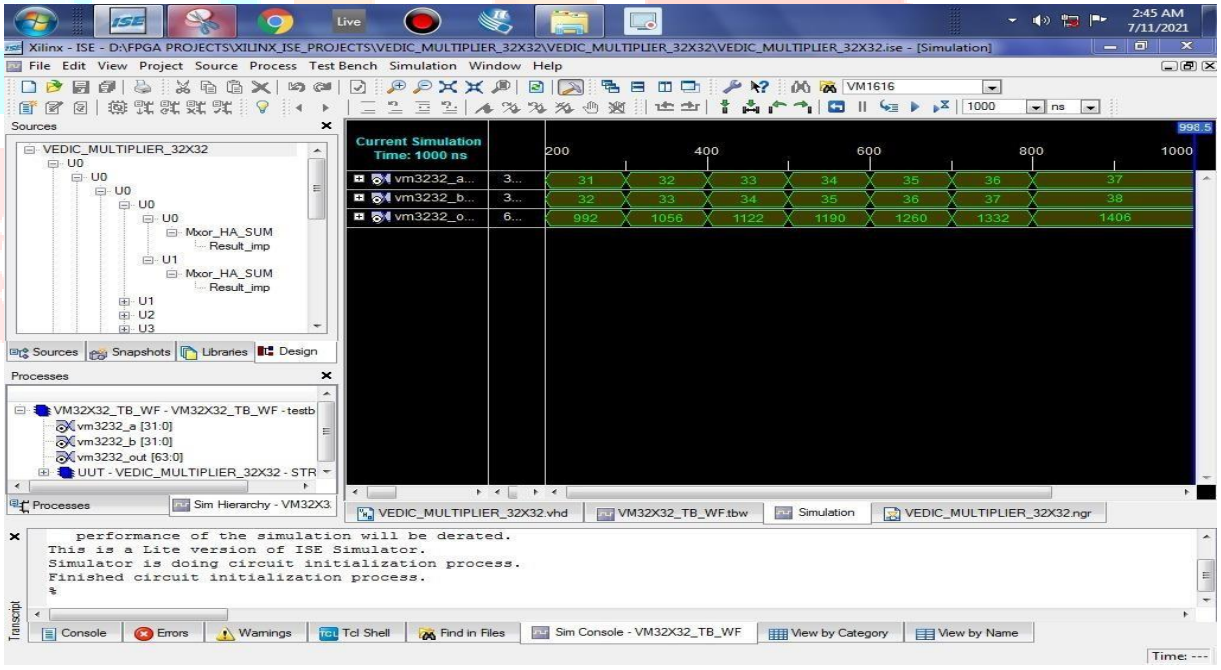

Fig.5 Simulation Results of 32x32 Bit Vedic Multiplier

RTL view of 32x32 Bit vedic multiplier with using KSA

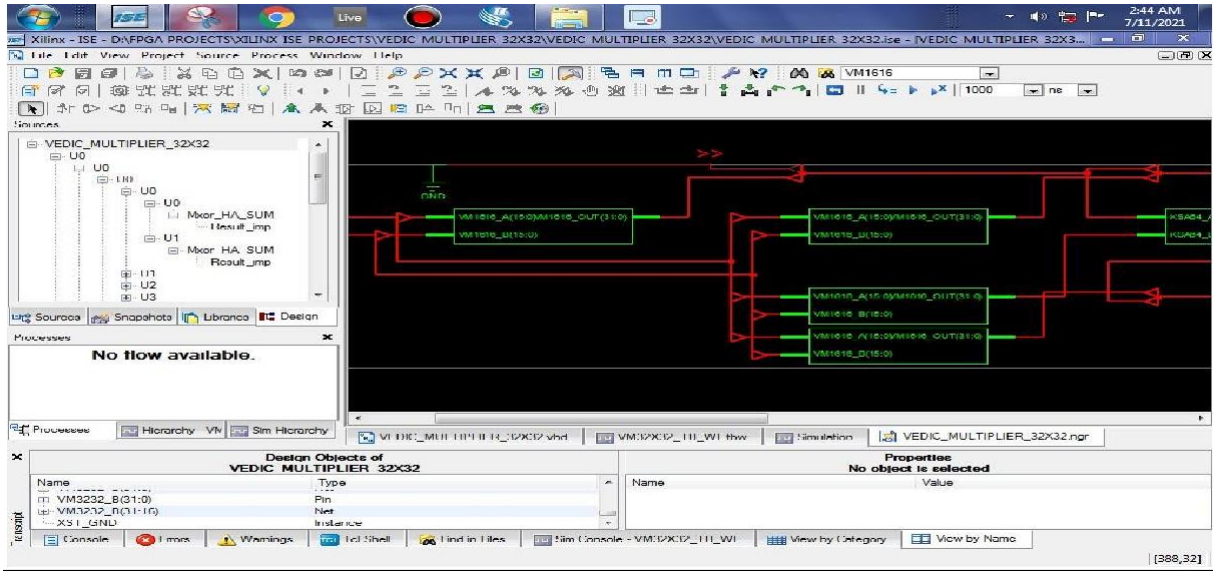

Fig.6. RTL view of 32x32 Bit vedic multiplier with using KSA

Comparision table :-

32x32 bit vedic multiplier		
Parameter	**Used**	**utilization**
No.of slices	**1774**	**12%**
No. of LUT's	**3137**	**10%**
No. of IOB	**128**	**51%**

Conclusion

Since multiplication operation is most essential operation in many arithmetic computations, it is required to havea multiplier which is efficient in terms of delay, area and the power consumption. In this project we have designed a multiplier to reduce delay and area. This project employs different adders and modifications in the existing multipliers and achieved 13.61% reduction in delay and 13.28% reduction in the area over existing multiplier.

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