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A Review On Issues With The Model-Free Time-Delay Compensation Techniques

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ABSTRACT :

The employment of digital microprocessors for the operation of grid-connected inverters has become possible as a result of recent advancements in the technology of digital signal processing. However, the phase lag that is caused by temporal delays is a barrier that prevents digital implementation from being successful. Within the context of this phase lag, the stability and robustness of the inverter controller are evaluated. Within the context of grid connections, this work provides a complete analysis of time-delay compensation techniques for both model-free (MF) and model-based (MB) inverter controllers. In most cases, proportional-integral and proportional resonance controllers are used in MF techniques. Additionally, some strategies are employed with the intention of decreasing time delay. MB control strategies and model predictive controller are summarized in this work. These techniques are among the most frequently used control techniques for MB. Along with a discussion of essential concerns pertaining to the MF and MB processes, this article provides a detailed description of several comparable strategies that have been extracted from the existing body of research with the intention of reducing delays. In this study, a theory is presented on the method that is currently being used, and a hybrid technique that combines the MF and MB procedures is proposed. This study also provides a path for more research to follow.

Keywords: Issues with Model-Free, Time Delay, Compensation Techniques, Digital Signal Processing.

1. INTRODUCTION

As a result of the growing demand for energy on a worldwide scale, conventional power systems have recently been going through a change within their regular operations that is undergoing a transformation. As a consequence of this, in order to meet the ever-increasing demand on a worldwide

scale, networks need to be liberalized so that they may include new energy sources like solar and wind. In the event that these renewable energy resources are completely harvested and used in a controlled context, they have the potential to provide a significant contribution of electricity to the primary grid. In order to fulfill this need, distributed generation (DG) is being used. This method involves the systematic interconnection of DG systems via the utilization of power electronic devices that are known as grid-connected inverters, resulting in the formation of a microgrid-like structure. The purpose of integrating individual distributed generation (DG) units is to improve the flexibility of the system, which in turn ensures the optimization, reliability, protection, integrity, and security of the system, as well as the control of power quality. New and strict standards for safe operation, power quality, and islanding protection are defined in [2]. This is due to the fact that the devices that interface with the grid face distinct problems, particularly when the circumstances are suboptimal [1]. Due to the implementation of real-time controllers that are capable of executing complex control algorithms and the emergence of power electronic devices that are able to manage high power and switch rapidly [3], these interconnection issues have recently attracted a significant amount of attention, which has prompted an increase in the amount of research that has been conducted. There are a number of problems associated with real-time controllers, some of which include latency in the control loop and delays during transitions between grid-connected and islanded modes. Time-delay is the capability of a physical system to respond to an applied force with a delayed impact [4]. This capacity is referred to as that system's ability to react. When energy or a control signal is being sent from one location to another, there is always a delay that occurs along the route. This delay is known as propagation. The length of the propagation delay is associated with both the speed of the signal that is being sent and the characteristics of the medium that it is traveling through. The design and execution of the controller are made more difficult by a prolonged delay in the digital control loop of the inverter or during the transition between grid-connected and islanded modes. This, in turn, makes frequency and voltage anomalies even more apparent. There are a variety of compensatory techniques that may be used to successfully resolve a moderate delay. Using LCL filters, grid-connected inverters may make use of a voltage, current, or direct power controller, or a combination of these controllers in a cascaded loop with either an inner-loop or outer-loop topology. Alternatively, these controllers can be employed in sequence. Inner current control has been used in a great number of research because to its ability to offer precise current tracking, sufficient control bandwidth, and quick transient response. On the other hand, the controller that is now in use is used in voltage source inverters (VSI) in order to enable the functioning of the inverter as a current amplifier within the current loop bandwidth [5]. On the other hand, the voltage controller is used in the outer-loop arrangement to provide protection against disturbances originating from the grid and input sources, therefore guaranteeing the flow of power throughout the system. In spite of this, the control bandwidth of the current controller is limited because of the time delay that occurs in the control loop, particularly in digital implementations. The use of digital microprocessors to regulate grid-connected inverters is another breakthrough that has occurred as a result of advancements in digital signal processing technology [6]. In comparison to analog control, the digital implementation provides improved dependability, more control flexibility, and the ability to reprogramme the system more quickly. There are a number of limitations associated with this

digital system, the most noteworthy of which is the phase lag that is caused by the time delay caused by the control loop. Furthermore, the implementation of additional control loops will make this delay much more apparent. Before delving into the various time-delay compensation strategies that are routinely used, it is essential to have a solid understanding of the key factors that contribute to time-delay in the control loop of a grid-connected inverter. The zero-order hold effect of digital pulse-width modulation, the amount of time required for controller computation, and the sampling and updating of voltage and current data for control purposes are the primary factors that contribute to time delays in the deployment of digital controllers. As a consequence of this, it seems to be fairly challenging to achieve excellent performance when the control loop is subjected to significant temporal delays. As a consequence of this, the controller displays a reduced control bandwidth, an increased overshoot (because to an inadequate phase margin), and a decreased transient responsiveness (due to a low-gain crossover frequency).

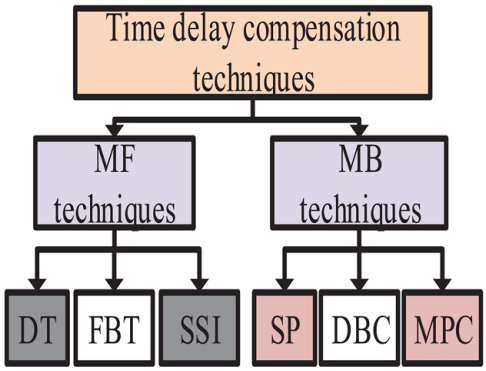

Fig 1 : Common time-delay compensation techniques for grid connected inverter

This will result in a number of negative consequences, including instability and a decrease in the controller's overall performance. These impacts may be mitigated or eliminated entirely by the use of compensators, which lessen or eliminate delays. There are a great number of time-delay compensation strategies that have been published in the literature. One way to categorize these techniques is according to whether they are model-based (MB) or model-free (MF) [6]. Figure 1 illustrates the two primary classifications. The approaches that are based on maximal likelihood (MF) are less exact but are not affected by the quality of the model. On the other hand, the methods that are based on maximum likelihood (MB) are more accurate but are greatly reliant on the accuracy of the model. Among the many different kinds of MB time-delay compensation algorithms, some of the most common ones include the Smith predictor (SP), the modified Smith predictor (MSP), the deadbeat controller (DBC), and the model predictive controller (MPC). Among the MF approaches that were used in comparison, the filter-based technique (FBT), the shifting the sampling instant (SSI) of the control variable, and the damping technique (DT) were some of the strategies that were utilized. In order to decrease the impact of time delay in the control loop of grid-connected inverters, the purpose of this research is to bring attention to the challenges that currently exist and the solutions that may be implemented to address them. Furthermore, it offers a path for additional study into reducing delays, which is a significant contribution. both the model and the deadbeat controller (DBC) are included.

2. ISSUES WITH THE MODEL-FREE

While LCL filters have benefits, they also have problems, such as power loss, making them unsuitable for grid-connected applications. Active-damping employing single-loop inverter-side control has been shown to be more stable than grid-side single-loop control when the time-delay effect is removed. When a unit delay is present in the system, grid-side single-loop control is more stable than inverter-side control. Inverter-side controls need additional active dampening to maintain stability. Researchers found that when an inverter-side single loop control is used with a small time-delay, the system is always stable (the first stable region). As time-delay increases, the system becomes unstable and then stabilizes (the second stable region if it exists).

The stability of grid or inverter-side single-loop control depends on the ratio of the inverter output filter's resonance frequency (fr) to the state variable sampling frequency (fs) due to time delay. According to [11] and [28], the critical frequency is 1 ×Td, and the resonance frequency is one-sixth of the switching frequency fs. A stable region is achieved when fr < f critical for inverter-side current control and fr > f critical for grid-side current control.

The stable area might shift owing to changes in grid impedance, resulting in a reduction in resonance frequency. A 10% change in grid impedance might lead to a 40% reduction in resonance frequency, reducing the controller's stable zone. To achieve stability in an inverter system using the previously stated compensation approach, the LCL filter should be carefully constructed to keep the resonance frequency (fr) within a stable range. However, careful design may not be feasible in practice due to grid impedance variation, which can cause a shift in the resonance frequency or cause it to change when the inverter is connected to a weak grid. Table 1 shows that using the single-loop technique for damping and time-delay compensation on both the inverter-side and grid-side does not guarantee stability, as the first stable region may become too short and narrow as the resonant frequency changes [26].

3. SUMMARY OF RESULTS

To overcome damping concerns in grid-connected inverters, widening the stable area allows for a greater range of resonance frequency fluctuation. To widen the stable zone for the inverter-side current controller, increase the critical frequency of the output filter. This may be done by reducing the time delay further. In contrast, grid-side current regulation requires reducing critical frequency via additional delays. Adding delay is not suggested for systems with quick transient responses, such as grid-connected inverters. Adding further delays will further reduce bandwidth for the existing controller. To reduce delay, additional active damping terms have been added to the current control loop (multi-loop) via capacitor current feedback [12, 15], capacitor voltage feed forward and grid voltage feed-forward.

TABLE 1 Summary of damping and compensation using single-loop techniques

	Author	Filter type	Inverter-side/grid-side control	Inner control loop	Outer control loop	Control parameter	Feedback loop	Technique
1	[10]	LCL	Grid-side	PI	N/A	*I*	GCF	SLDAT
2	[28]	LCL	Both	PI	N/A	*I*	ICF, GCF	SLDT

In contrast to prior studies, the authors used a multi-resonant component-based weighted feed-forward method with several quasi-resonant components to extract fundamental and objective harmonics. Table 2 provides an overview of research papers using this approach. Although this approach yields impressive results, it comes at a cost, reduces system dependability, and increases controller complexity, as well as topoor disturbance rejection capabilities.

TABLE 2 Summary of extending stable region techniques (multi-loop)

S/No	Authors	Filter type	Inverter-side/grid-side control	Inner control loop	Outer control loop	Control parameter	Feedback loop	Feed-forward loop	Technique
1	[13]	L	Grid-side	PR	PI	*I*, *V*	GCF	GVFF	ESRT
2	[15]	LCL	Grid-side	PR	N/A	*I*	CCF, GCF	N/A	ESRT
3	[26]	LCL	Inverter-side	PI	N/A	*I*	ICF	CVFF	ESRT
4	[33]	LCL	Inverter-side	PI	PR	*I*, *V*	ICF	CVFF	ESRT
5	[34]	LCL	Grid-side	P	N/A	*I*	GCF	GVFF	ESRT
6	[35]	LCL	Grid-side	PI	PI	*I*, *V*	ICF	GVFF	ESRT
7	[37]	LCL	Grid-side	PI	N/A	*I*	GCF	GVFF	QRCT
8	[36]	LCL	Inverter-side	PR	PI	*I*, *V*	CCF, GCF	N/A	ESRT

A cost-effective and reliable alternative to employing extra damping terms is to put an additional filter in series with the current controller. This needs no additional measurements or estimations and may vary the phase-frequency response of the LCL filter. Digital filters, including weighted filter predictors, first-order filters, second-order generalized integrators (SOGI), notch filters, low-pass filters, high-pass filters, and lead/lag filters, are used to reduce time delay in the control loop and suppress resonance frequency shift in the LCL filter, as shown in Table 3. The authors of [6] conducted a thorough examination and visual evaluation of MF approaches. They advocated using two parallel first-order filters to compensate for temporal delays and provide an ideal delay-free signal. The authors improved on [6] by using active damping to control resonance in the LCL filter and using the time-delay methods presented in [6]. This integrated technique yielded positive outcomes. The overall rating of this approach, as shown in Table 3, is quite positive. However, the success depends on precise filter parameter design and may be altered by grid inductance change or when the system is connected into a weak grid. Online parameter estimation may enhance resilience, but it might introduce disturbances into the inverter, thereby affecting current quality. Furthermore, the filter-based damping technique limits controller bandwidth, impacting dynamic performance and low-order harmonic suppression. To reduce time-delay, consider shifting the state variable sampling time to the PWM duty cycle and updating instants. This approach was used, resulting in reduced computational time delay. However, asynchronous sampling may cause undesired harmonics and aliasing effects in the controller [6]. To avoid aliasing, consider updating the PWM reference soon after the calculation is completed. This may maintain the synchronous sampling process.

TABLE 3 Summary of filter-based compensation techniques

S/No	Author	Filter type	Inverter-side/grid-side control	Inner control loop	Outer control loop	Control parameter	Feedback loop	Feed-forward loop	Technique
1	[6]	LCL	Inverter-side	PR	N/A	*I*	ICF	SLDT	FBT
2	[14]	LCL	Grid-side	PR	N/A	*I*	GCF, CCF	N/A	FBT
3	[17]	LCL	Inverter-side	PR	PI	*I*, *V*	CCF, GVF	N/A	FBT
4	[18]	LCL	Grid-side	PI	PI	*I*, *V*	GCF	N/A	FBT
5	[19]	LCL	Inverter-side	PI	PI	*I*, *V*	CCF, GVF	N/A	FBT
6	[38]	L	Grid-side	N/A	N/A	*I*, *V*	GCF	N/A	WFP
7	[44]	L	Grid-side	N/A	N/A	*I*	GCF	N/A	WFP
8	[41]	LCL	Grid-side	PI	N/A	*I*	GCF	CVF-AD	FBT
9	[40]	LCL	Grid-side	PR	N/A	*I*, *V*	GCF	N/A	FBT
10	[42]	L	Grid-side	DBC	N/A	*I*	GCF	N/A	FBT

This strategy was used in, which prevented the aliasing issue. This approach performs well when the controller's computation time is less than 0.25Ts, where Ts represents the sampling period. However, this approach is primarily useful for high-power applications with low switching and sampling frequencies. According to [21], relocating the sample instant to the center of the sampling period leads to harmonic rejection while introducing a one-period delay. Double-sampling the control variable and updating the PWM may minimize the one-sampling delay by half. This strategy was implemented, resulting in decreased time but increased processing and complexity. The authors evaluated and analyzed several carrier types used in multi-sampled PWM, resulting in considerable time-delay reductions. Research suggests that multi-sampling the control variable and updating the PWM may reduce the half-sampling delay caused by double sampling and double-updating techniques for particular fractions, without incurring extra costs.

This approach has received significant attention as a possible option for decreasing phaselag caused by time delays and overcoming the bandwidth constraint associated with digital controllers. This technique has been employed, and more recently. The multi-sampling and updating approach may introduce high-frequency disturbances, such as voltage ripples, into the feedback loop. As a result, there is a requirement for extra high frequency cancelation. One of the most easy cancellation methods is to employ an antialiasing filter. However, this simple method reduces the controller's phase margin, limiting the benefits of MSMU approaches. Researchers developed a ripple removal strategy that preserves the good phase margin associated with the MSMU technique. The authors employed a repeating ripple estimation technique to reduce noise from the sampled error signal. The issue of this strategy is that the PI controller has limitations in terms of disturbance ejection and costs for the FPGA. Further testing is needed with additional potential controller types. In [48], the author used the quadruple-sampling and updating approach (QSQU) for a single-phase active filter. Three kinds of current controllers were used: the P-controller, the DC controller, and the modified DBC. This experiment yielded positive results, however it is recommended to use quadruple sampling to inverter systems, particularly grid-connected ones. The technique's downside is that it was built on two FPGAs, which is costly. Therefore, there is a need to study the potential of implementing it on a micro-controller, which is simpler to manage. The authors performed research on MSMU carrier-based PWM for multi-level active shunt power filters.

However, the study only evaluated the signals at the peak and valley of each triangle carrier, which limited the dynamic of the multi-level converter. The authors of [24] did a full investigation of the multi-sampling approach for a high-power grid-connected inverter with an LCL filter. However, this study did not evaluate the previously reported limitations of MSMU.

The authors presented a technique for implementing MSMU with a minimal sampling interval, which they claim prevents sampling the current ripple induced by switching and destroying the voltage-second balance during modulation. The research found that using a single-phase L-type filter with a PR current controller resulted in difficult gain adjustment and a lack of resilience when several disturbances were present. This strategy should be tested with several kinds of controllers using an LCL filter. Table 4 presents an overview of the strategies.

TABLE 4 Summary of different sampling and updating techniques

S/No	Author	Filter type	Inverter-side/grid-side control	Inner control loop	Outer control loop	Control parameter	Feedback loop	Feed-forward loop	Techniques
1	[11]	LCL	Both	PI	N/A	I	GCF, ICF	N/A	SSITUT
2	[49]	L	Grid-side	PR	N/A	I	GCF	N/A	MSMU
3	[12]	LCL	Grid-side	PI	N/A	I	CCF, GCF	GVFF	MSMU
4	[22]	LCL	Inverter-side	N/A	QPI	I, V	ICF	N/A	DSDU
5	[24]	LCL	Inverter-side	PI	PI	I, V	ICF	N/A	MSMU
6	[43]	LCL	Inverter-side	PR, PI	N/A	I	ICF	GVFF	UIAC
7	[51]	LCL	Inverter-side	N/A	PI	I	ICF	N/A	SSITUT
8	[45]	L	Grid-side	PI	N/A	I	GCF	GVFF	SSITUT

This study reviews several MF time-delay compensation approaches that use cascaded conventional proportional controllers (P), proportional integrator controllers (PI), or proportional resonant controllers (PR). Figure 2 illustrates the use of either an inner-loop or outer-loop controller, or a combination of both. Although satisfactory performance has been reported, the controllers used have shown reduced accuracy and stability when handling time-varying signals. They also have poor disturbance rejection ability, slow response to abrupt changes in grid impedance variation, and complications in tuning for sinusoidal signals. Several changes to the classic controller have been suggested, including capacitor voltage feed-forward, grid voltage feed-forward, and multiple-state variable feedback. Modifications may increase controller bandwidth, albeit at the price of stability margin. To improve time-delay mitigation methods, more robust controllers with faster response, wider stable region, zero steady-state error, better time-delay mitigation ability, disturbance rejection, and high adaptability to the weak grid are needed. Simplicity and cost implications should also be considered.

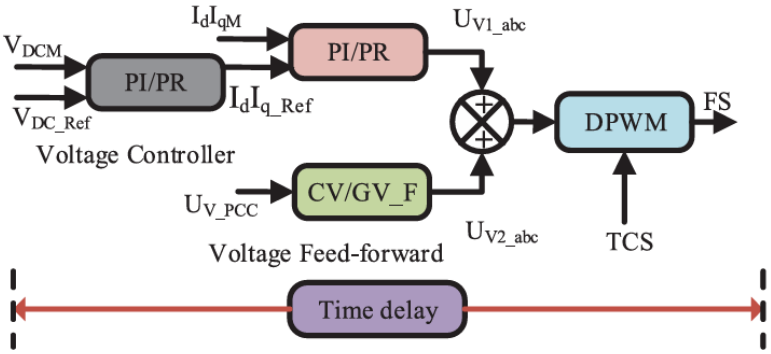

Fig 2 : Common Block diagram of a conventional PI/PR controllers with feed forward.

In micro-grids with linked inverters, MF approaches utilizing PI or PR controllers may not provide stability in the face of many disturbances, particularly when there is time delay and grid impedance per turbaton. This impact creates a resonance frequency shift in the output filter, resulting in a smaller stable zone for the controller. To achieve a broader stable zone and quicker reactions, using these strategies requires a more robust controller.

4. CONCLUSIONS

This article provides a concise overview of the analytical work that has been done on grid-connected inverter control loops that use time-delay compensation techniques. Despite problems with system stability in inverter-side and grid-side topologies, MF's average performance and relative simplicity made it the preferred method in this investigation. Each controller-dependent system model (MF and MB) is analyzed in this study. What follows is a comparison of the models. Connected to an unstable grid or otherwise disrupted, these controllers could not function properly. Many approaches were proposed to mitigate time-delay and enhance system stability with a reduced number of sensors and complexity; however, these controllers do not necessarily possess resilience. The first methods used to balance time-delays in conventional PID controllers were the Smith predictor and the modified Smith predictor, after the evaluation of model-based techniques. This resulted from the first use of the Smith predictor. Because grid-connected inverters' controllers lack the ability to handle time-varying signals and provide adequate disturbance rejection, this method is not as useful for them. On the other hand, DBC has become popular because to its rapid current monitoring, zero steady-state error, time-delay compensation, and rejection of disturbances. Based on whether the time delay impact is taken into account during controller design, this method is determined to be divided into two categories in this article. The assumption of continuous DC-link and grid power was made by several time delay investigations. The controller's design omitted the outer loop.

In order to point researchers in the right path, this study suggests combining DBC with some of the MF time-delay compensation methods: Application of DBC in the inner loop and MPC in the outer loop, as well as application of fuzzy logic in the outer loop utilizing QSQU. The stability of the system when using an LCL output filter can be guaranteed by these hybrid controllers, which have a low total harmonic distortion, a good output current, a fast transient and dynamic response, and a low control-loop

time-delay. According to the literature review, these controllers are not present.

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