IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Low Power Linear Feedback Shift Register

[1]Lingala Akhil Reddy, [2]Gomasa Ramesh

[1]M.Tech, Department of Electronics & Communication Engineering, [2]M.Tech, Department of Civil Engineering

[1,2]Warangal, Telangana, India.

Abstract: Built-in Self-Test (BIST) is becoming increasingly essential in today's IC designs for memory, which is the most critical component of the System on Chip. BIST is a method for circuit design that enables it to self-test. By enabling the use of low-cost test equipment at all phases of manufacturing, the method may save time and money when compared to an externally applied test. Because of the randomization characteristics of Linear Feedback Shift Registers, this needs relatively minimal hardware (LFSRs). Linear Feedback Shift Registers have been used to create test patterns for a long time (LFSR). The feedback taps on LFSRs, which are a sequence of flip-flops linked in series, are defined by the generating polynomial. The seed value is fed into the outputs of the flip-flops. The only input needed to create a random sequence is an external clock, and each clock pulse may result in a different pattern at the flip-flops' output. The random sequence at the output of the flip-flops may be utilized as a test pattern. The number of flip-flop outputs needed by the circuit under test must match the number of inputs required by the LFSR. This test pattern is used to verify that the required fault coverage is obtained on the circuit under test. A novel low-power pattern generating method is implemented using a modified Linear Feedback Shift Register standard benchmark circuit. Using an industry standard Xilinx tool called Power analyzer or Cadence, the circuit's instantaneous and peak power consumption is examined, and it is demonstrated that the new low power method uses considerably less power than the traditional pattern for the same fault coverage. The aim of the research is to test the multipliers using a Low Power Linear Feedback Shift Resister (LFSR), which is better suited to VLSI circuit testing built-in self-test (BIST) structures. Random values are needed for testing every circuit that is developed. To do so, we create random generators that produce random values. BIST is a design for testability (DFT) method for testing that makes use of built-in hardware characteristics. Because testing is integrated into the hardware, it is quicker and more efficient. The suggested test pattern generator minimizes switching activity between test patterns, resulting in a low-cost, high-speed solution.

Keywords: LFSR, BIST, LTLFSR, TPC, TPS, Test Patterns.

I. INTRODUCTION

Testing is carried out throughout the manufacturing of integrated circuits to detect faulty chips. This is critical for the delivery of high-quality goods. In order to enhance the manufacturing process, testing is often carried out to determine the cause of a chip failure. In order to repair a system, testing is done to identify components that need to be replaced. Applying a suitable set of input patterns (LFSR) to a digital circuit and verifying for the right outputs is what testing a digital circuit entail. Traditionally, the test is carried out by an external tester. Built-in self-test (BIST) methods, on the other hand, have been created in which part of the tester capabilities are integrated on the chip, allowing it to test itself. BIST has many well-known benefits. It does away with the necessity for costly test equipment. Because the chips can test themselves simultaneously, it allows for quick detection of faulty components in a system. It also enables at-speed testing, which involves evaluating the chip at its regular working clock rate, which is critical for identifying timing errors. Despite these benefits, BIST has found little usage in industry due to its high overhead in terms of space and performance, as well as the absence of BIST design tools. This dissertation covers these issues. Because BIST is becoming more popular, the research presented in this dissertation is timely. External tests are unable to keep up with the growing pin count, operation speed, and complexity of ICs. These issues are addressed by BIST. For BIST, pseudo-random testing is appealing. To apply pseudo-random patterns to the CUT, a LFSR may be utilized. This project offers a new low-power LP-LFSR based on some fresh findings regarding a standard LFSR's output sequence. The power in BIST implementation is reduced by using a low-power LFSR method. This paper presents an LP-LFSR design and testing of high-speed multipliers utilizing a low-power linear feedback shift register. This is to check if the multipliers are functioning or not using a Low Power Linear Feedback Shift Resister (LP-LFSR), which is better suited to Build in Self-Test (BIST) structures used in VLSI circuit testing. For every circuit that is built, random values are required for testing. To do this, we build random generators that produce random values. Traditional Linear Feedback Shift Registers have long been used to generate test patterns (LFSR). The generating polynomial defines the feedback taps on LFSRs, which are a set of flip-flops linked in series. An external clock is the sole input needed to create a random sequence, and each clock pulse may produce a unique pattern at the flip-flops' output.

The power used by the chip under test is a measure of the logic within the chip's switching activity, which is mainly determined by the randomness of the applied input stimuli. Reduced correlation between the consecutive vectors of the applied stimulus into the circuit under test may cause the device to use much more power than is allocated. For Test Pattern Generating (TPG), a novel low-power pattern generation method is used to reduce power consumption during testing. During testing in normal mode, the correlations between successive patterns are greater. The LP-LFSR method is based on the idea of minimizing transitions in the test pattern produced by traditional LFSR. By strengthening the correlation between the consecutive bits, the transition is sped up. Two 8-bit LFSRs and two 8-bit LP-LFSRs are used in this array multiplier test. Low Power Linear Feedback Shift Resister (LP-LFSR), which is better suited for testing VLSI circuits using Built in Self-Test (BIST) architecture. Cadence is used to both simulate and

generate the LP-LFSR architecture. Testing is quicker and more efficient since it is integrated into the hardware. The LP-LFSR test pattern generator minimizes switching activity across test patterns to the bare minimum, resulting in a low-cost, high-speed solution. For BIST, we suggested the creation of a test pattern. In fact, the power consumption of a simple LFSR is very significant. This article proposes a technique for reducing the power consumption of current low-power Linear Feedback Shift Registers. The Automatic test pattern creation on Built in Self-Test is explained in this article. Random test vectors can be produced in a standard LFSR, but the power consumption is significant due to the large number of transitions. To avoid this common LFSR disadvantage, a single LP-LFSR is employed in this pattern. The number of transitions is decreased, but the current bit is altered even one bit when compared to the prior pattern. This is a problem for which our approach provides a solution. Only OBM is used in this study (one bit Modifier). The creation of various patterns using a Moebius counter and a one-bit change counter is shown in this project. Another benefit is that it may be used for both Test-per-clock and Test-per-scan systems. Different A 7.5 percent cost is imposed by a single input modification that reduces the test power. It extends the fault coverage while reducing the length.

II. LITERATURE REVIEW

Author	Year	Research Findings
Singh	2009	This article presents a low-power linear feedback shift register (LFSR) for test pattern generation (TPG) to reduce power consumption during testing. During normal mode, the correlations between successive patterns are greater than during testing mode. The suggested method is based on the idea of minimizing transitions in the test pattern produced by LFSR. By increasing the correlation between consecutive bits, the transition is shortened. According to the simulation results, the testing power used by the interrupt controller benchmark circuit is decreased by 46% when compared to the power spent by a standard LFSR during testing.
Hamid	1998	In today's electronics sector, low power has become a major topic. Because of the requirement for low power, power dissipation has become just as essential as performance and area. In this respect, Lowy's (1996) article is very intriguing. The author describes a parallel architecture of linear feedback shift registers (LFSRs) and sequence generators that dissipate less power than traditional LFSRs. It is feasible to create significantly better sequences from Lowy's LFSRs structure using our methods. Furthermore, in our instance, power dissipation is constant regardless of the number of stages in the LFSRs.
Sasi	2017	Memristors are being explored as a viable replacement to CMOS technology's scalability limitations. This article presents a quick, compact, and low-power hybrid CMOS-memristor based Linear Feedback Shift Register (LFSR) architecture. As an example, a 4-bit LFSR was constructed utilizing the Memristor Ratioed Logic (MRL) architecture using 64 CMOS devices and 64 memristors. the suggested architecture is more efficient in terms of area. The simulation results show that the design is functional. In contrast to CMOS-based design, this method is acceptable in terms of speed. Furthermore, compared to a CMOS-based method, the suggested architecture offers a substantial power saving of over 66 percent.
Praveen	2017	LFSR are widely utilized in BIST for producing test vectors. The primary goal of this article is to develop and build a power-efficient LFSR for low-power applications utilizing reversible logic. The reversible D Flip Flop is implemented using the Pareek Gate (DFF) & to create an 8-bit reversible LFSR (DFG). The suggested method to constructing reversible LFSR lowers the power by 10% when compared to traditional design, according to the study. As a result, the suggested architecture may be utilized to create BISTs for low-power applications.
Baskar	2018	In medicine and biologically based healthcare problems, biomedical applications play a significant role. The biological procedure that uses physiological characteristics such as body glucose, pressure, heart rate, blood oxygen saturation, blood sugar level, blood pressure, and perspiration rate to identify and diagnose illnesses. The biomedical concept is used to identify issues linked with impairments by utilizing different physiological indicators. The recorded characteristics of impairments are forwarded to healthcare facilities for diagnosis, however one of the major problems in the biomedical system is data transmission quality. As a result, we provide a two-dimensional LFSR based CRC technique for error detection in biological data in this article. The suggested approach encrypts and decodes data while transmitting it, reducing error activities to a bare minimum. The rehabilitation of the individual may be given in an efficient way based on the safe transaction. Furthermore, the system's efficiency is assessed using experimental findings and conversations, which aid in the monitoring of the disabled patient's health.

Aloisi	2008	In this article, we will propose a method for lowering the power consumption of the widely used linear feedback shift register. Depending on the technical features of the used gates, the proposed system is based on the gated clock design approach and could save a lot of energy. In addition, the analytical condition for reducing the power of the gated-clock circuit has been discovered. Several transistor-level SPECTRE simulations using AMS' 0.35-mum digital standard cells technology were used to verify the theoretical analysis in the CADENCE environment. In comparison to theoretical derivations, simulation results showed a power decrease of approximately 10% and a mean inaccuracy of about 3%.
Mehri	2015	Future nanoelectronics computer systems will rely heavily on memristors, which are a developing history-dependent nanoscale sized element. Several pure and hybrid memristor-based implementation methods have been proposed in recent years. One of the most important topics for memristor-based logic implementation is material implication logic. This paper develops a memristor-based linear feedback shift register based on material implication logic. It is made up of 8 memristors, which take up a lot less space than traditional CMOS-based counterparts. In addition, to generate a 4-bit integer, the suggested memristor-based LFSR circuit requires 55 computing steps.
Sabir	2017	An efficient pattern generator is needed in today's high-speed, high-tech IC designs to minimize test power consumption without sacrificing overall system performance. BIST (Built-in Self-Test) is a key module and a promising DFT technique. The Linear Feedback Shift Register (LFSR) is the most often used pattern generator in BIST due to its low area overhead and excellent pseudo random characteristics. The BS-LFSR is an Ex-OR with non-zero selective seed that produces a single input change BS LFSR. The test vectors generated significantly enhance the correlation between test sequences. We've put it to the test and compared it to traditional methods, and the results are extremely promising. This method reduces transition activity, improves fault coverage, and reduces dynamic power dissipation.
Li, Rui,	2001	This article proposes a novel low-power BIST technique based on changing the structure of the LFSR. The effectiveness of the vectors drops significantly as the test continues in pseudo-random test mode. By changing the topology of the LFSR, the suggested method ignores nondefecting vectors during test mode, resulting in reduced power usage. It's worth noting that changing the structure of the LFSR is quick and has no effect on fault coverage.
Dharmendra	2017	The major difficulties for researchers in VLSI are to decrease the power dissipation by devices. To satisfy the specified output, the authors suggest a modified version of the Linear Feedback Shift Register in this article. The clock signal from the flip flop to design test pattern generator may be deactivated during testing power to minimize power consumption. The LFSR pseudo-random test pattern generator is used in the testing of ASIC chips, and it is utilized to create the required pattern generator's random sequences. This article will aid in the minimization of the ASIC's extra test inputs. The test pattern is designed in such a manner that component needs are minimized.

III. METHODOLOGY

Evolution of Testing

Testing of digital systems used to be divided into three stages. then on integrated circuits (ICs) as electronics technology advanced to greater degrees of integration. Though the difficulties with IC testing were not dissimilar to those with PCBs, the goal of testing had shifted to discarding bad units rather than identifying and replacing problematic components. The difficulties were relatively easy. The devices' internal nodes were readily manipulated and seen from the devices' main inputs and outputs. The circuit functions' simplicity allowed for extensive testing. More sophisticated systems were built using simple, well-tested components. The gate/pin ratios grew quickly as LSI and VLSI became the dominant technology, significantly decreasing the controllability and observability of internal nodes. As a result, the testing issues worsened by VLSI circuits may be summarized as follows:

Higher testing expenses, which are determined by test duration and therefore circuit complexity.

An increase in the time required to generate and verify test patterns.

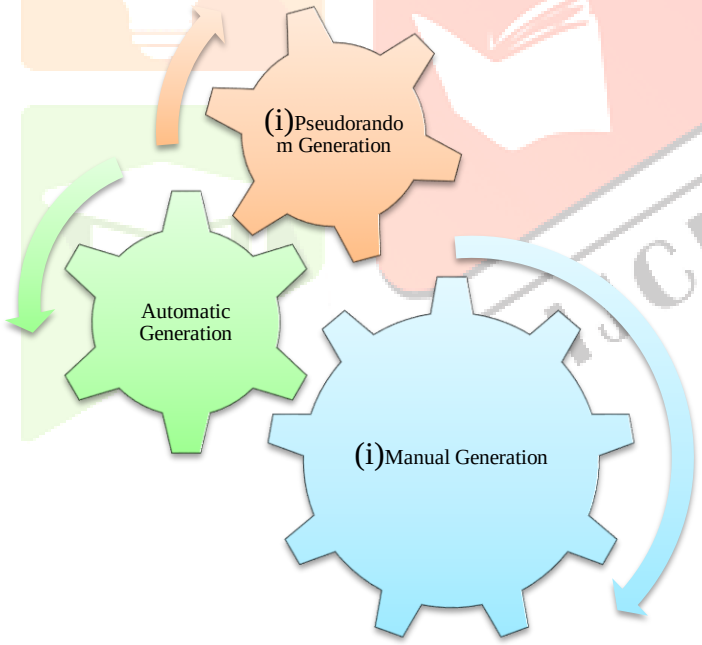
The amount of test data has increased.

Rapid advancements in VLSI technology, as well as increased usage of ASICs, have exacerbated these issues. ASIC applications have certain characteristics that make VLSI testing even more difficult. ASIC designs often have a low design time overhead, and therefore have a short product lifespan. As a result, extensive attempts to develop effective testing methods may depreciate the market value owing to time constraints. Because ASICs are application-specific by design, they have a limited manufacturing volume that cannot compensate for high test costs. The one-of-a-kind nature of ASICs necessitates one-of-a-kind testing methods for each application. Before manufacturing, verify that the circuit is operationally accurate and free of design flaws. To verify that the gadget is free of fabrication flaws once it has been made. To find the cause of a problem inside an integrated circuit. To identify a defective component or link across the whole system.

Functional and Structural Testing

Before LP-LFSR, digital systems were tested to ensure that they functioned as intended, for example, a multiplier would be checked to see whether it multiplied and so on. Functional testing, as defined by applying a sequence of relevant inputs to verify for proper output responses. in terms of device functioning, is a testing philosophy. Although this approach provides a solid understanding of circuit functioning, identify specific problems in circuits in order to validate their detection in the absence of a clear fault model. outputs that are visible as is clear, structural testing is reliant on the fault models supplied for the Circuit under Test (CUT), and any result obtained in this manner is untrustworthy unless the fault models used are well explained.

Test Pattern Generation



(i)Manual generation	Automatic (Algorithmic) generation	(i)Pseudorandom generation
•Depending on the extent of the original circuit or system designer's thorough understanding of the system, manual test pattern creation may be employed. The deterministic test set comprises of test patterns that will give the propagation of particular node failures and/or for certain functional conditions. The benefit of this method is that it allows for the quick identification of a more effective smaller deterministic set, but it may take a long time to analyse.	•As the gate count in VLSI systems grows quickly, automatic (algorithmic) test pattern creation has become the most commonly used method for test pattern generation. Dedicated ATPG programmes are often used for this job, and they operate on predefined fault models.	•The deterministic pattern generating methods discussed in the previous two sections are based on precisely specifying input test vectors that allow the identification of particular defects inside the circuit under test. The benefit of deterministic testing is that they offer a small test set that is focused on detecting the specified fault list. The apparent downside is the high computing cost and complexity. Fully exhaustive testing, on the other hand, requires virtually little complexity and has no cost in terms of computation when determining the test set.

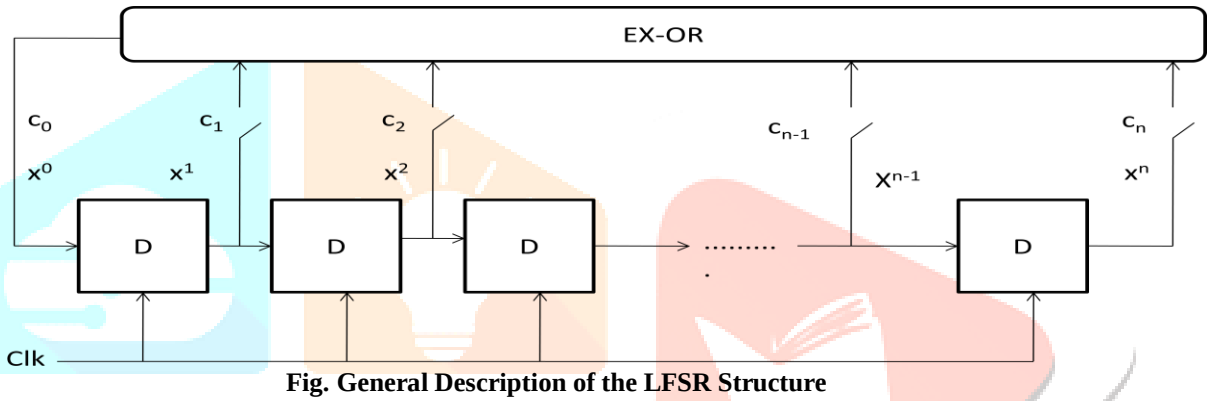
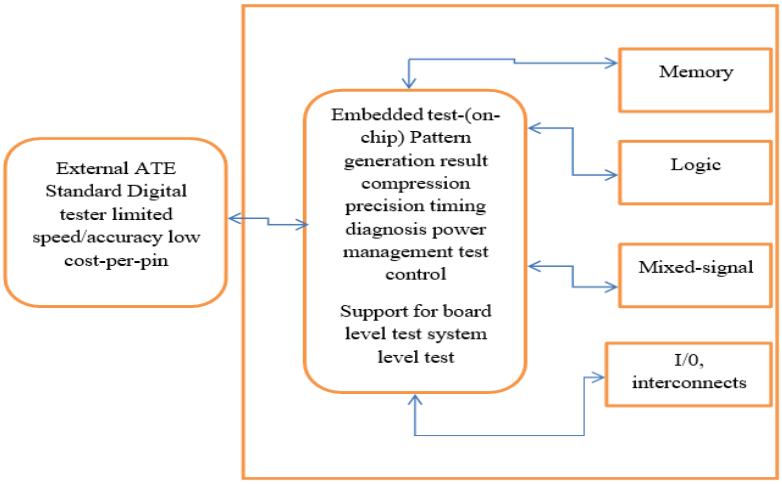


Fig. General Description of the LFSR Structure

The sigma operator represents modulo 2 additions rather than base 10 adds. Despite the fact that infinity limits the summation, it will be reduced to the length of the LFSR since anything beyond that is intuitively zero. As a prologue to the rest of the article, a well-applied approach in coding theory is to characterize a binary sequence as a polynomial, where the binary values represent the polynomial coefficients and the powers polynomial variables give the time or sequencing information.
The aim behind the LP-LFSR technique is to reduce transitions in the test pattern generated by conventional LFSR. By strengthening the correlation between the consecutive bits, the transition is sped up. Two 8-bit LFSRs and two 8-bit LP-LFSRs are used in this array multiplier test. LP-LFSR, which is better suited for testing VLSI circuits using Built in Self-Test (BIST) architecture.

IV. TESTS

SOC testing is best regarded as a set of tests performed in an iterative process. A test technique is shown in Figure 3.1. Depending on the device's complexity, a flat or hierarchical method may be employed. As the device's complexity grows, it's more common to suggest testing specific components using Scan and/or BIST rather than evaluating the whole design with a flat approach. The flat method entails flattening the whole design's net list, applying stimulation to the design's main inputs, and testing outcomes at the design's primary outputs.

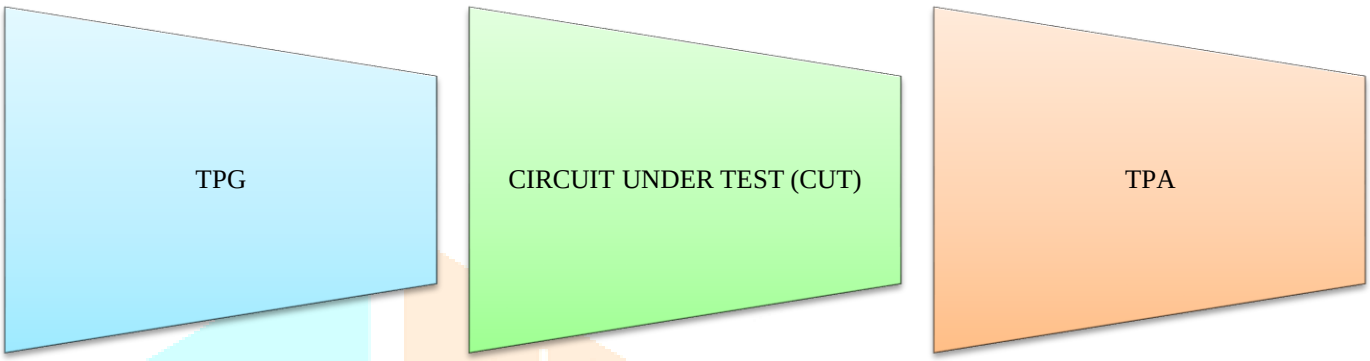


The ability to identify and fix the issue piecewise is one benefit of evaluating the SOC using a hierarchical method. The outputs of a specific macro are examined and validated when a test input stimulus is applied. Scan and Built-In-Self tests are examples of traditional test methods. Most SOC designs nowadays, on the other hand, use an embedded test strategy. Embedded testing is a

logical progression from the two methods previously described, namely external ATE and DFT. A combination of extremely costly low/high speed testers with variable bandwidth is required for an external ATE method. These testers may be set up to do function-specific tests. Embedded test incorporates the external ATE's high-speed and high-bandwidth parts directly into the IC, and this may be regarded the primary goal of the embedded test method. Test pattern development may be generated, integrated, analyzed, and verified using automatic test pattern generation/Fault Simulation technologies. One of the main advantages of embedded testing is the production of on-chip test data, which lowers the number of external patterns and may be modified according to the IP block type in the SOC. ATE data logging is reduced thanks to on-chip and data compression. True at speed testing may be achieved via on-chip timing generation.

Built-In Self-Test

Integrated circuit (IC) testing is critical for ensuring high levels of quality in product functioning in both commercial and privately manufactured devices. Testing has an effect on the manufacturing industry as well as those engaged in design. Given the breadth of design participation, determining the optimal method for attaining high levels of confidence in IC functioning is a significant issue. The goal to achieve a high degree of quality must be balanced against the expense and time required in the process.



In many respects, BIST is advantageous. For starters, it may lessen reliance on third-party Automatic Test Equipment (ATE). This has an effect on the cost/time constraint since the ATE is used less in the present design and may be employed elsewhere or on other devices. BIST can also do system testing of the Circuit Under Test at a high pace (CUT). This is critical for testing quality. Furthermore, BIST can overcome packaging-related pin restrictions, make effective use of available additional chip space, and offer more comprehensive information about the defects present. BIST is well-motivated by all of these advantages.

BIST Pattern Generation Using LFSR

The LFSR is the primary component of BIST, and it can produce random numbers that are utilized to detect physical defects in integrated circuits (IC). A sequential shift register with combinational logic is known as a linear feedback shift register. First and foremost, let us construct an LFSR. Cycle through a series of binary values pseudo-randomly. LFSRs may be implemented in two ways: Internal and external feedback are both important. The way feedback is applied differs across different methods. Taps refer to all of the flip-flops that feed an XOR gate. The patterns produced by the LFSR are determined by these taps, which define the LFSR's characteristic polynomial. The primary advantage of LFSR circuits is that they run through a defined sequence of states when clocked repeatedly, which has a number of explicit characteristics of randomness and can therefore be utilized as a TPG in a BIST scheme. (2n – 1) is the maximum number of such states, where n is the length of the LFSR (no. of flip-flops). However, the length of the series is determined by the polynomial chosen and, in certain instances, the starting state.

These two LFSR settings have a direct impact on the quality of the resultant test and therefore play a significant role in TPG. Let's have a look at a 3-bit LFSR. The LFSR's starting state is (001). After 7 rounds, the starting state is repeated. The identical sequence will be repeated in the following cycles. If you look at the sequence closely, you'll see that the recurrence period is 7 or 23 1. Except for all zeros, the recurrence cycle includes all conceivable combinations (000). Many other types of LFSR may be built, but the most important for BIST is the so-called maximum length LFSR (ML-LFSR). We can make a PRBS generator using an ML-LFSR. Remember that we can create virtually any binary pattern we desire using this method. In this section, we'll go further into the characteristic polynomial and the patterns it produces.

Theory of LFSR Taps

It's clear that an m-sequence will not be produced by all combinations of tap choices. As a consequence, a theory for identifying the tap sites that may create a m sequence, as well as requirements for the LFSR to generate all possible 2n -1 states, must be established.

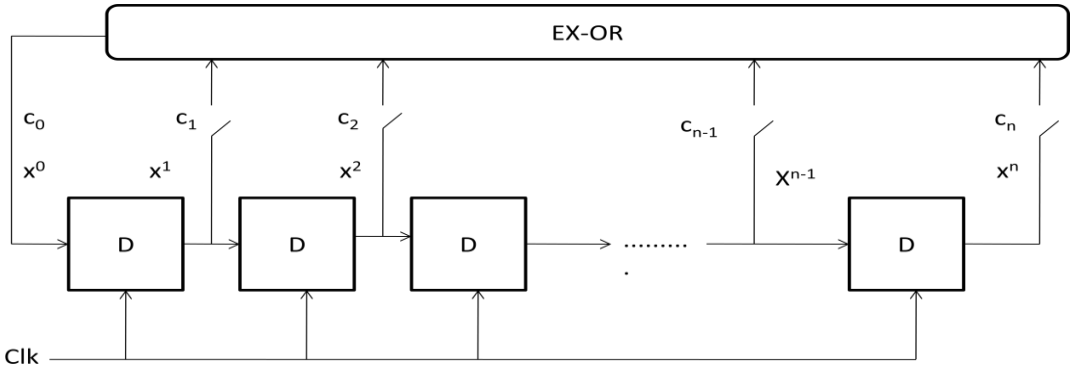


Fig. General Description of the LFSR Structure

Instead of base 10 additions, the sigma operator represents modulo 2 additions. Despite the fact that the summation is proven to be limited by infinity, it will be trimmed to the length of the LFSR since anything beyond that is intuitively zero. To set the stage for the remainder of the discussion, a common coding theory technique is to represent a binary sequence as a polynomial, with the binary values representing the data. The time or sequencing information is represented by polynomial coefficients and powers polynomial variables.

Primitive Polynomials

An LFSR is delightfully tiny and quick when compared to the typical logic for a binary increment. The cost is the difficulty of determining how many times the register has been moved after the fact. The discrete logarithm issue is a problem in number theory and cryptography. The discrete logarithm is used in cryptography to favor architectures where the computation is challenging since it is part of the decryption process.

The essential idea underlying this application is that just the increment function in a counting instrument has to be quick. Other online activities, such as comparison or general addition, are not required. Because the manipulation of the counts is done offline, it is possible to employ more costly computations than the quick increment. (Unfortunately, the otherwise attractive size of 32 bits has both issues!)

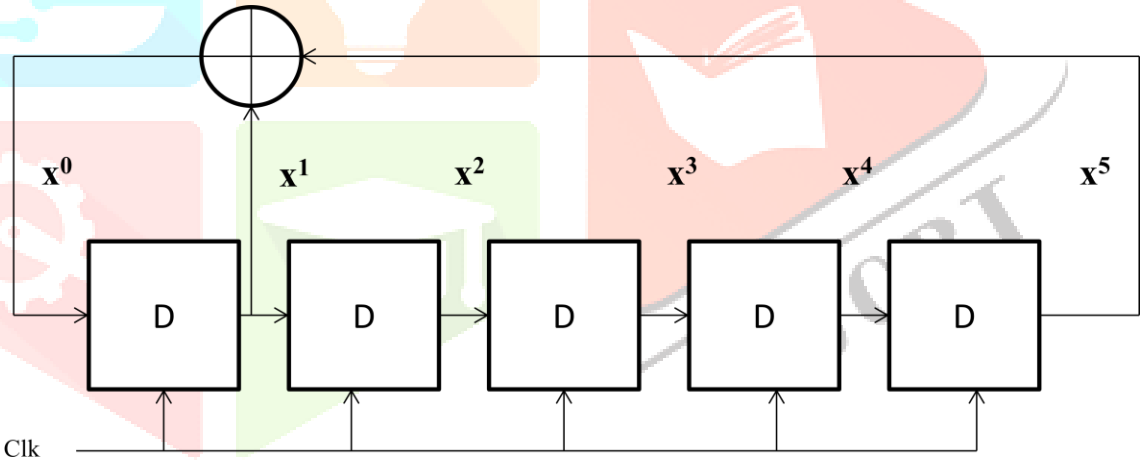


Fig. 5-bit LFSR

Circuit Diagram of 8-bit Ordinary LFSR

D1	D2	D3	D4	D5	D6	D7	D8	No. of Transitions Seed Value
0	1	0	1	1	0	1	1	
0	0	1	0	1	1	0	1	5
1	0	0	1	0	1	1	0	6
0	1	0	0	1	0	1	1	6
0	0	1	0	0	1	0	1	5
0	0	0	1	0	0	1	0	5
Total Number of Transitions								27

Low Power Pattern Generation

Avoiding frequent transitions of the main inputs' logic levels (1 to 0 or 0 to 1) is one approach to enhance the correlation between the bits of consecutive vectors. The new method involves adding three intermediate vectors between each pair of vectors. and the device under test consumes less power. The extra circuitry required to generate the three intermediate vectors is modest, which is illustrated in Appendix A and was created in Verilog, may be simply changed to accommodate the necessary number of LFSR outputs. The method of inserting three intermediate vectors is accomplished by adding two extra layers. The seed vector is fed into the flip-flop outputs in the simulation environment. The feedback taps are chosen in accordance with the polynomial x8 + x + 1. To activate the pattern creation and simulation of the design circuit, just two input pins, test enable and clock, are needed. It's also worth noting that, in addition to decreasing the number of transitions, intermediate vectors may experimentally help in fault detection just as well as traditional LFSR patterns.

Table: Test Patterns for 8-Bit LP-LFSR

#Clk	Pattern	En 1	En 2	S 1	S2	Modified LFSR Output
1	T_1	1	0	1	1	1010 1011
2	T_a	0	0	1	0	1010 1111(R)
3	T_b	0	1	1	1	1010 0101
4	T_c	0	0	0	1	1111(R) 0101
5	T_2	1	0	1	1	0101 0101

PATTERN GENERATION USING TEST PER CLOCK

Every clock period in a test-per-clock BIST system, a fresh set of defects is tested. This BIST method has the benefit of having the smallest pattern length feasible, which may or may not be significant. However, fault simulation time is a significant problem for BIST pattern length.

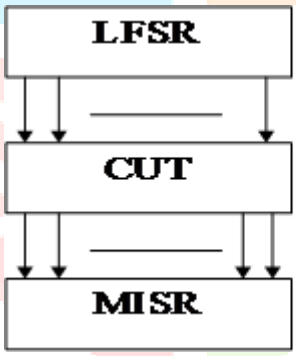


Fig. Test per Clock System

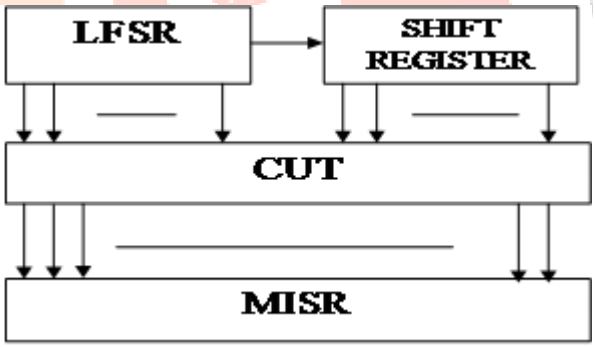


Fig. Large Input Test per Clock System

According to the picture, the patterns may be applied by utilizing the LFSR. If we examine the ordinary LFSR, the patterns can be compared to the previous patterns. The patterns change one or more times, but the inactive pattern is also active, thus the power is higher in the Ordinary LFSR. In Low Power LFSR, the same problem is solved. Because active flipflop is the only pattern that changes, the power is decreased less. This also causes one or more patterns to alter, therefore we may utilize the TEST PER SCAN to counteract this. The seed generator and moebius counter are used in this test per clock. Each moebius pattern is xored with the seed patterns up to a 2l moebius counter, which works similarly to a Johnson counter. As a result, each pattern is applied to the Cut before being applied to the MSIR following pattern creation. Our project may be described using a large number of main inputs and repeated patterns on the CUT, thus overcoming this issue will need the use of the LFSR with the Shift Register. When compared to the LFSR and LP-LFSR, the number of pattern creation is lower, and the changing bit is also lower. These, in turn, are linked to the CUT and the MISR.

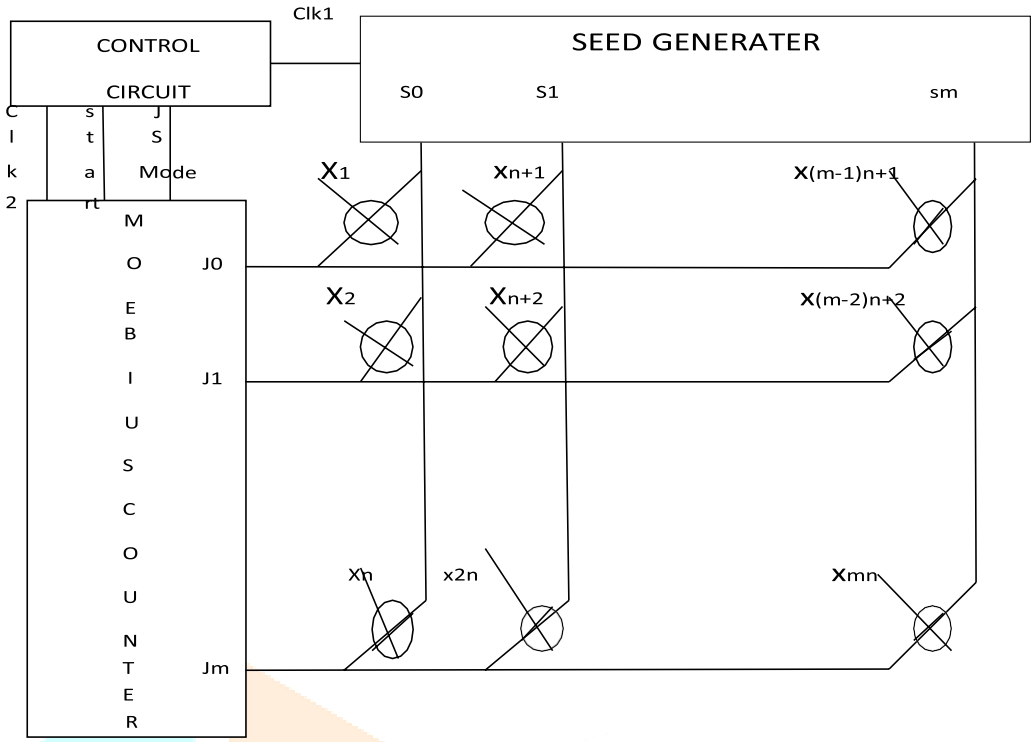
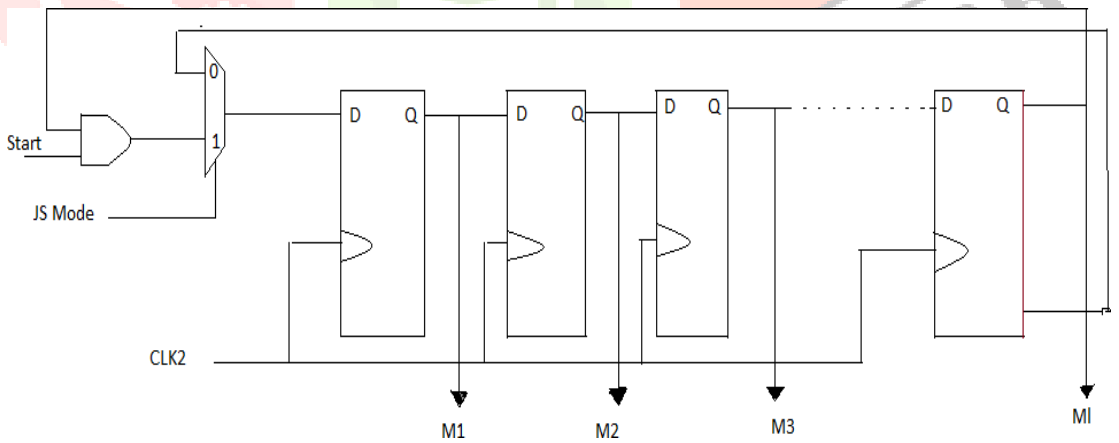


Fig. Test Per Clock Block Diagram

The seed generator functions similarly to an LFSR. In this seed generator, one seed value is generated for each CLK1. With the Moebius counter, this can be XORed. The Polynomial method is used to generate the seed value. The pattern generation is XOR with some element place using this polynomial method. If the pattern is three bits long, the last bit must XOR with the first bit to be inserted in the first position. This can be repeated for all patterns. Let's take a look at how patterns are created as an example. Consider 3bit patterns, such as 101, which represents the value at the first cycle. After CLK1 is triggered a second time, a new seed value, such as 010, the third bit XORed with the first bit, is generated and placed in the first position. This operation will continue for another 2l cycles. Every pattern can be XORed using the moebius counter's 2l cycles. A Johnson counter is similar to a Moebius counter. Multiple patterns are created by complementing the final piece of a pattern put in the first bit. And each pattern that is produced may be XORed with the pattern that the seed generates. This procedure may be repeated up to two times.



Moebius Counter

Table: Test Per Clock

CL K2	J1	J2	J3	CL K1	S1	S2	S 3	J [3:1] ^S [3:1]	N. T
	1	0	0		1	1	0		
1	1	1	0	1	1	1	1	001	
2	1	1	1		1	1	1	000	1
3	0	1	1		1	1	1	100	1
4	0	0	1		1	1	1	110	1
5	0	0	0		1	1	1	111	1
6	1	0	0		1	1	1	011	1
1	1	1	0	2	0	1	1	101	
2	1	1	1		0	1	1	100	1
3	0	1	1		0	1	1	000	1
4	0	0	1		0	1	1	010	1
5	0	0	0		0	1	1	011	1
6	1	0	0		0	1	1	111	1

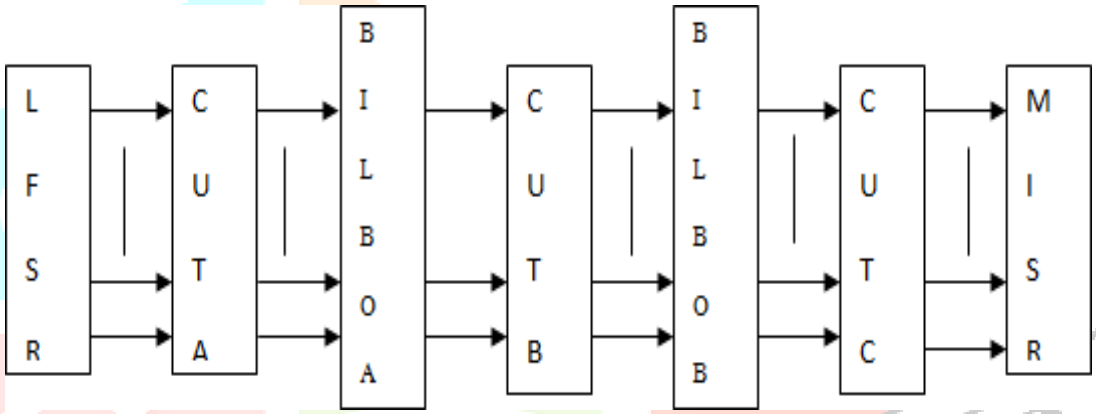
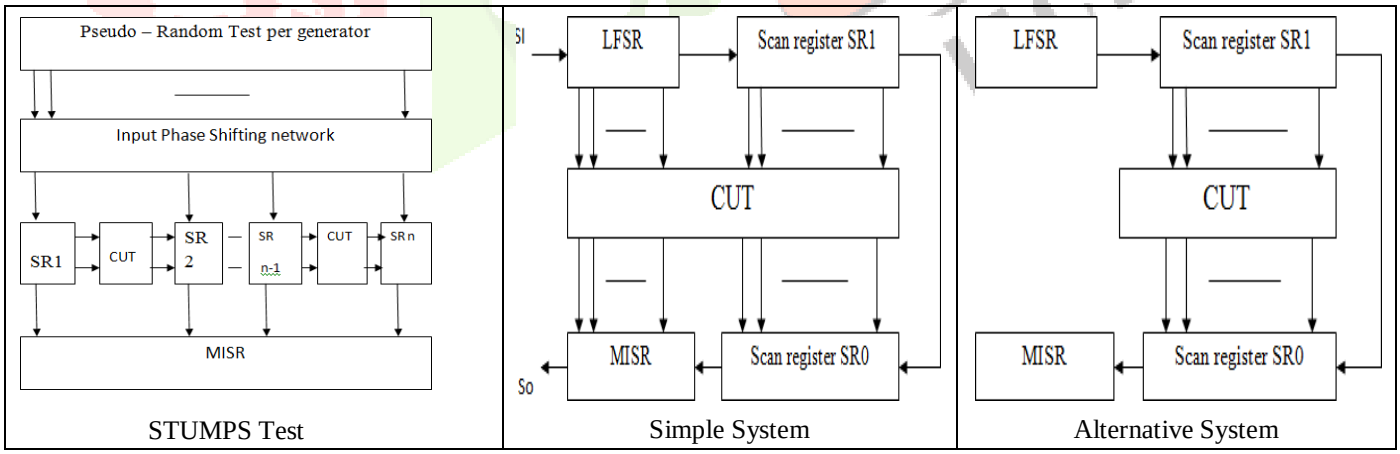


Fig. Test patterns configure using a BILBO

PATTERN GENERATION USING TEST PER SCAN



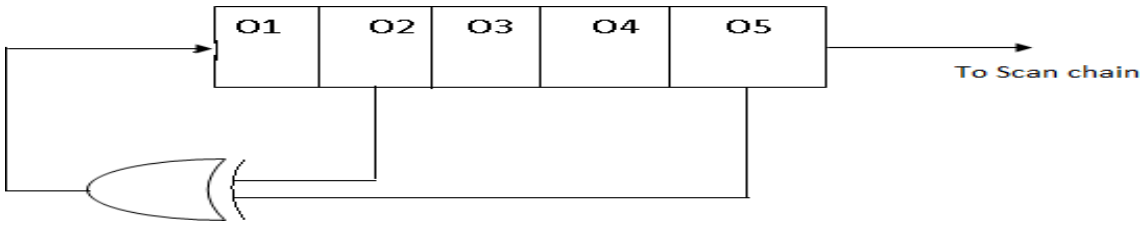


Fig. 5-Bit LFSR Where Bit 5 Feeds the Scan Chain

V. RESULTS AND DISCUSSION

The standard 6-bit pattern is generated using the LFSR configuration. The schematic for traditional pattern generation contains 36 flip-flops connected in series. Feedback taps are added to the design to create a maximal length pattern generator that includes all 0s and 1s. There will be a total of 26 vectors in this case. The clock is the same for all flip-flops. A seed value is assigned to each flip-output flop. Following that, each clock pulse shifts the logic value at the flip-input flop's output to its output.

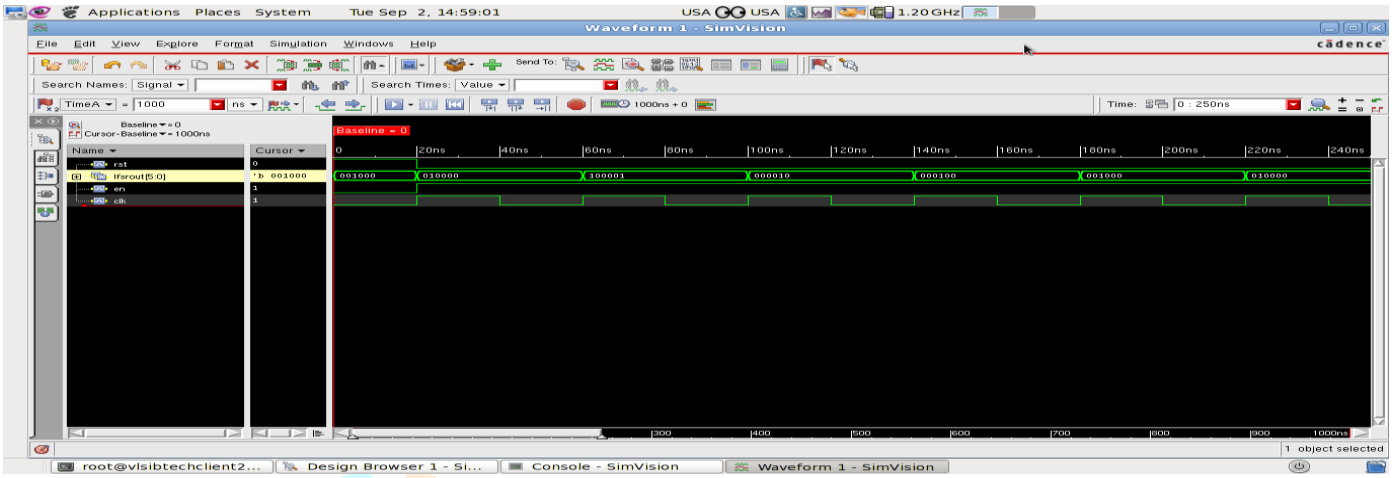


Fig. LFSR Pattern Simulation

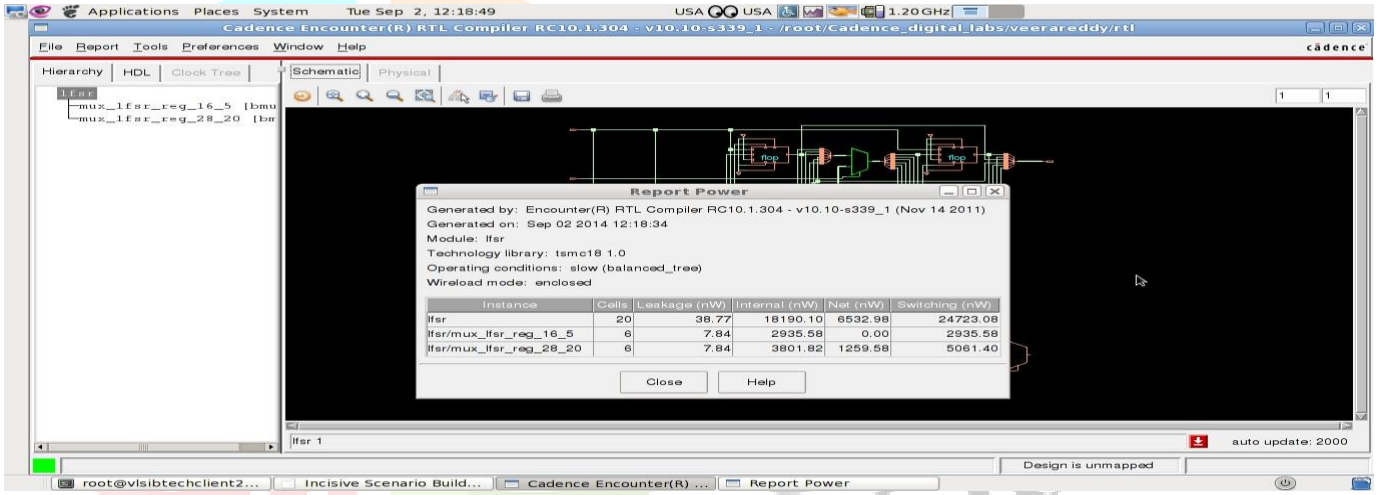


Fig. Switching activity in LFSR

Simulation for Test Per Clock

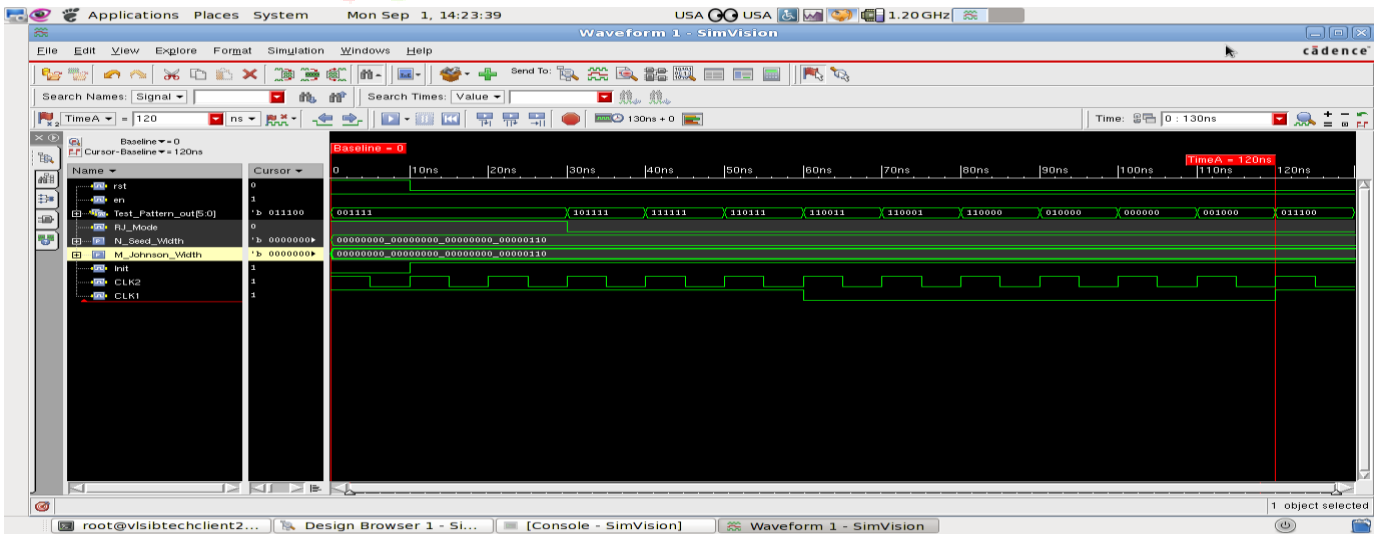


Fig. TPC Pattern Simulations

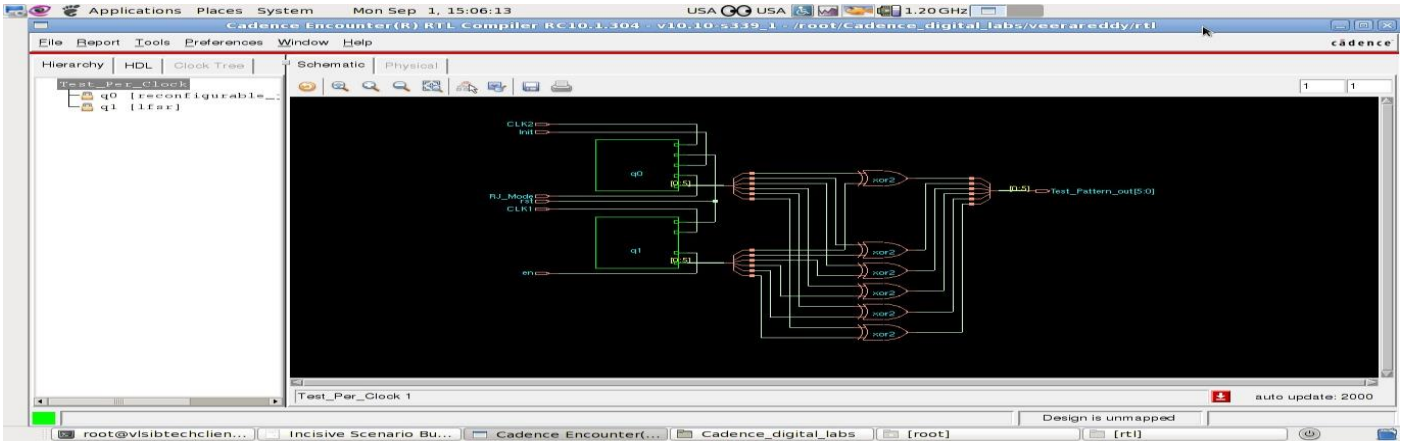


Fig. RTL View FOR TPC

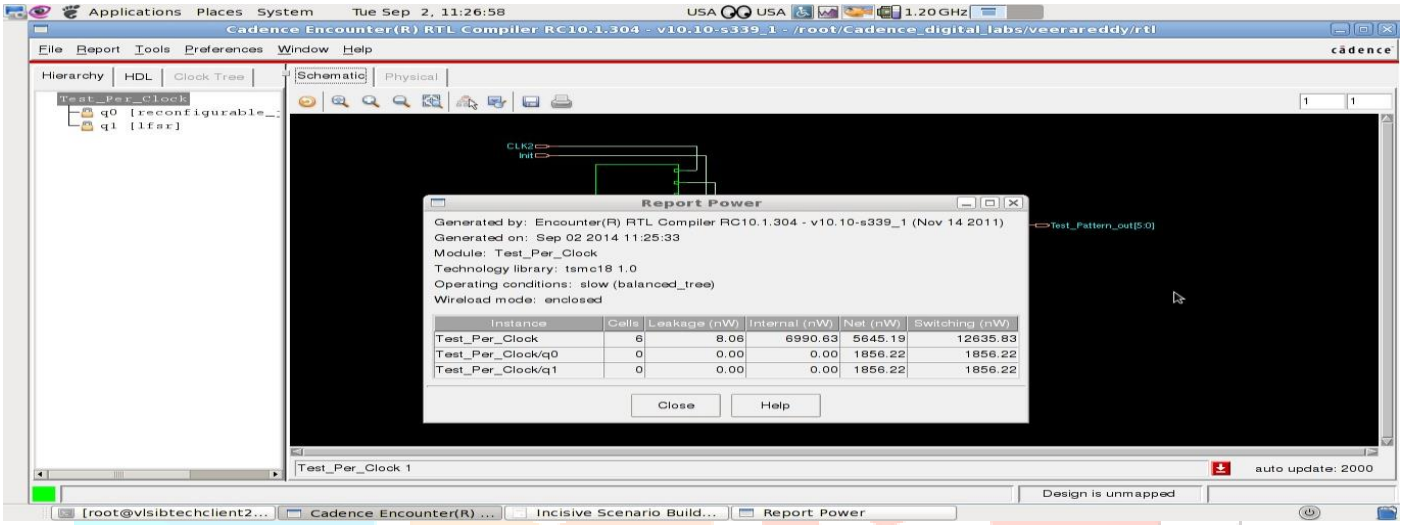


Fig. Detail Power Report of Switching Activity in TPC

Table: Power report

#	Module	Power(nw)
1	LFSR	54489.896
2	Test Per Clock	7011.390

VI. CONCLUSION

Both design and test engineers are challenged by the System on a Chip revolution, especially in the field of dissipation of electricity. In the manufacturing test model, the chip consumes more power than it does in normal operation in the intended system. Increased power consumption may lead to irreparable chip degradation, which has a direct effect on total yield and cost. The basic process for IC Design, Test, and Manufacturing, including design entry, tool flow methodology, and hand-off to Manufacturing, is examined in this paper. The verification and testing of ICs receives special attention. Today, the main stream method for IC design is Design-For-Test and Design-For-Manufacturing. This technique requires the whole SOC development team to work closely together in clearly defining sufficient test criteria and methods, as well as guaranteeing the chip's manufacturing capability. Other trade-off considerations, such as the number of pins required in the device for testing, and the development of external vs. internal patterns, and so on, must be carefully considered in order to arrive at the best cost-performance test solution. For power consumption estimate, a technique for generating low power PRPG is developed and used on an industry standard circuit. When compared to the LFSR, TPC reduces the power by approximately 78 percent.

REFERENCES

1. Singh, Balwinder, Arun Khosla, and Sukhleen Bindra. "Power optimization of linear feedback shift register (LFSR) for low power BIST." *2009 IEEE International Advance Computing Conference*. IEEE, 2009.
2. Hamid, Muhammad E., and Chien-In Henry Chen. "A note to low-power linear feedback shift registers." *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 45.9 (1998): 1304-1307.
3. Saraswathi, T., K. Ragini, and Ch Ganapathy Reddy. "A review on power optimization of linear feedback shift register (LFSR) for low power built in self test (BIST)." *2011 3rd International Conference on Electronics Computer Technology*. Vol. 6. IEEE, 2011.
4. Lowy, Menahem. "Parallel implementation of linear feedback shift registers for low power applications." *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 43.6 (1996): 458-466.
5. Tyagi, Abhishek, Neeta Pandey, and Kirti Gupta. "PFSCL based linear feedback shift register." *2016 international conference on computational techniques in information and communication technologies (ICCTICT)*. IEEE, 2016.
6. Sasi, Abubaker, et al. "Hybrid memristor-CMOS based linear feedback shift register design." *2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, 2017.
7. Kumar, YG Praveen, B. S. Kariyappa, and M. Z. Kurian. "Implementation of power efficient 8-bit reversible linear feedback shift register for BIST." *2017 International Conference on Inventive Systems and Control (ICISC)*. IEEE, 2017.
8. Baskar, S., and V. R. Dhulipala. "Biomedical rehabilitation: data error detection and correction using two dimensional linear feedback shift register based cyclic redundancy check." *Journal of Medical Imaging and Health Informatics* 8.4 (2018): 805-808.
9. Aloisi, Walter, and Rosario Mita. "Gated-clock design of linear-feedback shift registers." *IEEE Transactions on circuits and systems II: Express briefs* 55.6 (2008): 546-550.
10. Teimoory, Mehri, et al. "Memristor-based linear feedback shift register based on material implication logic." *2015 European Conference on Circuit Theory and Design (ECCTD)*. IEEE, 2015.
11. Hussain, Sabir, and V. Malleshwara Rao. "An SIC-BS linear feedback shift register for low power BIST." *2017 Devices for Integrated Circuit (DevIC)*. IEEE, 2017.
12. Krishna, K. Murali, and M. Sailaja. "Low power memory built in self test address generator using clock controlled linear feedback shift registers." *Journal of Electronic Testing* 30.1 (2014): 77-85.
13. Zhang, Xinmiao, and Yok Jye Tang. "Reducing parallel linear feedback shift register complexity through input tap modification." *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019.
14. Mishra, Shivshankar, Ram Racksha Tripathi, and Devendra Kr Tripathi. "Implementation of configurable linear feedback shift register in VHDL." *2016 International Conference on Emerging Trends in Electrical Electronics & Sustainable Energy Systems (ICETEESES)*. IEEE, 2016.
15. Li, Rui, et al. "A new low power BIST methodology by altering the structure of linear feedback shift registers." *ASICON 2001. 2001 4th International Conference on ASIC Proceedings (Cat. No. 01TH8549)*. IEEE, 2001.
16. Singh, Dharmendra, et al. "Low Power Optimization Technique Based Linear Feedback Shift Register." *i-Manager's Journal on Circuits & Systems* 6.1 (2017): 20.
17. Mehta, Digvijay Singh, et al. "A Hardware Minimized Gated Clock Multiple Output Low Power Linear Feedback Shift Register." *Advances in VLSI, Communication, and Signal Processing*. Springer, Singapore, 2020. 367-376.