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FUZZY CONTROLLED SERIES ACTIVE POWER FILTER IN SINGLE PHASE SYSTEM FOR MITIGATION OF HARMONICS

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Abstract: We devised a single phase series active power filter in this study to reduce harmonics in grids with non-linear loads and power electronic equipment. Active power filters (APFs) can compensate for power quality issues because they can dynamically vary their modes of operation in response to changes in load or in the power system. The series active power filter was designed specifically to address issues with the power system waveform and voltage amplitude among this solution. The series active power filter has not been widely used despite its ability to mitigate voltage sag, voltage swell, voltage harmonics, and voltage imbalance in three phase systems. The lack of interest in this equipment can be somewhat explained by the SeAPF conventional topology's limitations, as well as its high price. The regulated algorithm of a single phase SeAPF that is connected directly to the power grid without the usage of external power sources is discussed in this work. In the proposed configuration, the active power filter controller is further updated with a Fuzzy interface system with 49 rule basis, which would replace the old PI controller.

Index Terms **- Single Phase Series Active Power Filter, Active Power Filter, Harmonics, Power Quality, Voltage Swell, Voltage Sags**.

I. INTRODUCTION

Nowadays , electronic equipment is a part of the everyday life of any home , we live in such a technologically advanced era. Moreover, with the technology development of industy as well as more ambitious demands In terms of quality and quantity, industry. However, these sophisticated domestic and automated devices, when connected to the power grid (PG), produce a high harmonic current content, causing electricity quality problems that therefore have a monetary impact on consumers. Variable speed drives, soldering machines and other high-power electronic equipment as well as TVs, computers, Printers, electronic ballasts lamps, fridges and smartphone chargers are some examples with a steady presence in the industry and at home. Many of these devices are similar to an uncontrolled diode rectifier followed by a DC-Link, which causes a high current harmonic content. Therefore, these current harmonics, while following the line impedances,cause harmonic distortions in the PG voltage, which makes it a serious problem for electricity generators and in particular, for consumers.

In addition to the previously mentioned harmonic currents, there are other PQ issues with direct implication in PG, we present some examples below-

1. . . Th Momentary interruptions
2. Momentary swells (overvoltages)
3. Inter-harmonics
4. Voltage fluctuations
5. Voltage transients
6. Momentary sags (undervoltages)
7. Voltage notches
8. Voltage imbalance in three phase system

Furthermore , the PQ occurences result in enormous financial losses. According to roughly 30% of the most vulnerable industry sectors may pay a PQ cost of around 4% of their turnover, with voltage sags and temporary disruptions accounting for about 60% of the cost. When compared to the European economy as a whole, the total PQ cost was estimated to be above 150 billion eurose in October 2015 Despite the fact that the PQ issues are primarily caused by consumers, particularly industrial customers, there is a compromise between producers and consumers . the manufactures agree to keep voltage harmonics to a minimum in order to supply electrical energy within specific parameters (EN 50160 Standard)

.Active power filters research and development is a hot topic these days, with solutions capable of dynamically adapting their operation to the PQ problems that exist in the PG. the number of phases, topology, and kind of inverter are used to

categorise them. There are three types of APF phases: single phase, three-phase without neutral, and three-phase with neutral. Therae are four basic APF topologies : series APF (SeAPF),Shunt APF (ShAPF), Hybrid APF(HyAPF) and Unified Power Quality Conditionar(UPQC). The first two APFs, SeAPF and ShAPF, are primordial topologies that are widely employed to correct for voltage and current difficulties, respectively. An UPQC is formed when these two topologies are joined. The HyAPF, on the other hand, is based on combining SeAPF with tuned harmonic passive power filters. Finally, the APF is classified as a voltage source inverter(VSI) or a current source inverter (CSI) based on the storage element used in the power converter's DC-Link.

APFs are made up of an acquisition system and a control system, which work together with the power converter to enable autinimous PQ mitigation. The SeAPF, in particular, is capable of reducing the majority of the problems connected to the voltage of thePG, as shown by the PQ problems mentioned above (i.e momentary interruptions,sags,swells,voltage,fluctuation,notches,transients and voltage unbalance).

The SeAPF works in the same way as an ideal voltage source, supplying a voltage in phase opposition to the PG's harmonic content allowing the load's voltage waveform to be sinusoidal with this notion in mind, the first solutions to reduce PQ difficulties were devised in 1970.As shown in Fig. 1 (a), the "traditional" single-phase SeAPF topology with coupling transformer between the APF and the PG, as well as an auxiliary external power supply on the DC-Link, emerges at this time. These features offer galvanic isolation between the APF and the PG via the transformer, as well as the ability to correct for long-term undervoltages and overvoltages caused by the external power supply. However, because the SeAPF injects voltage harmonics through the coupling transformer, it results in high losses and overheating, shortening the SeAPF's life cycle.

Furthermore, the usage of transformers and external power sources increases the size and cost of this equipment, making it less appealing for purchase [17].As a result of these factors, a new topology is provided in this research, as seen in Fig. 1. (b). This revolutionary SeAPF architecture eliminates the superfluous and costly components of the traditional design, making it more efficient and compact. The control system, on the other hand, needs to be more advanced. The implementation of control algorithms, on the other hand, does not appear to be a barrier due to the technical improvement of microcontrollers, which now have a high processing capacity, additional memory, and peripherals. To accomplish so, a synchronisation method would be required to maintain a reference voltage that is immune to PG distortions and to control the SeAPF DC-Link to the reference voltage. It is feasible to manage the SeAPF to eliminate PQ difficulties and give energy to the loads with a sinusoidal voltage waveform by combining this with the information collected from the system sensors

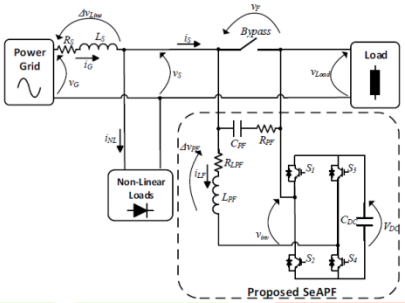

Figure : Proposed topology

CONTROL STRATAGY

The control strategy of this topology is divided into three main blocks: the Phase Locked Loop (PLL), the DC-Link regulation and the compensation voltage as shown in Fig. 2. The PLL control algorithm composes the first block. This algorithm has the functionality of generating a sinusoidal waveform, vPLL, synchronized with the fundamental component of the PG voltage, vS [15]. The implemented PLL control algorithm also generate a unitary signal, vPLL unitary, used in the Compensation Voltage Calculation block. The DC-Link Regulation block is in charge of determining a voltage component, vReg, that is responsible for DC-Link regulation. For this, the difference, VDC Error, between the reference value, VDC*, and the actual voltage value on the DC-Link, VDC, must be determined, as shown in (1). As shown in (2), the VDC Error and vPLL are then employed in a PI controller to compute the voltage regulation component, vReg, in order to force the SeAPF to operate continuously. Finally, vComp, the compensation voltage shown in (3), is the total of the three parts: To keep the load voltage at 230 V RMS, use the passive filter voltage, vpf, the harmonic voltage, vH, provided in the PG voltage, and the balancing voltage, vBalance. The passive filter voltage is calculated using (4), where the current passing through the inductor and the equivalent series resistor, RLPF, are used as inputs. Then, by comparing the PLL output signal, vPLL, and the PG voltage, vS, the (5) corresponding to the harmonic voltage, vH, is obtained. Finally, the balance voltage, vBalance, is computed by comparing vPLL and the intended load voltage, as shown in the diagram (6). To produce the reference voltage, vRef, that SeAPF needs to synthetize, equation (7) represents the total of the compensation and regulation voltages. When this value is compared to the SeAPF voltage, vF, an error signal, vRef Error, is generated (8). The SPWM block generates the pulses that will be applied to the gate of the IGBTs that make up the SeAPF, and this error is the input of a PI controller that will generate the modulation waveform, as shown in (9).

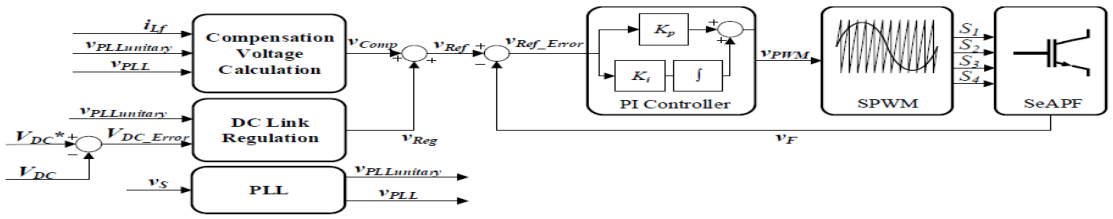

Fig. 2. Block diagram of the SeAPF control strategy.

$VDC\ error = VDC^{*} - VDC$ (1)

$v\ Reg = vpLL\ [kpVDC\ error + ki \int VDCerror\ dt]$ (2)

$vcomp = \triangle vpf + vH + vBalance$ (3)

$\triangle vpf = RLPFiLF + LPF\ d/dt\ iLF$ (4)

$VH = Vpll - vs$ (5)

$vBalance = A^{\wedge}\ .v\ PLL\ unitary - vPLL$ (6)

$vRef = v\ comp + vReg$ (7)

$v\ Ref\ Error = vF - vReg$ (8)

$Vpwm = kpvRef\ Error + ki \int vref\ Error\ dt$ (9)

SIMULATION RESULTS

Computer simulation is now a common technique for validating not only the hardware topology but also all of the control algorithms that make up the control system. It is feasible to forecast the behaviour of the SeAPF and tweak the control algorithms using specialised simulation software. It was therefore feasible to do a more extensive analysis of the SeAPF in order to appropriately size all of the components. The simulation results achieved using the proposed topology are shown in this section. The simulation graphs depict the behaviour of each control block shown in Figure 2. With the system parameters defined, the suggested topology was simulated using the PSIM 9.1 software tool.

TABLE I defines the parameters. The suggested topology, which consists of a two-leg full-bridge inverter with an RLC passive filter in series with the PG and the load, does not utilise a transformer or an external power source (a resistive load in the presented results). The simulation employed unipolar sinusoidal pulse width modulation as the voltage modulation (SPWM).The simulation includes five case studies to validate the system's reliability: (1) PLL; (2) pre-charging of the DC-Link capacitor; (3) system in steady state operation; (4) system in transient operation, facing PG voltage sag; (5) system in steady state operation; (6) system in transient operation, facing PG voltage sag; (7) system in steady state operation; (8) system in transient operation, facing PG voltage .

TABLE I. System parameters used in the SeAPF simulation model.

System Parameters	Value
PG Voltage/Frequency	230 V/50 Hz
Power System Apparent Power	2.4 kVA
DC-Link Nominal Voltage	200 V
Load impedance	26 Ω
Switching frequency	20 kHz Unipolar SPWM
Passive Filter	L_{PF} = 800 µH, C_{PF} = 40 µF; R_{PF} = 8 Ω

A.THE PHASE-LOCKED-LOOP (PLL) IS A TYPE OF PHASE-LOCKED LOOP.

During the turn-on transient, the PG voltage, vS, and the consequent plot of the PLL control algorithm, vPLL, are shown in Fig. 3. The vS utilised in the simulation is identical to the actual voltage waveform in the laboratory, obtained using a power quality analyzer FLUKE 435 series II, in order to bring the simulation closer to reality. As can be seen, the vPLL is fully synchronised after four PG cycles, and the synchronisation is maintained after that. Furthermore, even with a THD of 5.76 percent on the PG voltage, the resulting signal exhibits a residual total harmonic distortion (THD) of 0.56 percent.

B. Method of DC-Link Pre-Charging

The DC-Link pre-charging approach is based on the SeAPF synthetizing a low amplitude sinusoidal waveform in phase opposition to the PG voltage, as detailed in section II. Figure 4 depicts the result obtained using this strategy. Because the SeAPF is connected in series with the load and must operate in good circumstances, this pre-charging is done slowly, requiring many hours. To attain the DC-Link reference voltage, it took 7.5 seconds. It's worth noting that the DC-Link pre-charging occurs only once, when the system is turned on, and the SeAPF doesn't compensate for voltage harmonics at this time.

C. Stable State

The system switches to SeAPF mode after the DC-Link has been charged with the reference voltage. The SeAPF operation yielded the following results (Fig. 5). (b). As can be seen, the PG and load voltages have the same rms values and are equivalent to the nominal voltage of 230 V. However, as can be seen, the load voltage, vLoad, has a sinusoidal waveform, indicating that the SeAPF adjusted for the PG voltage harmonics. The PG voltage has a THD percent f of 5.57 percent, while the load voltage has a THD percent f of 0.89 percent.

D. Power Grid Disturbances and Transient Operation

One of the SeAPF's requirements is to compensate for voltage sags and swells. A voltage sag and a voltage swell of 30 percent and 13 percent severity, respectively, were simulated to establish this right operation, as shown in Fig. 6. In both scenarios, compensating for PG disruptions relies on maintaining a constant energy absorption from the SeAPF and reducing the PI

controller's integral error in the DC-Link regulation process. When the PG sags or swells, this strategy provides for a quick response.

1) a sag occasion

The sag event was set to occur after 6 seconds. The control system was able to detect it very instantly and apply user constraints. To keep the load voltage, vLoad, constant, the SeAPF injects the energy stored in the DC-Link.stable. This procedure is depicted in Figure 6. (a). The recovery process is depicted in Fig. 6 (b), where the DC-Link voltage, VDC, is quickly restored without interfering with the load voltage, vLoad's stability

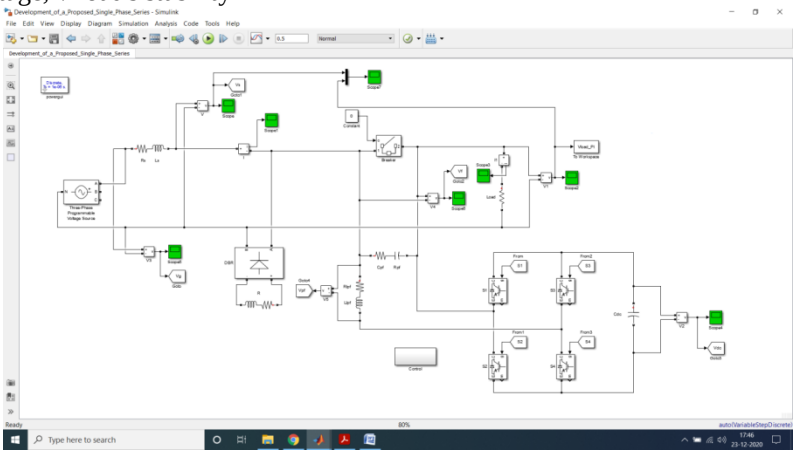

Fig. : Modeling of proposed test system

The test system shown above is modelled with a three-phase programmable grid source but only uses one phase. This block is used to make sags and swells in a line using the programming time settings as shown below.

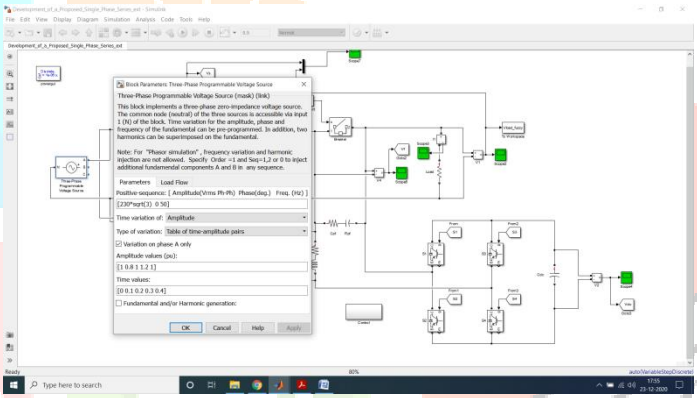

Fig. : Sag swell conditions in programmable source

The simulation time is set at 0.5 seconds in total. The sag condition is set between 0.1 and 0.2 seconds, and the swell condition is set between 0.3 and 0.4 seconds. The system continues to function normally with no sags or swells for the remainder of the time. For the suggested series active power filter, the control structure modelling with PI controller is shown below. As a tweak to the system, control structure modelling with fuzzy controller is given below.

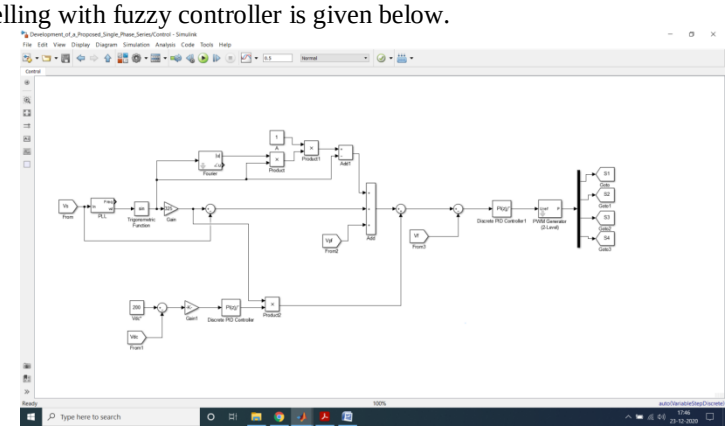

Fig. : Proposed control structure with PI controller

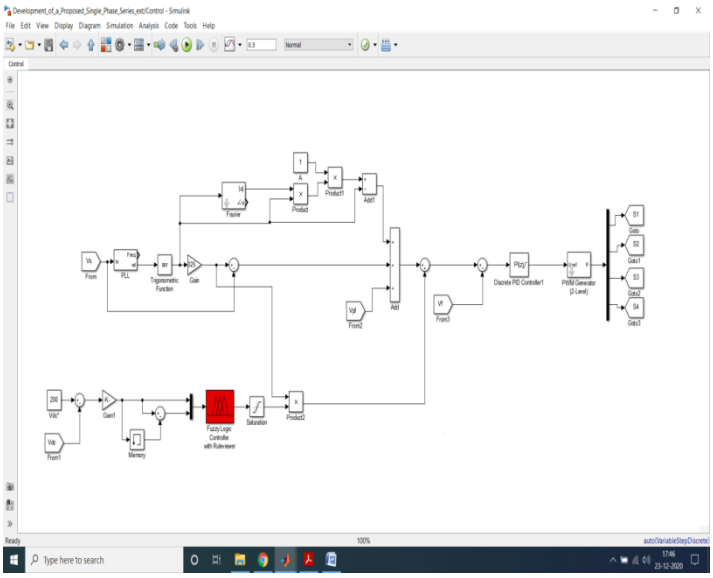

Fig. : Proposed control structure with fuzzy controller

After running the simulation for 0.5sec the output are plotted as below.

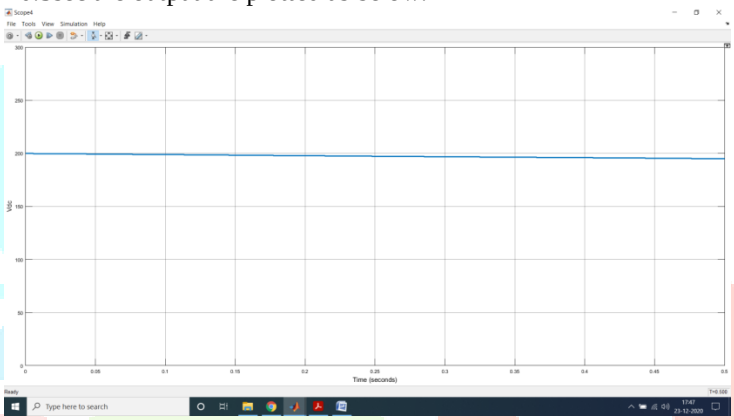

Fig. : DC voltage across DC capacitor

The above is the DC link capacitor voltage of the series active power filter.

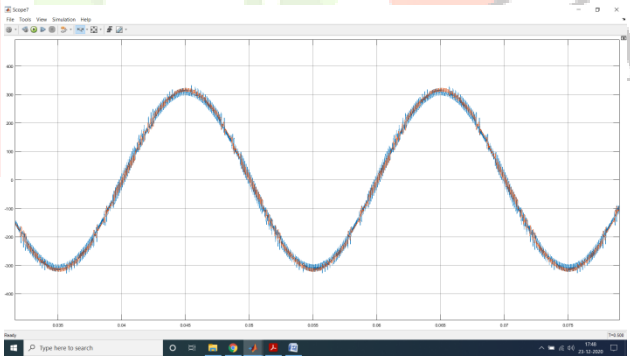

Fig. : Vs and VL during normal operating condition

The above graph is the comparison of source voltage Vs and load voltage VL during normal operating condition. As said above a voltage sag is introduced from 0.1 to 0.2sec. for which the Vs and VL comparison is shown below.

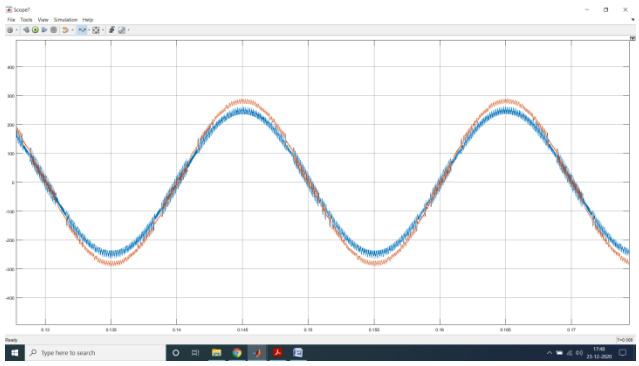

Fig. : Vs and VL during sag operating condition

The same comparison of Vs and VL is done for swell condition from 0.3 to 0.4sec.

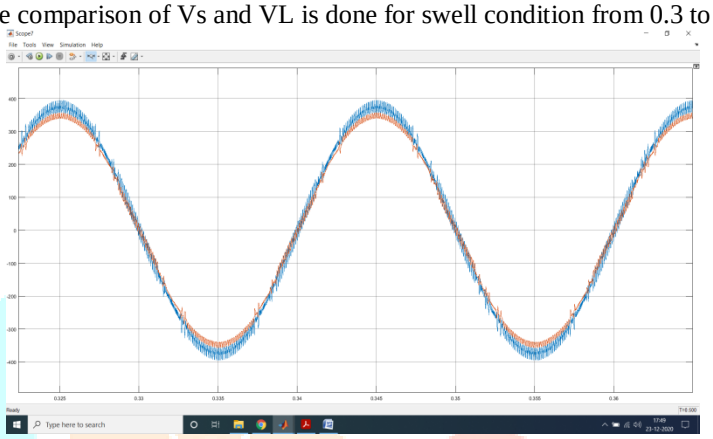

Fig. : Vs and VL during swell operating condition

The total harmonics distortion of the voltages are taken using FFT analysis tool available in powergui block of simulink. The below are the THD analysis of Vs, VL with PI controller and VL with fuzzy controller.

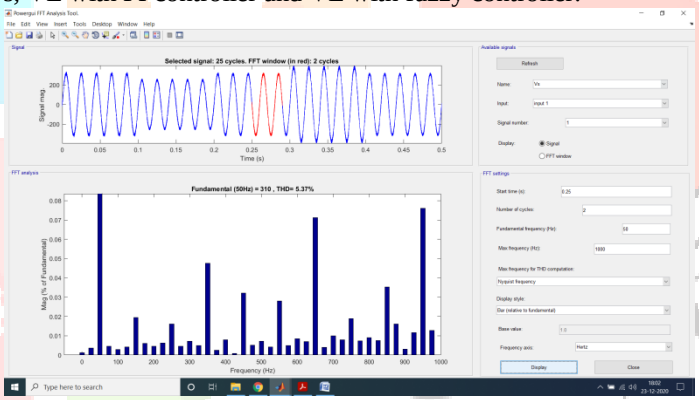

Fig. : THD of source voltage Vs

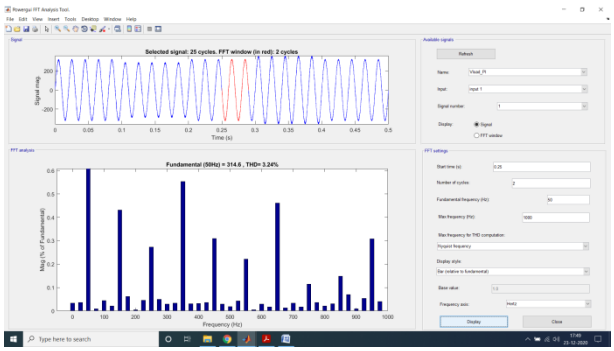

Fig. : THD of load voltage with PI controller

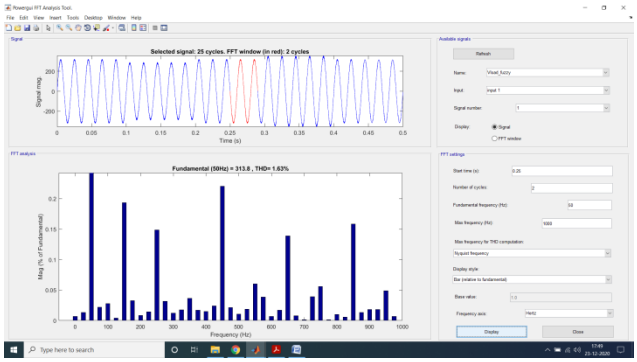

Fig. : THD of load voltage with fuzzy controller

CONCLUSION

Voltage compensation during sag and swell is performed using injection and absorption of voltage from the line in the above study and comparison of the series active power filter linked to a single phase grid. To synchronise the control signals with the PG and calculate the compensation voltage, the control method relies on a PLL circuit. During steady-state operation, the SeAPF compensates for PG voltage harmonics, resulting in a sinusoidal load voltage. Using the FFT analysis tool on the source voltage Vs and load voltages VL for both the PI and fuzzy logic controllers, the THD with the fuzzy logic controller is maintained at 1.63 percent, while the PI controller is maintained at 3.24 percent. Both controllers, however, enhance THD of the voltage when compared to Vs, which is 5.37 percent, but the fuzzy controller has less THD than the PI controller.

Future Scope

The controller can be upgraded with better synchronous controllers, which will improve the voltage profile even more and provide better voltage compensation for the system. Enhanced controllers, such as optimization and adaptive controllers, will improve compensation voltage prediction as well as voltage injection and absorption under sag and swell circumstances.

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