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Design of ALU using Ternary logic.

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ABSTRACT: Ternary logic is a reliable method for defining, analyzing, testing and implementing the basic combinational circuitry with VHDL simulator. It offers better utilization of transmission channels because of its high speed for higher information carried out and it gives more efficient performance. One of the major advantage of the Ternary logic is that reduces the number of required computation steps, simplicity and energy efficiency in digital logic design. This project using reliable method is brought out for implementing the basic combinational, sequential and T-ALU (Ternary Arithmetic and Logic Unit) circuitry with minimum number of ternary switching circuits (Multiplexers). In this the potential of VHDL modelling and simulation can be applied to ternary switching circuits to verify its functionality and timing specifications. An intention is to show how proposed simulator can be used to simulate MVL (Multi Value Logic) circuits and to evaluate system performance.

Keywords: Gate count, MVL, reliability- unreliability model, Ternary switching levels

I. Introduction

Digital system design has traditionally been associated with the binary circuits where digital computations are performed on two possible logic values , that is 0 and 1 in the boolean space. However, for the last couple of decades, multi valued logic(MVL) has received and increasing interest over the binary ones for designing digital circuits[1]. The most efficient MVL, which provides less complexity and product cost than binary logic, is three-valued logic or ternary logic. As a result extensive research can be found on circuit and system implications of ternary logic using CMOS in the ternary logic.

II. Arithmetic Logic Unit

An arithmetic logic unit (ALU) is a digital circuit used to perform Arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers[2]. A register is a small amount of storage available as part of a CPU. The control unit tells the ALU what operation to perform on that data, and the ALU stores the result in an output register. The control unit moves the data between these registers, the ALU, and memory.

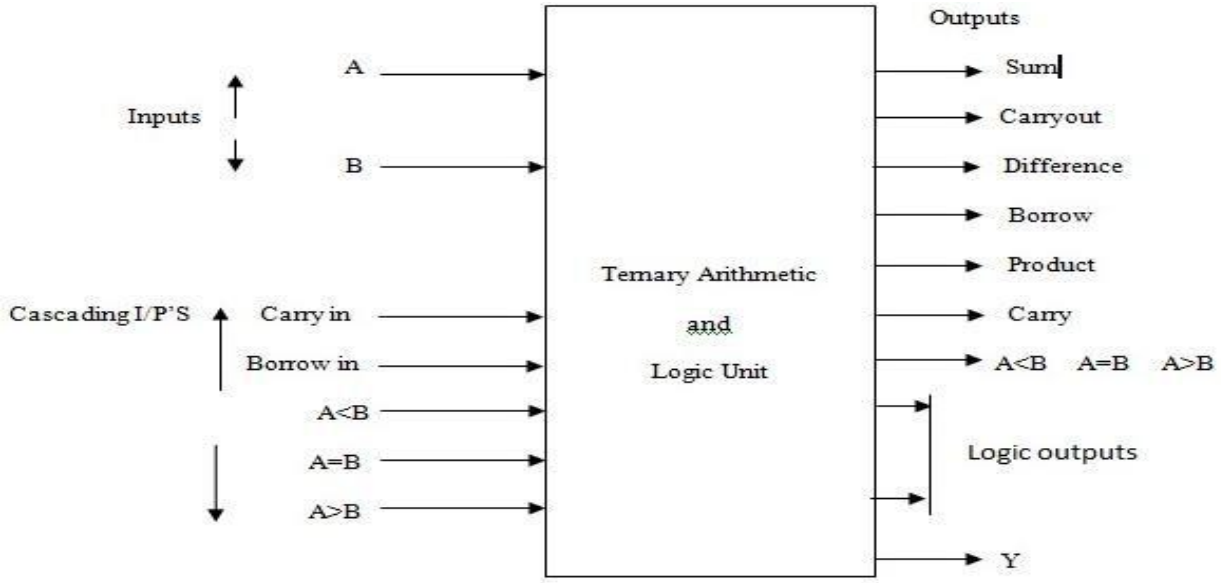

Figure 1 : Block Diagram of ALU

We all are familiar with the arithmetic operations like addition, subtraction, multiplication and division of decimal number. Similar operations can be performed on ternary numbers. The rules for ternary addition, subtraction, multiplication and division are different but these are closely related to binary arithmetic operations. In existing binary digital system, the output of the system is decided by considering two input conditions i.e. either ON (favorable or true logical level 1) or OFF (un favorable or false logic at logic level 0) leaving behind the third conditions i.e. when both the input conditions are same, here decision is consider as don't care or it is discarded by the system. Such situation generally occurs in sequential circuit design. Consider a digital system where both the inputs are same i.e. either 00 or 11as shown in figure 1.2 Hear in binary system output will be uncertain or will be same as that of previous state of the system but in practice, system must give the output that will satisfy both the input conditions mentioned above. It is shown in figure 1.2 here the system gives the output which is balanced and this state is regarded as third state i.e. can't say or

can't make any decision. So to make third decision the radix of the system must be greater than 2. Here the third logic level is introduced whose system radix is greater than 2.

In a circuit, logic gates will make decisions based on a combination of digital signals coming from its inputs[3][4]. Most logic gates have two inputs and one output. Logic gates are based on Boolean algebra. At any given moment, every terminal is in one of the two binary conditions, *false* or *true*. False represents 0, and true represents 1. Depending on the type of logic gate being used and the combination of inputs, the binary output will differ. A logic gate can be thought of like a light switch, wherein one position the output is off -- 0, and in another, it is on -- 1. Logic gates are commonly used in integrated circuits (IC).

III. Ternary Arithmetic & Logic Circuits

Ternary Logic Circuits

Ternary inverter is a circuit that gives the output in inverted form of input. Three types of inverter operations are possible in ternary logic. These are STI (simple ternary inverter) PTI(positive ternary inverter) & NTI (Negative ternary inverter) such that,

STI is 2-x ; PTI , NTI $= \overline{X}^i = 1$ if $X \neq i$; PTI , NTI $= \overline{X}^i = i$ if $X = i$;

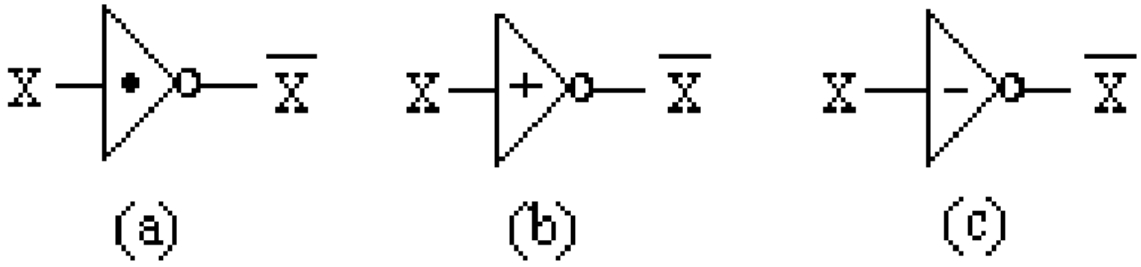

Figure 2 : Symbols for STI, PTI & NTI

Table 1 : Truth Table for STI , PTI & NTI

Input X	Output		
	STI	PTI	NTI
0	**2**	**2**	**2**
1	**1**	**2**	**0**
2	**0**	**0**	**0**

In general OR operation is defined as (*y*) = max(*x*1, *x*2…*xn*) i.e. where y is an output and x's inputs. Ternary OR is a circuit that have X1---Xn as input & Yo as output such that T −OR = Y0 = X1+ X2 − − − − + Xn = Max[X1,X2 − − −Xn] & Ternary NOR has an output that is compliment as OR function . The sign '+' indicates logical ternary OR logic operation. Depending upon the type of inverter used, the logic functions T-

OR/NOR can be Simple ternary OR/NOR [ST-OR/NOR], Positive ternary OR/NOR [PT-OR/NOR], Negative ternary OR/NOR [NTOR. NOR]

AND operation is defined as (y) = min(x1, x2...xn) i.e. where y is an output and x's are inputs i.e. T −AND = Y0 = X1.X2 − − − − −Xn = Min[x1 x2 …….xn] ; T − NAND is the Compliment of AND Function.

Ternary Ex-OR is ternary addition neglecting carry. It is defined as T - EX - OR = X1⊕X2 ;

Table 2 : Truth Tables for Ternary AND, OR, NAND, NOR, EXOR

X1	X2	AND	OR	NAND	NOR	EX OR
0	0	0	0	2	2	0
0	1	0	1	2	1	1
0	2	0	2	2	0	2
1	0	0	1	2	1	1
1	1	1	1	1	1	2
1	2	1	2	1	0	1
2	0	0	2	2	0	2
2	1	1	2	1	0	1
2	2	2	2	0	0	0

Ternary Arithmetic Operations

Let augend be equal to 0, addend be equal to 0 it gives Sum = 0 + 0 = 0 and no carry generated so carry = 0 . If when augend be equal to 1, addend be equal to 2 we get 1 + 2 = 3.i.e. representation for 3 in ternary is 01 that implies sum = 0 and carry = 1. Similarly when augend be equal to 2, addend be equal to 2 we get 2 + 2 = 4. i.e. representation for 4 in ternary is 11 that implies sum = 1 and carry = 1.

Let Minuend be equal to 0, Subtrahend be equal to 0 it gives Difference = 0 – 0 = 0 and no Borrow generated so Borrow = 0 [5] . If when Minuend be equal to 1, Subtrahend be equal to 2 we get 1 - 2 = -1.i.e. representation for 3 in ternary is 01 that implies Difference = 0 and borrow = 1. Similarly when Minuend be equal to 2, Subtrahend be equal to 2 we get 2 - 2 = 0. i.e. representation for 0 in ternary is 00 that implies Difference = 0 and borrow = 0.

In Comparator we are comparing two 1 bit ternary numbers , based on the condition satisfied i.e., a>b, a<b, a=b; the output is set to '2', and all the other values are set to '0'

Table 3 : Truth table for Half-adder, Half Subtractor & Comparator

A	B	Carry	Sum	Diff	Borrow	A=B	A>B	A<B
0	0	0	0	0	0	2	0	0
0	1	0	1	1	2	0	0	2
0	2	0	2	1	1	0	0	2
1	0	0	1	1	0	0	2	0
1	1	0	2	0	0	2	0	0
1	2	1	0	1	2	0	0	2
2	0	0	2	2	0	0	2	0
2	1	1	0	1	0	0	2	0
2	2	1	1	0	0	0	0	2

IV.Results

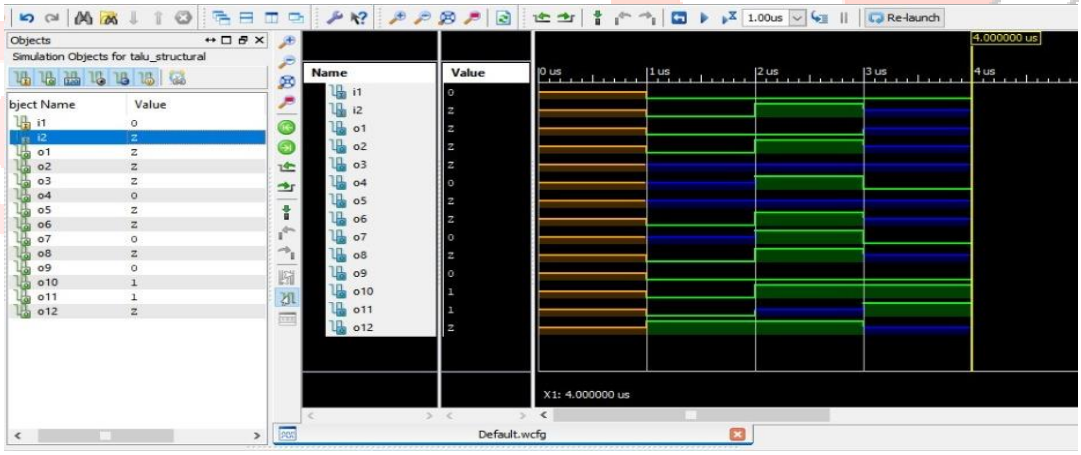

Figure 3 : Simulation Result for Ternary ALU when Input is '0', 'Z'

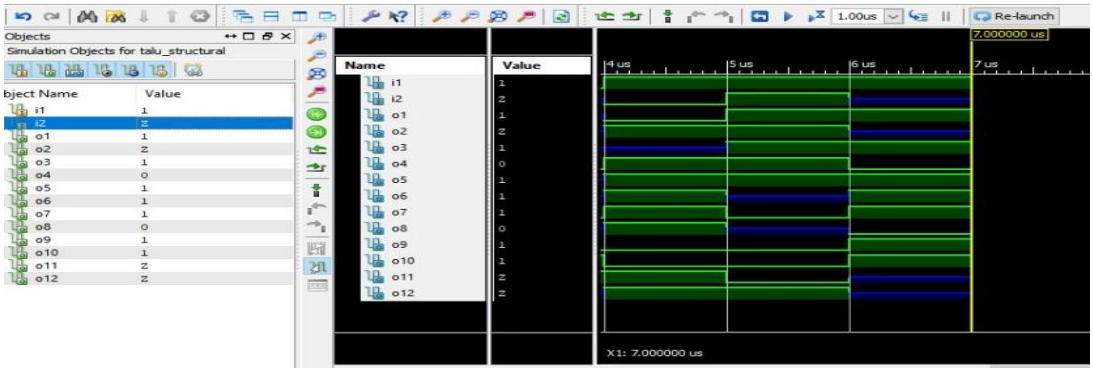

Figure 4 : Simulation Result for Ternary ALU when Input is '1', 'Z'

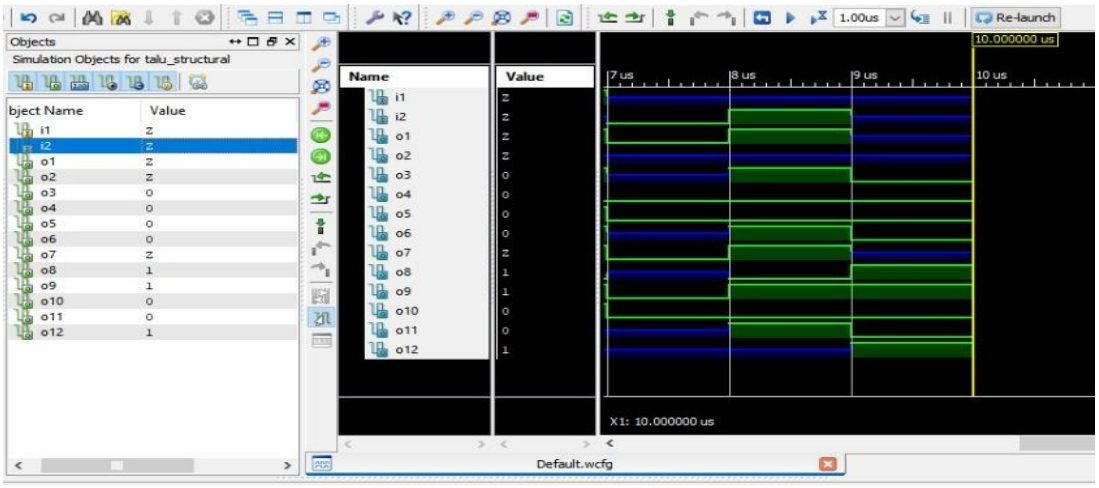

Figure 5 : Simulation Result for Ternary ALU when Input is '1', 'Z'

IV. Conclusion

The ternary logic is a promising alternative to the conventional binary logic design technique. The ternary and binary logic gates can be used to take advantage of their respective merits, to improve performance in terms of computation speed and power consumption. Expanding the existing logic levels to higher levels higher processing rates could be achieved. This ternary system is capable of transmitting more information as compare to binary system.

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