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IMPLEMENTATION OF COST EFFECTIVE SINGLE STAGE THREE LEVEL ISOLATED AC/DC PFC CONVERTER

Ch.S.V.Prakash1,Koyyana Srinivasa Rao[1],G.Mohan Krishna[2],K.Amit Kumar[2],L.Bhuvana Chandra[2],Y.V.S ai Ram[2]

[1](Asst.professor, Dept. of EEE, Lendi institute of engineering and technology, AP, India)

[2](Students, Dept. of EEE, Lendi institute of engineering and technology, AP, India)

Abstract: For low-cost isolated ac/dc power converters adopting high-voltage dc-link, research efforts focus on single-stage multilevel topologies. This paper proposes a new single-stage three-level isolated ac/dc PFC converter for high dc-link voltage low-power applications, achieved through an effective integration of ac/dc and dc/dc stages, where all of the switches are shared between two operations. With the proposed converter and switching scheme, input current shaping and output voltage regulation can be achieved simultaneously without introducing additional switches or switching actions. In addition, the middle two switches are turned on under zero current in discontinuous conduction mode operation, and the upper and bottom switches are turned on under zero voltage. Due to the flexible dc-link voltage structure, high power factor can be achieved at high line voltage.

Key words: DC to DC converter,

I .INTRODUCTION

The power supply unit is an essential circuit block in all electronic equipment. It is the interface between the ac mains and the rest of the functional circuits of the equipment. These functional circuits usually need power at one or more fixed dc voltage levels. Switch mode power supplies (SMPS) are most commonly used for powering electronic equipment since they provide an economical, efficient and high power density solution compared to linear regulators. The devices generally used in industrial, commercial and residential applications need to undergo rectification for their proper functioning and operation. They are connected to the grid comprising of non-linear loads and thus have non-linear input characteristics, which results in production of non-sinusoidal line current. Also, current comprising of frequency components at multiples of line frequency is observed which lead to line harmonics. Due to the increasing demand of these devices, the line current harmonics pose a major problem by degrading the power factor of the system thus affecting the performance of the devices. Hence there is a need to reduce the line current harmonics so as to improve the power factor of the system.

This has led to designing of Power Factor Correction circuits. Power Factor Correction (PFC) involves two techniques, Active PFC and Passive PFC. Here active power factor circuit Converter was designed for improving the power factor. This converter is to observe the effect of the active power factor corrector on the power factor. The advantage of using power factor correction circuits is that to obtain better line regulation with appreciable power factor. Active PFC can be implemented by controlling the conduction time of the converter switches to force the ac current to follow the waveform of the applied ac voltage. Passive PFC is the simplest and most straightforward method to eliminate input current harmonics. This is achieved by using passive reactive elements either at the input or at the output side of input rectifier employed in the design of AC-Converter. Advantages of this method are high efficiency, low EMI and simple implementation. However, the main drawbacks particularly at the low frequency are the size, weight and cost. AC-DC power converters are required to operate with high power factor (PF) and low total harmonic distortion (THD) for improved grid quality and full capacity utilization of the transmission lines.

Passive PF correction (PFC) circuits consist of inductive and capacitive filters followed by a diode bridge provide the simplest way of achieving high PF with high efficiency; however, they require low line frequency filters which are bulky and heavy. In order to operate at high frequency and reduce the size of the circuit, high frequency two-stage active PFC converters have been proposed. In this architecture, a front-end ac/dc PFC converter is operated with a switching frequency in the order of tenths to several hundred kHz for converters with Si semiconductor devices, and from several hundreds of kHz to tenths of MHz with wide-band gap devices, to shape the input current close to sinusoidal waveform in phase with the grid voltage. The second stage dc/dc converter provides the galvanic isolation and output voltage regulation. The controllers of the two stages are completely independent. The flexibility in control allows optimizing power stages, fast output voltage regulation and operating with high PF and low THD. However, this method comes with the expense of more components and larger size. Moreover, the constant switching losses such as parasitic capacitance losses associated with power switches reduce the efficiency of the converter at light loadcondition.A cost-effective approach to reduce the number of switches is to use single-stage ac/dc converters. In single-stage PFC converters, the front-end PFC stage and dc/dc stages are integrated and their operations are performed in a single-stage, basically, by sharing some of the switches and control scheme. An energy storage unit, capacitor or inductor, is located in between two stages, acting as a power buffer and providing sufficient hold up time. Numerous PFC ac/dc single-stage topologies have been proposed in literature, particularly, operating in discontinuous conduction mode (DCM) for simple yet effective PFcontrol.Majority of the proposed single-stage converters are proposed for low-power applications, where a fly back or forward converter derived topologies are used to achieve input current shaping and output voltage regulation. These converters offer cost-effective solution for low-power applications; however, they suffer from excessive voltage/current stresses on the switches, and are suitable for power levels lower than 200 W.

For medium to high power applications, the research efforts have focused on ac/dc single-stage full-bridge (SSFB) converters. Current-fed SSFB converters deploy a current shaping inductor connected to the input of the diode-bridge achieving high PF.However, due to the lack of dc bus capacitor on the primary side of the transformer, the dc bus voltage is subjected to excessive overshoots and ringing. Furthermore, the output voltage contains high amplitude second-order harmonic oscillating with twice the line frequency, which restricts their operation. Voltage-fed SSFB converters do not exhibit the drawbacks of current-fed SSFB converters, where a large capacitors located on the primary side dc bus. However, the dcbus voltage remains unregulated and it can be excessive at light load condition, as both input current shaping and output regulation are achieved with a single controller. In the literature, resonant converters adopting variable switching frequency have been proposed. In these converters, it is difficult to tune the resonant tank components over a wide load range, and optimize EMI filter. In majority of these aforementioned converters, the output current ripple becomes very large and the converter operation may transit to DCM mode. In two-level SSFB converters, the switches are exposed tohigh voltage stresses; thus, dc-link voltage is typically set close to 400V.In multilevel configurations, the voltage stresses acrossthe switches are significantly reduced. Quite recently, single stage three-level (SSTL) converters have been studied, which allow a flexible dc-link voltage in the rangeof 400 to 800 V. In a resonant SSTL converter is proposed to alleviate the drawbacks associated with SSFB converters, while reducing the voltage stress on the switches. In a recent publication a three-level converter is integrated withthe PFC boost stage by sharing the bottom switch. It is aimedto decouple the dc bus voltage and output voltage controllers,while the input current is adjusted with a constant duty cyclein DCM mode. The duty cycle of the bottom switch shapes theinput current as well as is used to transfer energy from dc busto output, simultaneously. The required duty cycle is the sum ofthe values achieved from individual PI controllers. The output voltage regulator sets the base duty cycle, while the PI controller of dc bus voltage regulator extends the duty cycle for the bottom switch. This topology alleviates most of the problems associatedwith SSFB converters, operated at constant switching frequency with a flexible dc-link voltage.

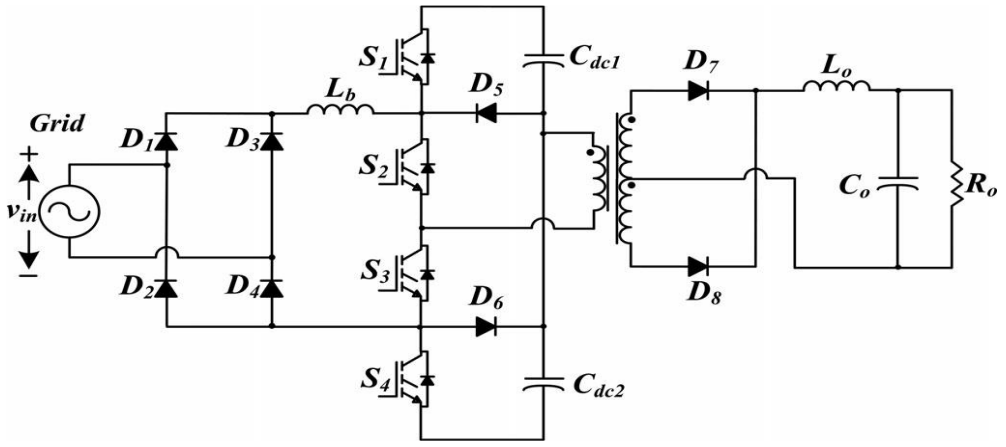

Fig.1 Proposed three-level single-stage PFC ac–dc converter

II. THREE-LEVEL SINGLE-STAGE PFC CONVERTER

Voltage-fed, single-stage power factor correction (SSPFC) full-bridge converters are attractive because they costless than two-stage converters, but their use has been limited because of the drawbacks that they have. Most of these drawbacks are because they are controlled by a single controller that regulates the output voltage so that the dc bus voltages left unregulated. As a result, the primary-side dc bus voltage of these converters may become excessive under high-inputlineand low-output-load conditions. Measures can be taken to limit the dc bus voltage so that does not become excessive, but these measures affect the performance of voltage-fed, SSPFC full-bridge converters in several ways. The input power factor of a single-stage voltage-fed SSPFC converter is not as high as that of current-fed converters. The output inductor current of a single-stage voltage-fed SSPFC converter is discontinuous for all operation conditions, which results in higher secondary-side component peak current stresses. The performance of voltage-fed, SSPFC full-bridge converters cans be improved if the limit on the dc bus voltage (typically < 450 V) is relaxed. This is not something that can be done for SSPFCfull-bridge converters that are based on two-level topologies, but this can be done for converters that are based on threelevel,multilevel topologies as the primary-side switching devices of these converters are exposed to half the peak voltage stress that those of two-level converters are. As a result, the dc bus voltage limit can be doubled for multilevel converters, but the peak voltage stress of the switches is the same as that of two-level type topologies.

In this chapter, a new AC-DCSSPFC PWM multilevel converter is proposed. The basic operation of the converter is explained as are the various modes of operation that the converter goes through during a switching cycle. The steady-state characteristics of the converter are determined by mathematical analysis and are used to develop a procedure for the design of key converter components. The proposed converter is essentially an integrated version of a boost PFC circuit and three-level isolated dc–dc converter. Basically, a diode bridge and an inductor are added to the three level isolated dc–dc converter topology. Here, the inductor is charged when S2 and S3 are turned on simultaneously. Body diodes of S1 and S4 serve as the boost diode of the PFC boost converter. At the same time, S1 to S4 are switched to apply *V*dc/2,−*V*dc/2, and zero voltage across the primary side of the transformer. Thus, all of the switches are shared between the two-stages, which makes it fully integrated single-stage converter without any additional auxiliary switch

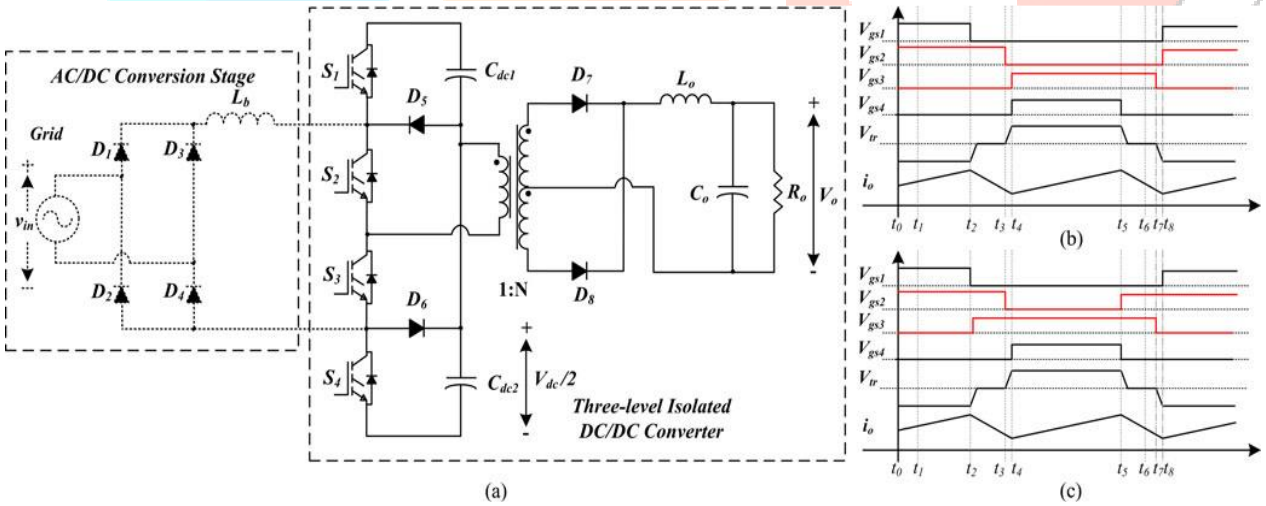

Fig.2 the proposed single-stage PFC converter (a) topology, (b) switching scheme of the conventional three-level dc/dc converter, and (c) modified switching scheme.

Switching scheme of the conventional three-level isolated dc/dc converter is given in Fig. (b). In this conventional scheme, the duty ratios of S2 and S3 are fixed close to 50% for simplicity in control and to ensure upper or lower three switches are not turned ON simultaneously as this would cause short-circuit through dc-link capacitors. Overlapping these two signals, as long as short-circuit condition is avoided, has no impact on the operation of the circuit. Similar to that in the conventional scheme, zero voltage is applied across the primary side of the transformer. This modified switching scheme is presented in Fig. (c). When a boost inductor and a diode bridge is added to the nodes as in Fig. (a), the overlap of gate signals of S2 and S3 enables applying input voltage across the boost inductor

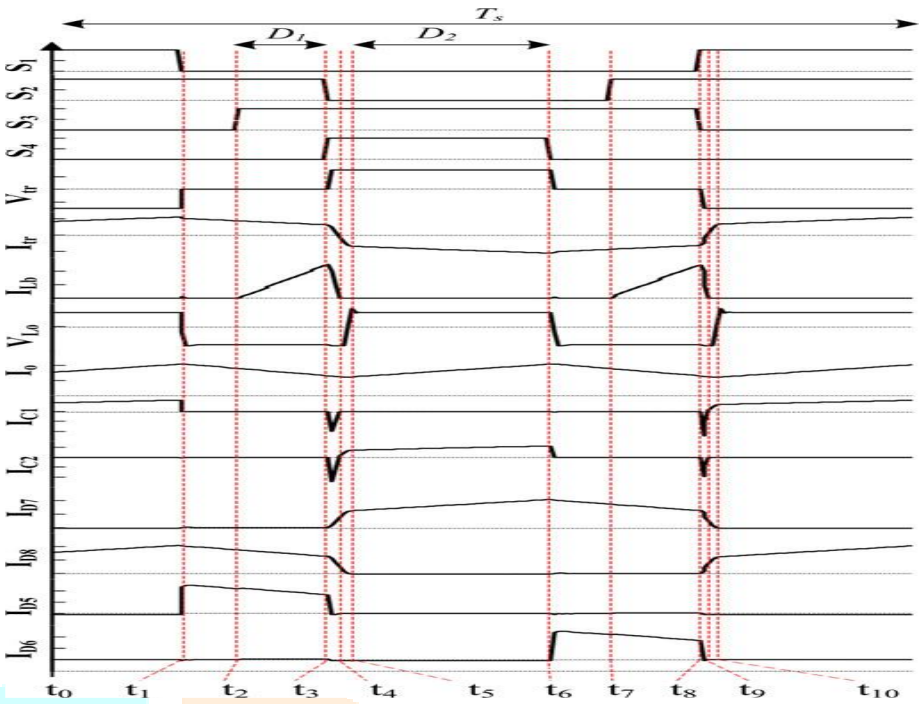

Fig.3 switching scheme of the proposed integrated three-level ac–dc converter

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The switching scheme of the converter is given in figure. The switches S2–S3 , and S1–S4 have 180° phase shift with respect to each other. The duty ratios of S2–S3 should be greater than 0.5 such that two signals overlap. Here, the circuit isexplained considering that input inductor current is discontinuous and the switching scheme is as follows; S1 is turned on right after S3 is turned OFF, and similarly, S4 is turned on when S2 is turned OFF. A dead-time should be inserted in between the turning ON instant of S1 and turning OFF instant of S3, and likewise between switching of S2 and S4 to avoid short-circuit.

III. Operation Mode

The operation modes of the circuits are explained in this section.

Mode 1 [t0 < t < t1]:

In this mode, both S1 and S2 are on. The upper capacitor, *C*dc1, discharges to the load by applying −*V*dc/2 to the primary side of the transformer. The primary side current increases linearly under constant voltage. *D*8 conducts at the secondary side of the transformer. The voltage across the output inductor is *V*Lo = *V*dc/2*N* − *Vo* .

In this mode, the boost inductor, *Lb* , does not interfere to the operation of the circuit.During this mode1, switches S1 and S2 are ON and energy from the dc-link capacitor *C*1 flows tothe output load. Since the auxiliary winding generates a voltage that is equal to the total dc-link capacitor voltage (sum of*C*1 and *C*2), the voltage across the auxiliary inductor is the rectified supply voltage. This allows energy to flow from the acmains into the auxiliary inductor during this mode.

Mode 2 [t1 < t < t2]:

At *t* = *t*1, S1 is turned OFF and S2 is kept on. The current in the leakage inductance conducts *D*5 and the primary side current freewheels; hence, zero voltage is applied across the primary side of the transformer. The output inductor voltage is equal to −*Vo* . The output inductor current decreases linearly.S1 is OFF and S2 is ON during this mode 2, shown in Fig 4. The energy stored in *L*in during the previous mode iscompletely transferred into the dc-link capacitor. The amount of stored energy in the auxiliary inductor depends upon therectified supply voltage. This mode is a freewheeling mode as the primary current freewheels through S2 and*D*1 and theoutput inductor current freewheels through both secondary diodes. This mode ends when the current in *L*in, *i*Laux, reacheszero.

Mode 3 [t2 < t < t3]:

At $t = t2$, S3 is turned on, while S2 still remains on. The primary current continuous to freewheel and zero voltage is applied across the primary side; hence, the output inductor current continuous to decrease under output voltage. Meantime, Vin is applied across Lb , and input current increases lin

Mode 4 [t3 < t < t5]:

In the beginning of this mode, S2 is turned OFF, S4 is turned ON, while S3 is kept on. Within this time interval, the following two operations are completed. The energy stored in the input inductor is transferred to the dc-link capacitors. The inductor current decreases linearly under Vin $-V$dc. Meantime, Vdc/2 is applied across the primary side of the transformer. The current in the leakage inductance is transferred to Cdc2. This causes the output current to commute from $D8$ to $D7$. At the end of this time interval, the energy in the input inductor is completely transferred to the dc-link capacitors and the commutation of the output diodes is completed. Depending on the dc bus voltage, and input current, one of these operations ends earlier than the other one. In this case, the energy stored in Lb is transferred to the dc-link at $t = t5$. Then, the current commutation from $D8$ to $D7$ is completed at $t = t6$.

Mode 5 [t5 < t < t6]:

Cdc2 discharges over to the load and Vdc/2 is applied across the primary side of the transformer. Thevoltage across the output inductor is VLo = Vdc/2$N - Vo$. The input current remains at zero in DCM mode. This mode is the same as Mode 1 except that S3 and S4 are ON and energy flows from capacitor $C2$ into the load.

Mode 6 [t6 < t < t7]:

At $t = t6$, S4 is turned OFF, and only S3 is on. This allows leakage current to freewheel through $D6$, and zero voltage is applied to the primary side. The output current decreases linearly under $-Vo$ .This mode is the same as Mode 2 except that S3 is ON.

Mode 7 [t7 < t < t8]:

At $t = t7$, S2 is turned ON. The energy from the input is stored in the inductor. This is similar to Mode 3, except that this time the primary side current is opposite to that in Mode 3 and freewheels through $D6$.

Mode 8 [t8 < t < t10]:

At the beginning of this interval, S3 is turned OFF, S1 is turned ON, and S2 remains ON. This mode is similar to Mode 4, where the stored energy in the inductor is transferred to the dc bus capacitors, and $-V$dc/2 is applied to the primary windings. In the meantime, the output inductor current commutates from $D7$ to $D8$.

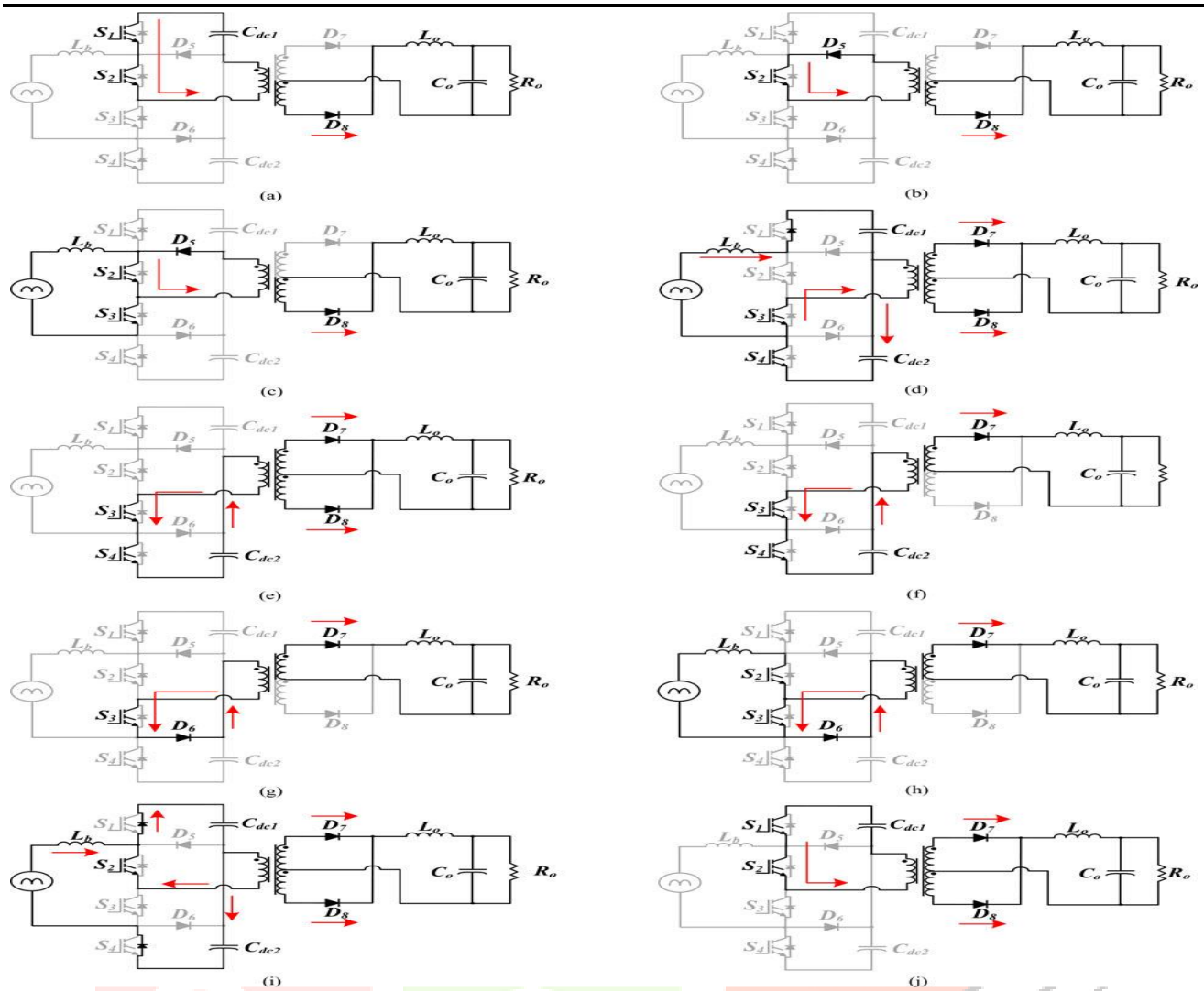

Fig. 4. Operation modes of the converter. (a) Mode 1: $t0 < t < t1$. (b) Mode 2: $t1 < t < t2$. (c) Mode 3: $t2 < t < t3$. (d) Mode 4: $t3 < t < t4$. (e) Mode 4: $t4 < t < t5$. (f) Mode 5: $t5 < t < t6$. (g) Mode 6: $t6 < t < t7$. (h) Mode 7: $t7 < t < t8$. (i) Mode 8: $t8 < t < t9$. (j) Mode 8: $t9 < t < t10$

IV SIMULATION AND RESULTS

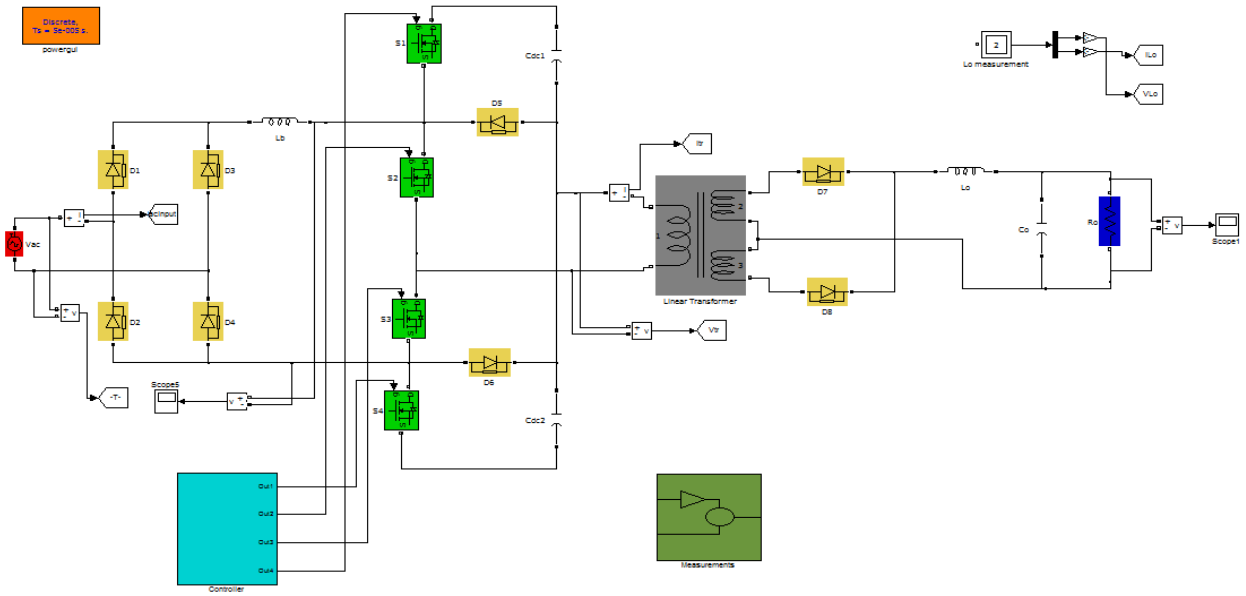

Fig 5 SINGLE STAGE THREE LEVEL ISOLATED AC/DC PFC CONVERTER

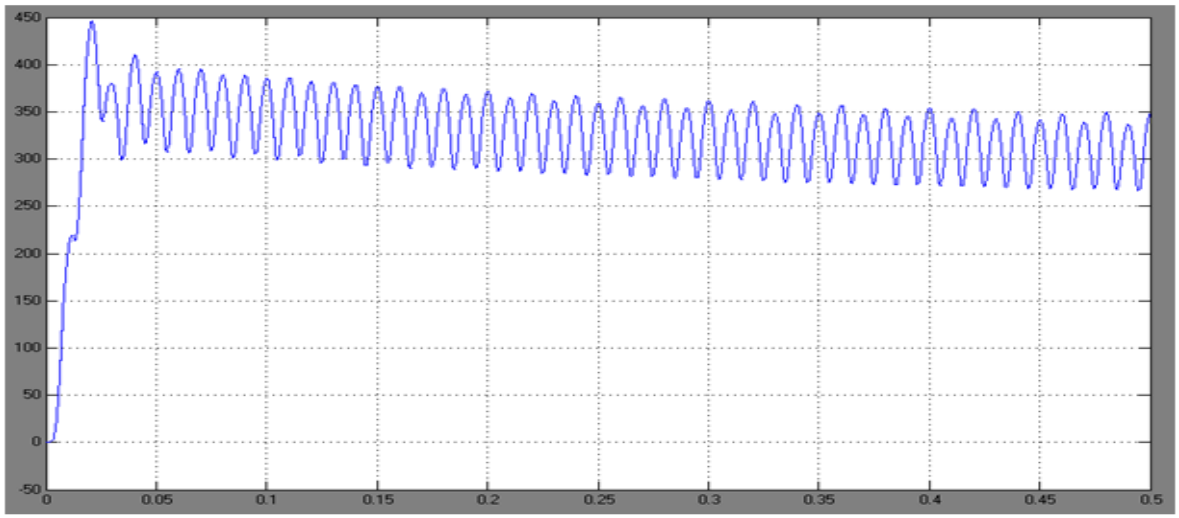

Fig 6 DC voltage for resistive load

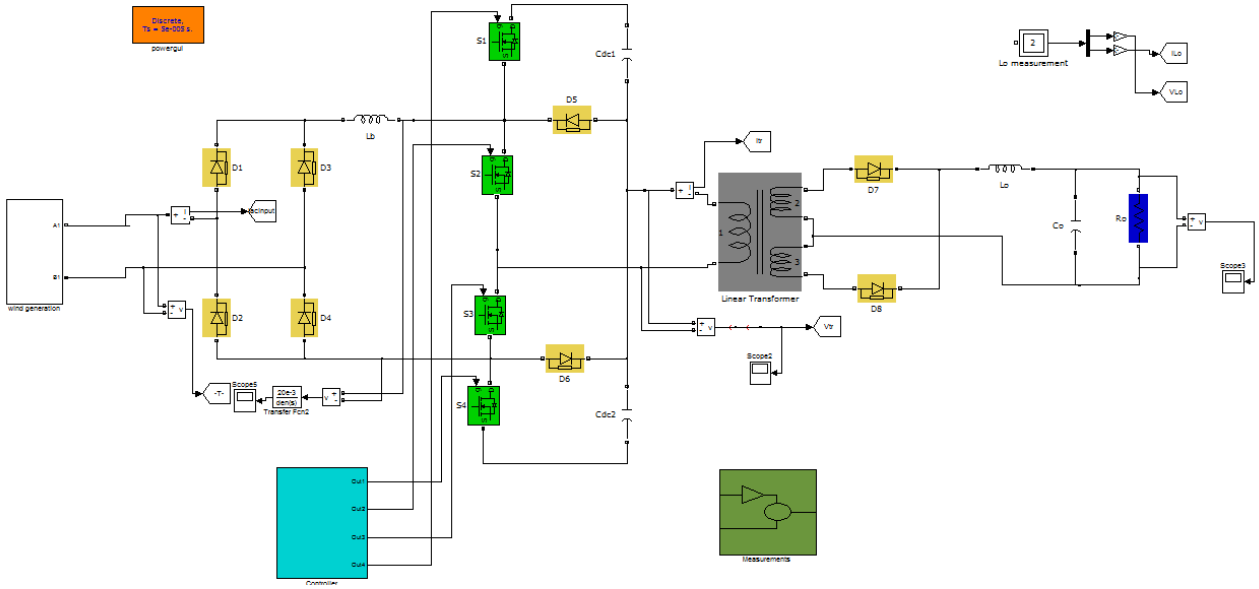

Fig 7 Single stage three level isolated ac/dc pfc converter with turbine modeling

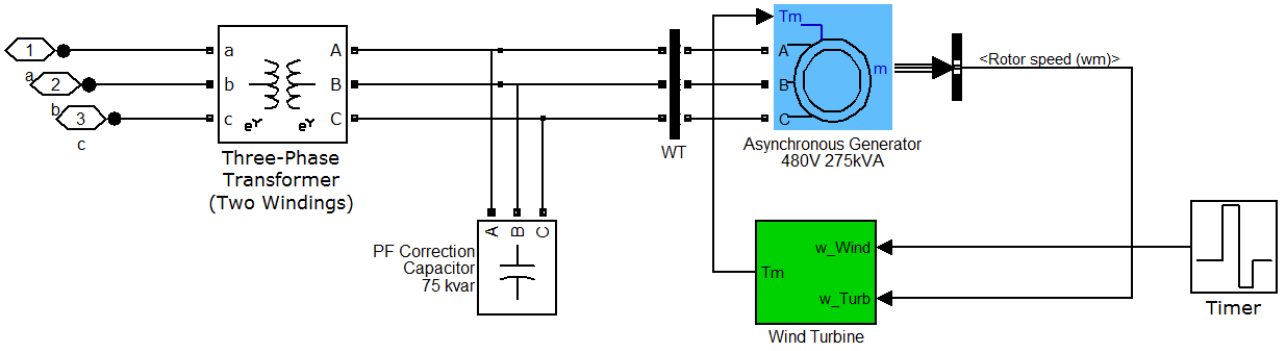

Fig 8 dc output with wind turbine

V.CONCLUSION

In this paper, a three-level single-stage PFC ac/dc converter is proposed for low-power applications. The proposed converter exhibits high PF with less number of switches/diodes, operated at constant duty ratio. A PFC inductor and a diode bridge are added to the conventional three-level isolated dc/dc converter, while the switching scheme is modified to be compatible with single-stage operation. The input current ripple frequency is twice of the switching frequency contributing to using smaller PFC inductor. Two independent controllers, in favor of shaping the input current and regulating the output voltage, are adopted which simplifies the design and control of the circuit. The tradeoff between the PF and overall efficiency in the case of adopting a variable dc-link voltage is analyzed through developed loss model.

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