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A Comparative Study and Analysis of Different CMOS VLSI Technology used for SRAM

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***Abstract*—This paper presents a comparative study and analysis between Various Nano meter CMOS technology used to implement the Radiated Hardened 14T-SRAM. The technology used in this paper include 65-nm, 28-nm, 22nm and 16nm technology.**

In order to design and Implement of 14T-SRAM that is used for Space applications, a precise CMOS technology and speed, power and area has been considered.

A comparison has been made on basis of the CMOS technology, Area and Power between the simulation results. Comparison of these models have been made with proposed design CMOS Technology.

***Keywords*—CMOS, Power, Area, Technology, Radiation Hard By Design (RHBD)**

I. INTRODUCTION

Radiation Hard By Design(RHBD) memories[7] are used in space borne ASICs for various on board applications like payload control, data getting, progressed correspondence, etc RHBD Application IC involved various modules like chip place, coprocessors, periphery modules, SRAM, straightforward modules and various kinds of I/Os. Radiation Hard By Design base cell libraries and Intellectual property for on chip capricious memories have been developed, yet RHBD Non-precarious memory IP is at this point not open locally.

A radiation solidified capacity gadget having static irregular access memory cells incorporates dynamic entryway disengagement structures set sequential with oxide seclusion districts between the dynamic locales of a memory cell exhibit. The dynamic [5] entryway separation structure incorporates a door oxide and polycrystalline silicon entryway layer electrically coupled to a stockpile terminal prompting an exuberant entryway confinement structure that thwarts a conductive channel stretching out from contiguous dynamic areas from framing. The door oxide of the dynamic entryway segregation structures is relatively meager contrasted with the conventional oxide seclusion locales and subsequently, will be less helpless against any unfavorable impact from caught charges brought about by radiation openness.

Semiconductor memory gadgets utilized in Outer Space, for model, in a Satellite, are Subjected to Severe natural conditions that may bargain the honesty of the Stored information, or prompt the memory gadgets to fizzle. By and large, the memory gadgets are essential for a bigger implanted System, where the memory gadget is only one of numerous gadgets.Having a similar bite the dust. The honesty of the memory gadgets utilized in space applications

is basic in light of the fact that the data Stored by the memory gadgets might be identified with basic capacities, Such as direction, situating, and transmitting and accepting information from a ground base Station.

Moreover, Semiconductor memory gadgets for use in Space applications ought to stay useful for the lifetime of the Satellite, which might be up to Several years. Differentiation this with applications where the memory gadgets are likewise Subjected to unforgiving working conditions, Such as direction Systems in rockets, however just for a moderately short time span.

Various studies have been focused on characterization of circuit- and layout-level optimization design and different approach to design of SRAM such as interleaving ,stacked approach etc. Few of the mathematical simulation models in VLSI CMOS technology has been formed and correspondence relevant results have been shown in following studies.

II. SYSTEM DESCRIPTION

In a recent technology, SRAM is defenseless to the high energy particles under cruel radiation conditions with more storage area and creating soft error rate in SRAM cell, and it's creating sensitivity with latching single Occurred upset (SOU) and single event transient (SET) and thus it's taken more power consumptions and more noise margin.

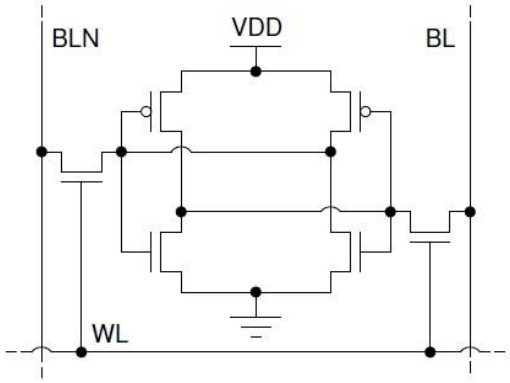

Fig.1 6T SRAM CMOS

III. DIFFERENT TYPES OF SRAM AND TECHNOLOGY

A low force SRAM [2] cell might be planned by utilizing cross-coupled CMOS inverters. The main benefit of this circuit geography is that the static force dispersal is minuscule; basically, it is restricted by little spillage current. Different benefits of this plan are high commotion resistance because of bigger clamor edges, and the capacity to work at lower power supply voltage.

To develop a precise equivalent circuit for Radiated hardened SRAM, Area, Power and space utilization has to be considered properly. This paper shows the different methods to achieve the Radiated hardened SRAM's implementation as described in the following Content.

A. RSP-14T SRAM CELL (65nm CMOS Technology)

The Working theory of the RSP 14T SRAM is expressed as follows 1) write Theory 2) Peruse Theory 3) Hold Activity theory.

In the compose activity, the piece lines BLB and BL are set to "1" and "0" expecting the Que B = "0" and Que="1".Exactly when the Write bit is impelled, the worth set aside in Que and Que B will be changed to "0" and "1," independently. The CMOS EN4 and EN5 are turned on, BLB(bit line) will be delivered When Picked Write bit is completely Engaged. The sense intensifier creates the difference voltage between Bit lines and it is consequently escalated. During hold Activities write bit is disabled and in this way the limit center points are kept from the BLs; thusly, they keep up the main instrument of hidden state.

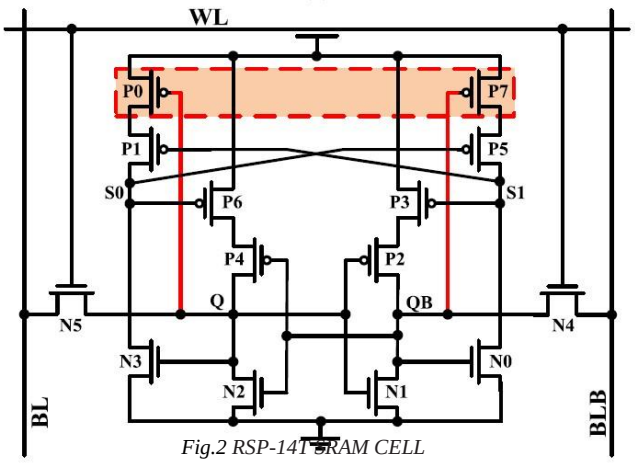

Fig.2 RSP-14T SRAM CELL

It clarifies, semiconductors, for example, one PMOS P0 and one PMOS P7 are wont to control the affiliation or threshold cutoff between the workplace supply and semiconductors PI by PV, which is useful to redesign the create speed and power use differentiated and Radiated Hardened-12T. Make sure that , selected template is used for the SRAM application device and should be in some standard format paper size of A4.

B. ILS-14T SRAM cell.(28nm,22nm and 16nm CMOS Technology)

The Block Circuit diagram for the ILS-14T SRAM cell is shown in Fig.3. PMOS and NMOS from M9 to M12, all these Mosfets are under managed by write word lines (WWLB and WWL). Joint write bit lines (WBL and WBLB), and storage nodes Que(Q), Que(QB), PB & P. Mosfets M13 and M14 connect the ground (GND) and therefore the read bitline (RBL) for read operation. M2, M9, M1, and M10 are transistors or Mosfets with high threshold voltage in order to realize area efficiency increased and improved reliability. The stacked Pmos and Nmos from M3 to M6 improve the Single event Upset Potential to withstand of the 14T cell. Data has been written in permanent storage nodes such as Que(Q), Que(QB), PB & P in the process of write operation, Hold operation proceeds and procides access to Mosfets from M9 to M12.They are turned off. If the Mosfets from M9 to M12 are powered on then Mosfets from M3 to M6 are Powered off. Starting of the Peruse operation, the read word line turns off M13 and RBL is changed to "1."After all the process Read Word Line activates M13 for Perusing operation.

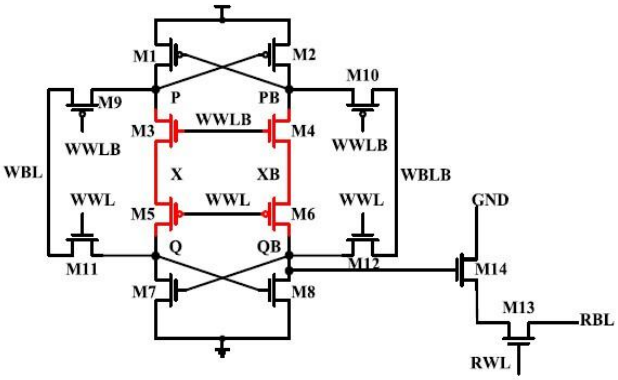

Fig.3 ILS-14T SRAM cell

C. Radiation Hardened 12T SRAM

The graphic diagram is shown in Fig. 4 and layout for the Radiated hardened 12T-SRAM cell is shown in Fig.5. The entrance semiconductors, Mos5 and Mos6, are associated with the piece lines (BL and BLB). The fixed memory cell comprises of eight NMOS semiconductors such as from Mosn1 to Mosn8 and four PMOS semiconductors Mosp1 from Mosp4. Semiconductor Mosfets Mosn7, Mosn5, Mosn6 and mosn8 are constrained by word line (WL). Subsequently. When Writing Word line WL_1 cell is in ON mode WL is se to 1, these semiconductors from Mosfets Mosn5 to Mosn8 are turned ON finally read along with compose tasks should be possible run.

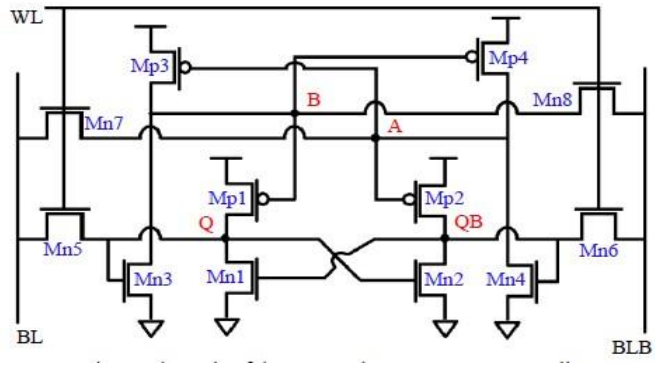

Fig.4 Radiated Hardned 12T SRAM

A tale energy productive and higher lenient SRAM cell in close to limit locale. The given 12T memory cell includes, a lower helplessness to Single occurred Upsets and more modest peruse and compose access time, and lesser zone when contrasted with the detailed SEU solidified memory cell.

Single occasion Upset is disturbed with lot of external factors in the space.one should taken care of the place where the Single occasion upset will be formed and resolution with efficient Testing.

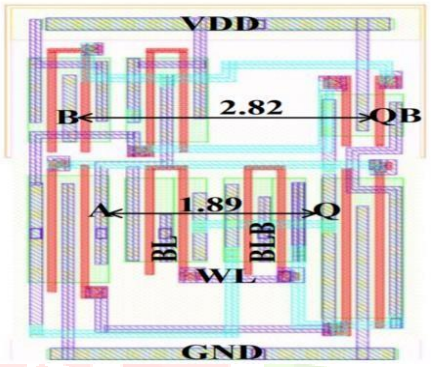

Fig.5 Layout of SEMNU hardened 12T-SRAM

D. Stacked SRAM-14T cell.(28nm,22nm and 16nm CMOS Technology)

Following Fig.3, estimations of RQ and RPB in ILS-14T gadgets are lower extreme situations where besides at 1 to 0 which gives immediate shocking results on 0.3V Supply Voltage. Stacked gadgets or semiconductors may be versatile to both 0–1 and1–0 bombshell. It implies that the 0 &1 agitated along with 1–0 furious about touchy hubs of the ILS-14T cell cause just little voltage transient at excess hubs. Quatro-based modular cells approach may be strong to Single occurred Events due to repetitive hubs. Anyway, only one out of every odd delicate hub of these cells is hearty at both 0–1 annoyed and 1–0 bombshell. As its interleaving stacked design shows improved execution at keeping voltage transient from proliferating to repetitive hubs, because of improved insusceptibility of both upset events of 0 & 1, its can be say that ILS-14T mosfet cell semiconductor is superior to its other Quatro-based and stacked cells because of the resentful and 1–0 irritated with VCC from 0.3 V and 0.9 VCC. The weaknesses of these Semiconductor cells are the degeneration of security integrity and also small basic charges in delicate hubs.

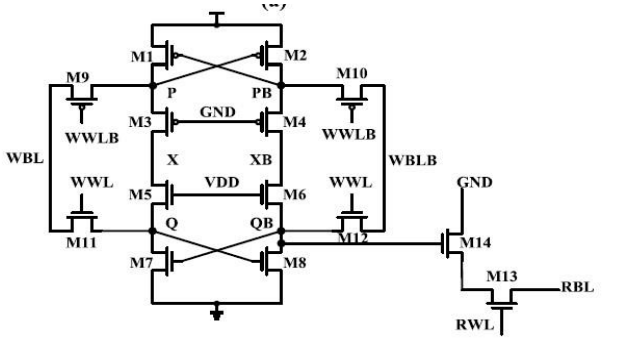

Fig.6 Stacked 14T-SRAM

IV. RESULTS OF SIMULATIONS AND ANALYSIS STUDY

After Studying the Simulation Results of all the devices with different technologies , here are the summarized the results with respect to the technology used ,area and Power is taken into the consideration.

The Simulations had been performed on different tools like Cadence Virtuous, Hspice, Tanner etc. Below are the some of the Technology study comparison for the tools used to simulate the SRAM Memory Cell. As CMOS innovation is downsizing, the customary memory cells are more defenseless to single occasion upset (SOU) unwavering quality test. This is a result of the diminishing stock voltage, diminishing basic charge and expanding densities.

A. Simulations Tool Comparison

FOM	**CMOS Technology**	**Simulation tool**	Power Consumed in nW
RHD 10T	65nm	TCAD	8.88
Stacked 10T	65nm	TCAD	6.64
12T SRAM	65nm	HSPICE	9.5
RSP-14T SRAM	65nm	TCAD	8.5
ILS-14T SRAM cell	28nm,22nm,16nm	Tanner	6.5
Stacked SRAM	28nm,22nm,16nm	Tanner	6.45

Power Consumption [1] for the Stacked and ILS 14t SRAM are much better with compared to all other design implementation.

B. AREA and RNM Comparison

FOM	Area without ECC	Area with SECDEC	Area with 3bit burst ECC in %	RNM @0.9V VDD in %	RNM @0.3V VDD in %
RHD 10T	NA	269%	341	No Info.	No Info.
Stacked 10T	NA	320%	406	100	131
12T SRAM	NA	269%	341	200	146
RSP-14T SRAM	NA	289%	494	92	98
ILS-14T SRAM cell	NA	494%	628	208	154
Stacked 14T-SRAM	334%	379%	481	200	154

After Seeing results of all different models for SRAM, RHBD 14-T SRAM is having more advantage in terms of Area without ECC and RNM @0.3VDD and @0.9VDD[3] .Stacked and Interleaving 14T SRAM are standout devices of memories which can be used for space research activities and also its optimized area provides an added advantages in reduction of usage of Sio2 wafer. So Preferably the highest CMOS technology as of now is to be consider the 16nm or lower CMOS technology to implement SRAM Memories

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