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EFFICIENT DRAINAGE MANAGEMENT SYSTEM FOR SMART CITY USING FPGA

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***Abstract*:** Drainage water management is the practice of using a water control structure in a main, sub main, or lateral drain to vary the depth of the drainage outlet. Drainage water management is the practice of raising the drainage outlet during times of the year when drainage is not needed or a higher water table could benefit the crop. Drainage water management allows producers to have more control over drainage. In this paper, we tried to build a project or system based on FPGA which is going to help drainage management for smart cities. As we have seen unless and otherwise drainage system is properly maintained the dream of Smart City remains as dream. Proposed system is prototype, implemented on Altera FPGA Development Board using VHDL.

Keywords - ***Drainage System, Smart City, FPGA, VHDL***

I. INTRODUCTION

The flow of water through well-defined channels is known as drainage and the network of such channels is known as drainage system. Since 21 century, the problem of lacking water resource has become the focus of concerning by more and more people. So, understanding the spatial distribution heterogeneity of water resources and spatial-temporal evolution rule is the emphasis of river basin management. The river basin has seen a renewed interest in recent years as a fundamental landscape unit for development planning and management. Living in an age of water scarcity makes all countries worry about something as simple as having enough water to grow sufficient food and fibre for their people. Efficient water use is the most economically and environmentally preferable solution, especially when there are signs for expected water drought and increasing competition over limited water supplies.

If drainage is not maintained properly the following problem may crop up:

1. Overflow of drainages leads to water flow on to roads, resulting diseases.
2. Overflow of drainages leads to stagnation of water on roads leading to damage of roads.
3. Damages roads bring hell to earth to those who suffer from back ache, pregnant women etc.
4. Damaged roads also lead to accidents less in day light and more in night.
5. If drainage system is not up to mark, investment on roads gets wasted.
6. Improper drainage system also leads to contamination of water, leading to water borne diseases.
7. Improper drainage system, flooding of roads lead to traffic jams resulting loss of valuable man hours, loss of revenue and employment.
8. Improper drainage system leads to dislocation and woes to population.

Removing storm water and household waste water is an important environmental health intervention for reducing diseases. Poorly drained storm water forms stagnant pools that provide breeding sites for disease vectors. Because of this, some diseases are more common in the wet season than the dry season. Household waste water may also contain pathogens that can pollute groundwater sources, increasing the risk of diseases such as lymphatic filariasis\. Poor drainage can lead to flooding, resulting in property loss, and people may even be forced to move to escape floodwater. Flooding may also damage water supply infrastructure and contaminate domestic water sources. So, the steps are required to be taken to maintain good drainage system. Some of the steps are as follows:

1. Silt in the drains should be cleaned regularly. If necessary, machines should be employed, the silt removing operation should aim at 0% overflow or leakage of drains.
2. Whenever drainage covers are arranged in the middle of the road, it should be strong work, wherein drainage manhole is very strong and filling around it is very strong. Passing of vehicles on it should not damage its construction.
3. Whenever new drainage connection is given to household the filling between drainage hole and residence where connection is given should be strong.
4. Steps to reduce rain water overflow both on roads as well as in drains.
5. Underground drainage system should be efficient and easily manageable.
6. Urban authorities should have proper control over the functioning; designing should help in reduction in maintenance.

II. RELATED WORK

Intelligent drainage system is developed by various researchers with help of embedded system design and sensors, which is further described below.

Aditya Dinesh Gupta et.al. [1] presents a review research that exhibits the current state-of the-art of the on-going SWT along with present challenges and future scope on the mentioned technologies. Nathila Anjum. G. et.al. [2] represents the implementation and design function of an underground drainage and manhole monitoring system (UDMS) for IOT applications. The proposed model provides a system of monitoring the water level and atmospheric temperature and pressure inside a manhole and to check whether a manhole lid is open, it also determines the level of harmful gases. G. Sunitha et.al. [3] designed where it can overcome these in an innovative and efficient way. This idea can be implemented for smart buildings, cities, colleges, hospitals, public spots and bus stand. A precautionary system is developed where this issue of sewage and dustbin overflow can be reduced by early sensing of increase in its level. The system design comprises of a sensor to sense the level, a controller to command, a communication network to register the complaints on blockage and continues increase in the level of sewage. L. Nikhil Sai et.al. [4] proposed system would track the level of water, flow of water and harmful gas in the sewage system. The range of values will be stored in the cloud storage, then analyzed. The status of drainage is will be sent as SMS through the Blynk server to near the corporate office. Then the corporation people will take appropriate action. Gaurang Sonawane et.al. [5] represents the application and design function of a smart and real-time Drainage and Manhole Monitoring System with the help of Internet of Things. The manholes present in the drainage will have a module which is having microcontroller interfaced with gas sensor, level indicator, NRF. The system will monitor if the blockage is occurred in between two manholes and also it will sense the rise in number of various gases which are harmful to the human beings, and also a system of monitoring the water level then it will trigger an alarm and will provide that information to the health departments from which the particular action will be taken. S. Ravichandran et.al. [6] describes a smart drainage management system. The drainage system describes the design and mechanism of locating the blockage and removing the same in the drainage system using internet of things. The manholes present in the drainage are having a module which is having microcontroller interfaced with gas sensor, level indicator, RFID. Whenever the level indicator identifies any blockage in between two manholes then it will trigger an alarm and inform the exact location to the user by highlighting different colour depending upon the distance from the blockage. Yan Pang et.al. [7] explores various machine learning techniques to model the nonlinear relationship between rainfall and drainage water level nearby and predict the water level with lead time up to 10 minutes in advance. Through the analysis, it is found that the Artificial Neural Network model is superior in modeling the nonlinear relationship during the training stage, while the Random Forest and SVM-radial models are robust and offer better accuracy in drainage water level prediction. V. Vani et.al. [8] presents with flow sensor and ultrasonic sensor which detects leakage and overflow respectively with the help of Wireless Sensor Network (WSN) which is based on ZigBee technology and Internet of Things (IOT) and an alert is sent through the mobile app to the authorities in Municipal Corporation prior overflow or any blockage to avoid leakage. Vikki Edmondson et.al. [9] presents the design and development of a prototype Smart Sewer Asset Information Model (SSAIM) for an existing sewerage network. The SSAIM, developed using Industry Foundation Class version 4 (IFC4) an open neutral data format for BIM, incorporates distributed smart sensors to enable real-time monitoring and reporting of sewer asset performance. Results describe an approach for sensor data analysis to facilitate the real-time prediction of flooding. R. Priya et.al. [10] proposed system has been developed for water supply management with sensor devices.

III. PROPOSED WORK

The generalized implementation of efficient drainage management system as shown in fig1. The system used number of sensors in a single node. As we can see we use sensors from sensor 1 to sensor n under a single node called node A. There are number of nodes used from node A to node m. The nodes are connected to FPGA kit.

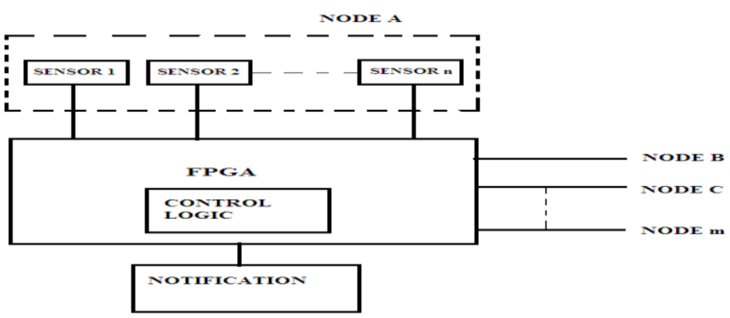

Fig 1: Proposed implementation block diagram

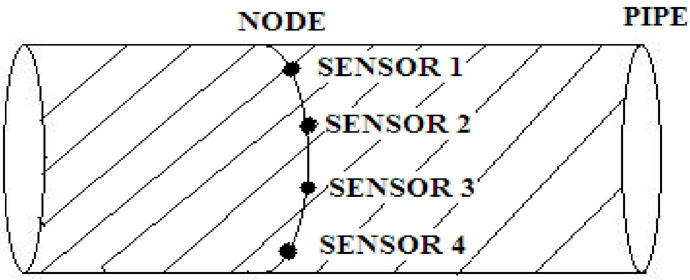

Fig 2: Prototype Implementation on drainage system

Figure 2 shows the prototype implementation on drainage system. As we can see a pipe carrying drainage water consists of nodes, having single node. We can use number of nodes in a single pipe. The node is carrying number of sensors. These sensors are connected in a cylindrical or a ring pattern in a pipe. As the water level increases it will be detected by sensors, sensors give input to FPGA logic, output will be display as notification.

The sensors are used to detect the water level in pipe. A sensor is an object whose purpose is to detect events or changes in its environment, and then provide a corresponding output. A sensor is a type of transducer, sensors may provide various types of output, but typically use electrical or optical signals. A sensor's sensitivity indicates how much the sensors output changes when the input quality being measured changes.

The FPGA is field programmable gate array is an integrated circuit designed to be configured by customer or a designer after manufacturing hence field programmable. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application specific integrated circuit (ASIC). FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

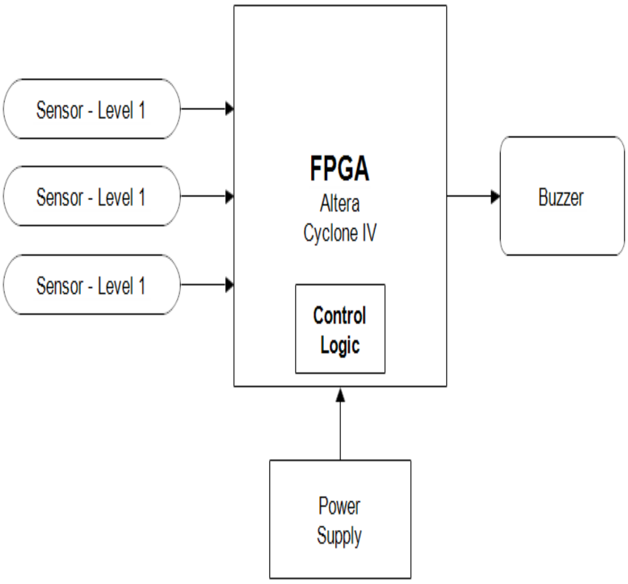

Fig: 3 FPGA Implementation Diagram

As specified earlier in this project we are building prototype for a single node for implementation of drainage monitoring as well as alert for different levels of drainage as shown in fig 3. Sensors used for detecting water level is as shown in fig 4. For implementing this approach, we are using the finite state machine. The fsm code is written in vhdl and analysed using two software platform –Modelsim and Altera which are detail explained in the chapter 4-system tools.

Water Level Sensor

The sensor has a series of ten exposed copper traces, five of which are power traces and five are sense traces. These traces are interlaced so that there is one sense trace between every two power traces. Usually, these traces are not connected but are bridged by water when submerged.

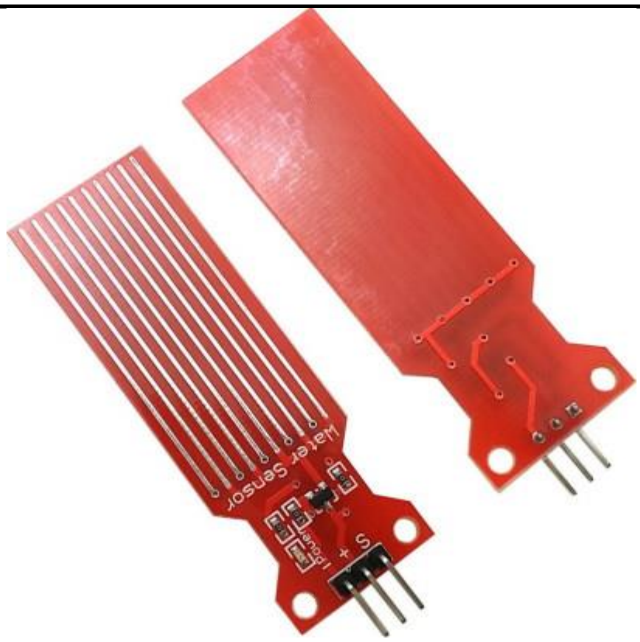

Fig: 4 Water Level Sensor used for prototype

The working of the water level sensor is pretty straightforward. The series of exposed parallel conductors, together acts as a variable resistor (just like a potentiometer) whose resistance varies according to the water level. The change in resistance corresponds to the distance from the top of the sensor to the surface of the water. The resistance is inversely proportional to the height of the water:

- The more water the sensor is immersed in, results in better conductivity and will result in a lower resistance.
- The less water the sensor is immersed in, results in poor conductivity and will result in a higher resistance.

The sensor produces an output voltage according to the resistance, which by measuring we can determine the water level.

5V Buzzer

Fig: 5 Buzzer for Notification

While writing the VHDL code of the FSM we should consider best synthesis. FPGA synthesis tool provides a variety of design constraints which essentially helps the designer to meet the design goal such as area and speed optimization to obtain the best implementation logic. This describes the implementation of FSM with single and multiple processes and the important aspects of synthesis optimization like resource sharing for area, speed, latency and power. At the synthesis level, the high-level description is converted into an optimized gate-level representation or RTL form. At this level of abstraction when global constraints of area or speed is set the synthesis tool will try to meet constraints, calculate cost of various implementation and try to generate best logic topology for given constraints, algorithm and target process. Normally synthesis tools use wire load models which statistically estimates the interconnect delay in the absence of physical layout data. For a wire delay with given fanout, the wire load model specifies the capacitance, resistance and area of the wire. Although the synthesis tool has complete control over the netlist, the resulting timing is greatly affected by the physical layout. The synthesis-based gate-level optimizations will include constraints like Finite State Encoding (FSM) algorithm (like auto, one-hot, compact, sequential, gray, Johnson, speed1), hierarchy setting (which allows MAP's physical synthesis options to optimize across hierarchical boundaries), logic duplication (avoids replication of logic), FSM style, register duplication and so on. By setting the required constraints the design can be optimized. As a general rule faster design requires parallelism at the expense of slice area, and minimize area design requires less logical depth. The issues in optimization of synthesis tool in sequential logic which is elucidated by the design of Finite State Machine (FSM) with different encoding algorithm constraints like gray, one-hot, sequential, Johnson, speed1 and auto. Finite state machine is a restricted class of sequential circuits called synchronous circuits which assumes the existence of a common global clock. An FSM is a discrete dynamic system that translates the sequence of input vectors into sequence of output vectors. States in an FSM specification can be either symbolic or binary-encoded. To optimize the circuit at sequential level, state minimization and state assignment procedure are executed. State minimization reduces the redundant states and state assignment encodes the symbolic states into binary codes.

Finite State Machine (FSM)

A finite state machine has the general structure shown in Figure 3.

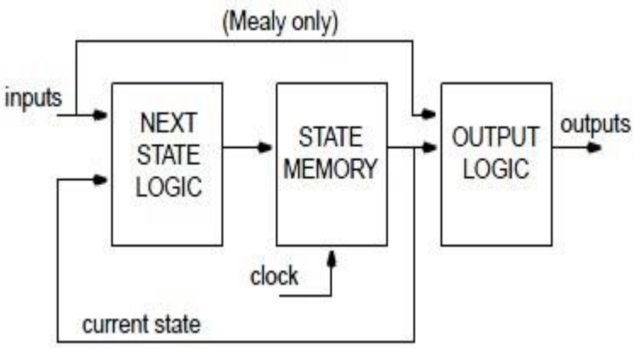

Fig 6 Finite State Machine

FSM is used to model a sequential logic circuit. A sequential logic circuit has three main parts:

1. Present state of the system
2. Next state logic
3. Output logic

The states of the system are represented by flip-flops (or registers). Both next state logic and output logic are entirely combinational logic. A simple block diagram for a state machine is shown in Fig. 6 which contains a Present State Logic section, Present State section, and an Output Logic section. The current state of the machine is stored in the state memory, a set of n flip-flops clocked by a single clock signal (hence "synchronous" state machine). The state vector (also current state or just state) is the value currently stored by the state memory. The next state of the machine is a function of the state vector and the inputs. Mealy outputs are a function of the state vector and the inputs while Moore outputs are a function of the state vector only.

FSM with VHDL

The logic in a state machine is described using a case statement or the equivalent (e.g., if-else). All possible combinations of current state and inputs are enumerated and the appropriate values are specified for next state and the outputs. A state machine may be coded as per Figure 1 using two separate case statements, or using only one. A single case statement may be preferred for Mealy machines where the outputs depend on the state transition rather than just the current state

One of the main advantages of implementing an FSM with VHDL is that we can directly derive the VHDL code from a state diagram (or an ASM diagram).

We will introduce a VHDL template to implement a state machine based on the model shown in Fig.6. You should use this template for your design.

The VHDL file will include 3 main sections:

1. Present State section:

- The function of this section is to assign the next state to the present state at the active clock edge.
- An asynchronous reset signal should be included to initialize the system to the default first state of the system.
- This section is implemented with sequential (behavioral) VHDL code with a PROCESS.

2. Next State Logic section:

- The function of this section is to establish the next state of the system.
- This section is implemented with behavioral (sequential) VHDL code with a PROCESS.

3. Output Logic section:

- The function of this section is to generate the outputs of the system.
- This section is implemented with concurrent VHDL code with conditional assignment statements.

IV. RESULTS AND DISCUSSION

Effective draining management system is implemented as prototype and description logic has been developed using VHDL, simulation is performed using Modelsim SE 6.3f software & synthesized using ALTERA Quartus II on Cyclone® IV EP4CE22F17C6N FPGA. Also same has been implanted on Altera FPGA DE0 Nano development board.

FPGA Board	DE0 Nano Development Board
FPGA Family	Cyclone IV
FPGA Device	EP4CE22F17C6N

Quartus II is a software tool developed by Altera/Intel Corporation for the synthesis and analysis of Hardware Descriptive Language (HDL) designs. It enables the synthesis of designs, timing analysis, Register Transfer Level (RTL) diagram examinations, and simulation as per different environments. The system is designed by VHDL using FSM (Finite State

Machine) logic which keeps a distance between the obstacle and vehicle to prevent collision. The VHDL is verified and simulated by a software tool called Modelsim.The flow of the project used in implementation is given in steps which is been followed to design the project.

Fig 7 shows the simulation of proposed system in which input is various level sensors attached to pipe for single node, similarly same can be implemented to other nodes also and output the level indication based on the notification in terms of alarm or LED is given. Table 1 shows the synthesis summary based on Altera Cyclone IV FPGA in terms of logic resources, power dissipation and total propagation time delay.

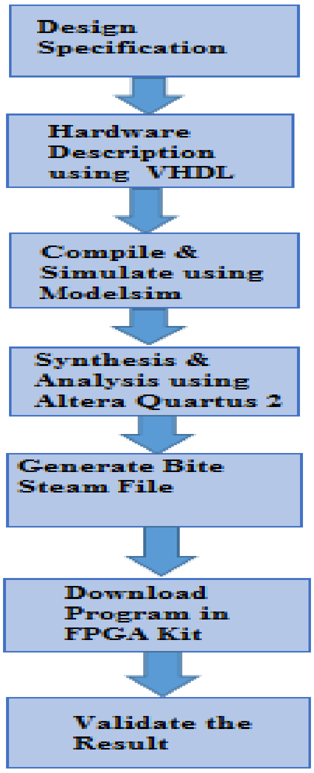

Fig 7: Design flow chart

Description:

It indicates how our project has been implemented. It gives the design flow of our project. First the design of our system is finalized and then its specification is defined. The design Specification of our hardware is defined by VHDL. VHDL convert the design into a software program. This program is then compiled and simulated using modelsim software. Further, it is analyzed and synthesized by xilinx software tool which generates a bit stream file. Finally, the generated bit stream file is then burned into FPGA kit.

Hardware Interfacing:

In our system, water sensor module is fitted to the pipe at different locations. The input of sensor is connected to FPGA IO pins. Also at output stage, we connected Buzzer to FPGA IO pins for alert notification. The output of different levels of sensors is shown on the LED whenever it receives a high or/and low signal. The on-board LED indicator helps user to check status of the sensor without using any additional hardware.

Simulation Results:

The simulation result of system is explained in terms of different cases. Here in this reset, level_sensor1, level_sensor2 and level_sensor3 are used as input signals, while led1, led2 and led3 and buzzer are used as output signals. When reset signal is assigned logic '1'then both the level_sensors are at logic '0' that is the sensors are not active thus all the led are at logic '0' as shown in fig 4. This indicates that when reset signal is high sensors are in active and system is not working and thus all led are inactive or OFF. Hence, reset signal should be at logic '0' in order system to work.

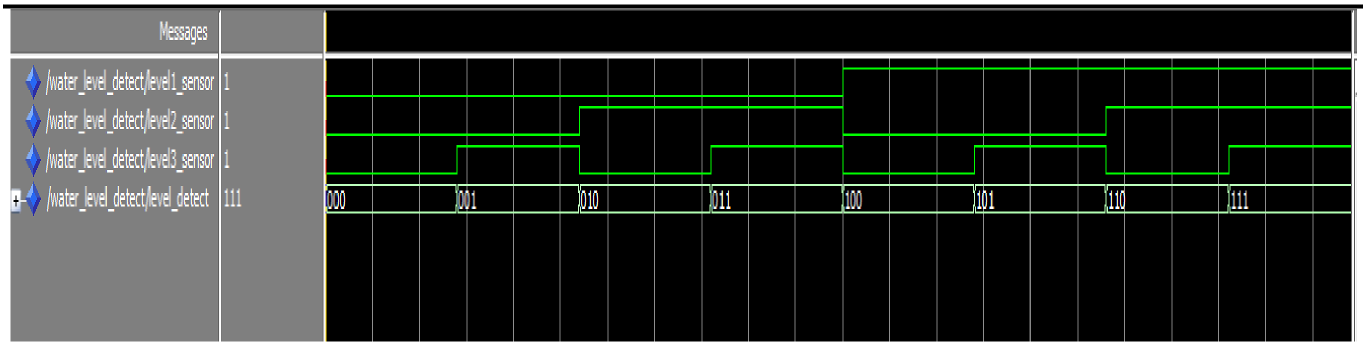

Fig 8: Simulation of proposed system

Now we will fix reset signal to logic '0' and observe the different conditions. However, output is provided by switching LEDS.

Hardware Analysis:

Proposed VHDL code is synthesized on ALTERA Cyclone IV using Quartus II software as per design flow mentioned above in fig 7.

Flow Summary

Flow Status	Successful - Thu May 27 10:46:31 2021
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	airport_cs
Top-level Entity Name	airport_cs
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Preliminary
Met timing requirements	N/A
Total logic elements	7 / 22,320 (< 1 %)
Total combinational functions	7 / 22,320 (< 1 %)
Dedicated logic registers	5 / 22,320 (< 1 %)
Total registers	5
Total pins	10 / 154 (6 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)

Fig 9: Device Utilization Summary

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Thu May 27 10:51:38 2021
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	airport_cs
Top-level Entity Name	airport_cs
Family	Cyclone IV E
Device	EP4CE22F17C6
Power Models	Preliminary
Total Thermal Power Dissipation	91.83 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	81.06 mW
I/O Thermal Power Dissipation	10.77 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig 10: Power Analysis Summary

Table 6.1: Parameters Summary

Parameters	Value
Total LE's	7
Min Propagation Delay	3.274 ns
Max Frequency	305MHz
Power Consumption	91.83 mW

Figure 11 shows the interfacing of prototype model with FPGA development board, and notification is displayed on LED for appropriate level is achieved.

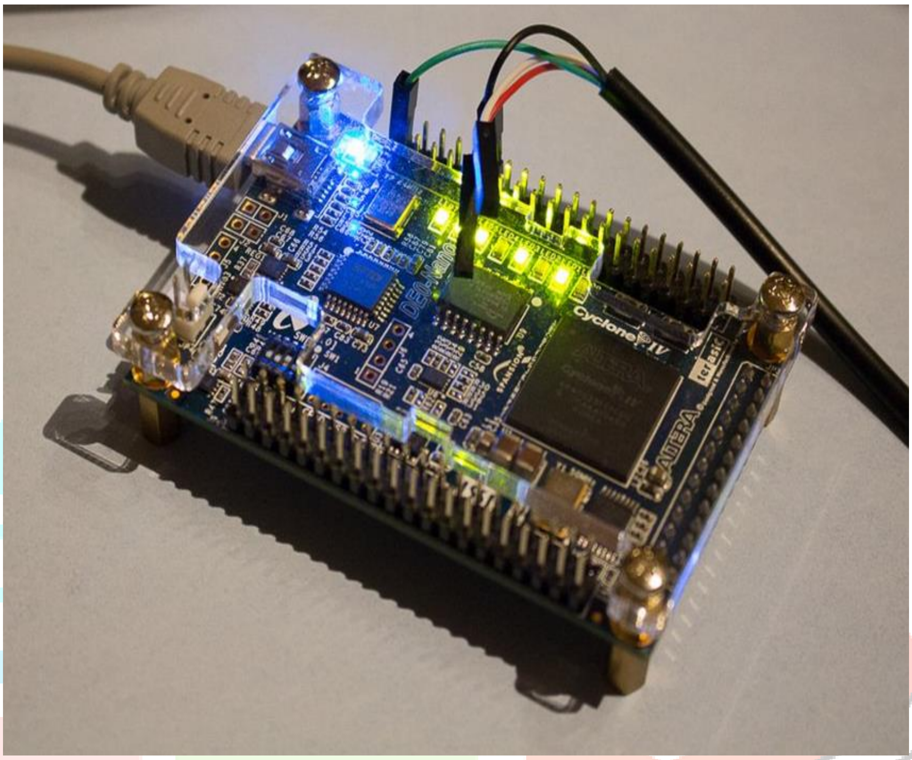

Fig 11: Interfacing with FPGA development board

V. Conclusion

Efficient drainage management systems are useful for making cities clean. The waste water or drainage water can be also provided to the farms using proper water purifying technique. Our project is prototype implementation for effective drainage management or monitoring system using FPGA. In this project, we simulate the VHDL code by using Modelsim software and waveforms is analyzed and code synthesis is performed by using DE0 NANO BOARD to get optimize solution. The prototype has given an alert regarding system on LED or Buzzer and show all levels to the control room for monitoring purpose. As such this project will contribute little bit towards national development. We can implement this prototype into SoC or ASIC.

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