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Verilog Implementation of ITU-R Standard BT.1120-8 High Definition Video Decoder

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Abstract*:* In this paper an implementation of BT 1120-8 using verilog is carried out. The priority includes working on Standard Definition signals and the video stream flows in BT-656.In this project decoding of high definition signals to be used for various applications is carried out. The incoming 8/10bit video is decoded into Y,Cm,Cin format and produces Horizontal Synchronization and Vertical Synchronization blanking plus along with the pixel clock. Even though many decoders are already available in market for the purpose of academic learning as well as to make efficient decoder , the present work is carried out.

Keyword:-
ITU-R(International Telecommunication Union Radio communication Sector) ,BT(Broadcasting service Television), SAV(Start of Active Video) , EAV (End of Active Video), Hsync(Horizontal Synchronization), Vsync(Vertical Synchronization **),**HDL(HardWareDescriptiveLanguage),HD(HighDefinition),Videocompression.

INTRODUCTION :-

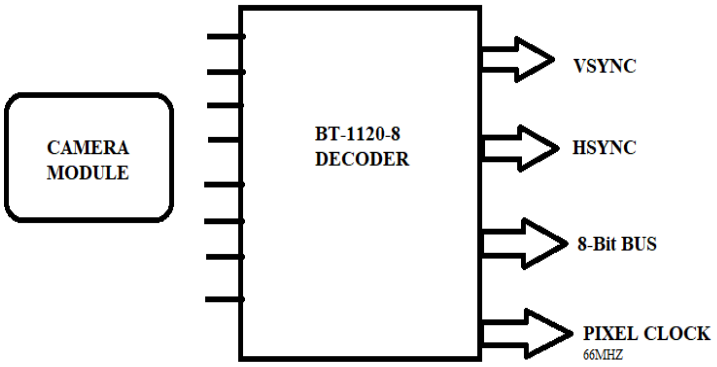
In this the role of ITU-R is to possess the rational, equitable, efficient use of frequency spectrum by all ITU-R communication services with together with Broad casting services. The video signal to be transported ought to meet with the characteristics as of BT-656. The digital interface may be a uni facial interconnection the information signals square measure reborn into binary format victimization associate encoder so the binary values square measure sent into BT-1120 decoder. eight bit video information can use a pair of LSBs of Zeros to create ten bit words. Y,Cbm,Cin signals square measure given with twenty bit information words by time multiplexing Cbm and Cbin components. Hsync and Vsync square measure drawn from the decoder wherever we are able to notice the quality Definition video .where it's a pulse that synchronizes the beginning of the horizontal image scan line within the Television with the image supply created in it , Vsync assures the monitor scan starts at the highest of the television at the proper time of video. Pixel aren't controlled by them in any respect .A element is that the smallest image unit which will be displayed .Imagine the screen may be a grid and every cell will contain one shade (or) colour, the picture consists of the many of them ,each sufficiently little that the human eye cannot distinguish them ,individual therefore it sees them 'blind' in to an image. within the unfold sheet analogy, every cell is one element, Hsync would mean begin at column zero& Vsync would mean begin at row zero . In associate 1060*1120pixel .In screen there are many elements that the time scan the full image would be the amount of 1 pixel multiplied by the quantity of pixels .That solely provides the time to attend on the 'visible a part of the image through it doesn't embody the time spent in synchronization pluses .Depending on begin timing to feature one vertical set pluse length

,Without knowing however long those set pluses last , cant tell you the full time . BT1120 can use embedded time codes, you only ought to flip them on. there's a register bit for that. Please seek for Ab Codes within the hardware guide. The Ab code block is employed to insert Ab codes into the video information stream. The insertion purpose for the Ab codes is planned by default and is adjusted mechanically to suit this video customary as per the PRIM_MODE[3:0] and VID_STD[5:0] settings. BT 1120 may be a digital video decoder with integrated colour-space convertor. It's perform is to extract the valid pixels from a BT.1120 video stream and convert them to eight bit for future process. Video coding begins once reset is de-asserted and on the rising-edge of clk once the video_val signal is declared high. (The signal video_val may be a clock-enable signal that permits the sampling and process of every input byte). Pixels square measure extracted from the BT.1120 input stream and reborn to 1080 format. These pixels square measure then bestowed at the output of the decoder along side field and set flags. All signals square measure synchronous with the input clock. The video output from the decoder follows an easy valid-ready streaming protocol that's common to all or any different Zip cores video scientific discipline. Output pixels and flags square measure sampled on a rising clock-edge once pixout_val and pixout_rdy square measure each high.

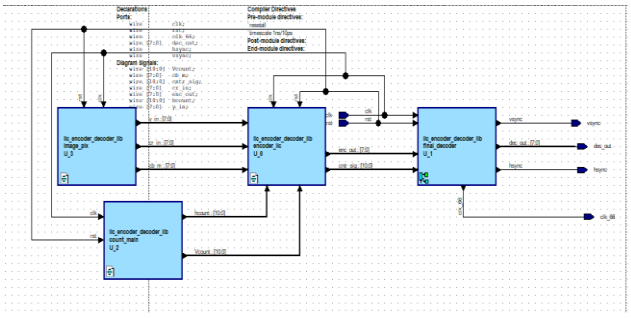
Soft ware Tool :-

Here we use HDL designer for designing the decoder and Mentor Graphics pe student edition for the simulation of the design HDL is a very often used software in the chip design industry where we can design any chips by simply taking the components need from the tool box and connected the wires digitally rather than writing the hole code as in the olden days we can produce state machines and work on them easily.

BLOCK DIAGRAM



In this block diagram we have sent an 8 bit data from the camera module to the decoder and the BT 1120 decoder will start working when RST goes to 0 and the 8 bit data is converting into a High definition video 8 bit bus with Hsync and Vysnc and a pixel clock is generated as the out of the decoder data. It is to enhance the video quality and resolution.



As the input we have given with a video data we have to first convert to binary data with the help of encoder and later on using the HDL tools we connect the output of the encoder that is 8 bit data to the decoder input as shown in the above figure where we convert video into binary data and out we get as

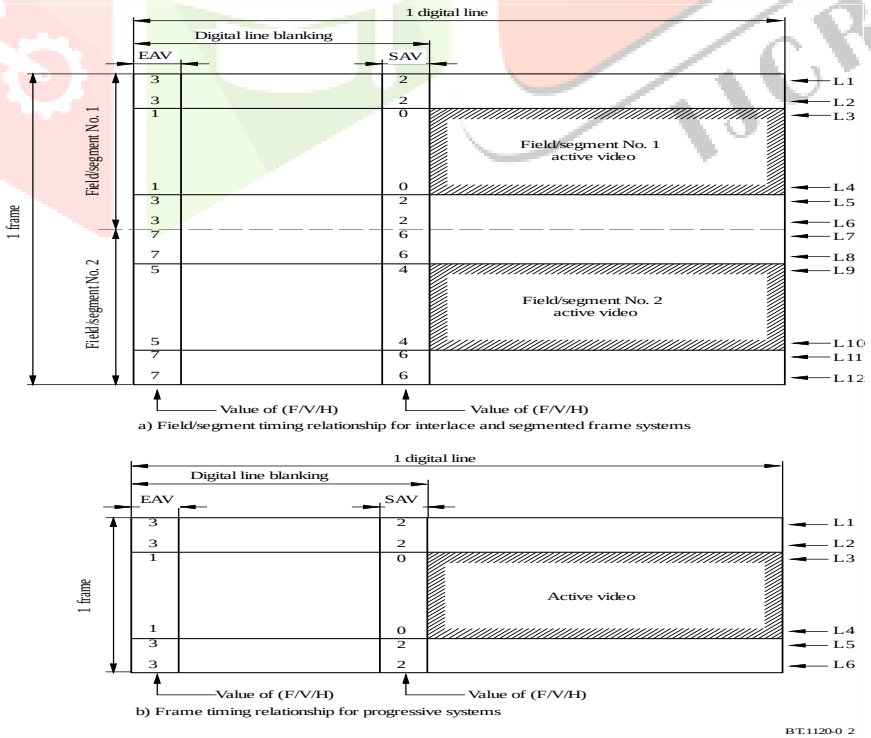
per the block diagram with the timing values and the field segment we have 1080 active lines to define the HD video data and we can find and decode the active data in between these 1080 active lines.

TABLE :- FIELD INTERVAL TIMING SPECIFICATION

Symbol	Definition	Interface digital line number
	Number of active lines	1 080
L1	First line of field No. 1	1
L2	Last line of digital field blanking No. 1	20
L3	First line of field No. 1 active video	21
L4	Last line of field No. 1 active video	560
L5	First line of digital field blanking No. 2	561
L6	Last line of field No. 1	563
L7	First line of field No. 2	564
L8	Last line of digital field blanking No. 2	583
L9	First line of field No. 2 active video	584
L10	Last line of field No. 2 active video	1 123
L11	First line of digital field blanking No. 1	1 124
L12	Last line of field No. 2	1 125

NOTE: – Digital field blanking No. 1 denotes the field blanking period that is prior to the active video of fieldNo. 1, and digital field blanking No. 2 denotes that prior to the active video of field No. 2.

Video timing Refernce Codes SAV and EAV



These are the timing reference values for where our video filed will begin and how the SAV and EAV are present with respective to the active video each video is enhanced frame by frame and the timing of the video digital lines start from L1 and last up to L12 where we will have all the blank video and active video from that we will extract the active video and enhance it by using the decoder.

Bit assignment for video timing reference codes

Word	Bit number									
	9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
First	1	1	1	1	1	1	1	1	1	1
Second	0	0	0	0	0	0	0	0	0	0
Third	0	0	0	0	0	0	0	0	0	0
Fourth	1	F	V	H	P_3	P_2	P_1	P_0	0	0
Interlaced andsegmented framesystem	F = 1 during field/segment No. 2 = 0 during field/segment No. 1			V= 1 during field/segment blanking = 0 elsewhere				H= 1 in EAV = 0 in SAV		
Progressive system	F=0			V = 1 during frame blanking = 0 elsewhere				H= 1 in EAV = 0 in SAV		

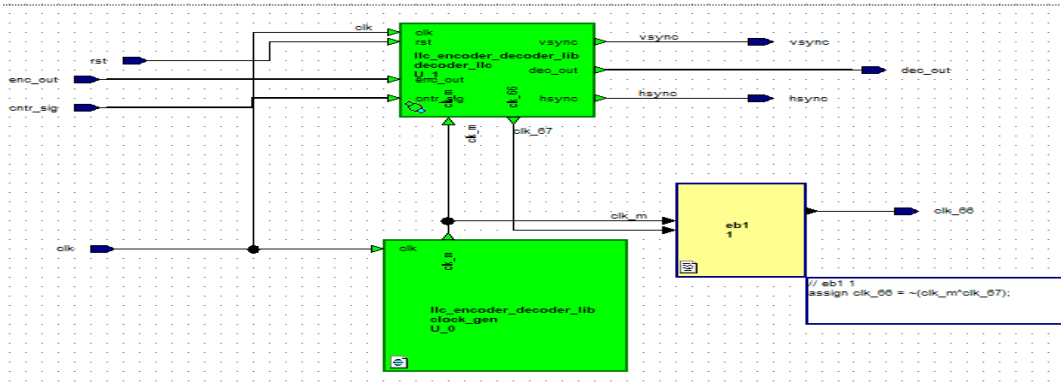
These are the bits that are protected for the video timing where every field is interlaced frame by frame here P_0, P_1, P_2, P_3 in the fourth word are the protection bits see the below protection bits table for these.

TABLE II: Protection bits for SAV and EAV

	SAV/EAV bit status			Protection bits					
Bit 9 (fixed)	8 (F)	7 (V)	6 (H)	5 (P_3)	4 (P_2)	3 (P_1)	2 (P_0)	1 (fixed)	0 (fixed)
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	0	0
1	0	1	0	1	0	1	1	0	0
1	0	1	1	0	1	1	0	0	0
1	1	0	0	0	1	1	1	0	0
1	1	0	1	1	0	1	0	0	0
1	1	1	0	1	1	0	0	0	0
1	1	1	1	0	0	0	1	0	0

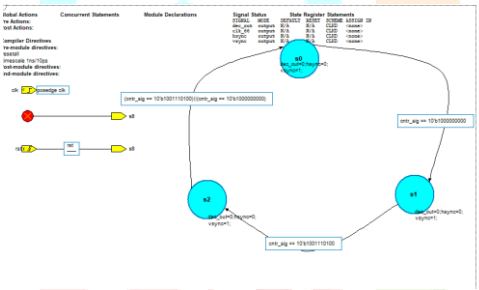
The above figure represents the protection bits that we have assigned to the decode for the detection of the active video and these bits are encoded in the encoder with the coding part using HDL encoder llc and the values indicates the starting and ending of the video and we are having 2 field bits where video starts decoding if and only if RST is 0 and clock is 1.

BT 1120 Decoder:-

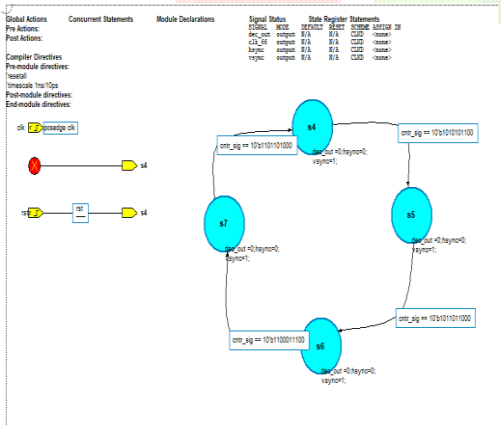


It is the main part of the whole project where the decoding of the video signal is processed we are set with the protection bits in the encoder part if the video signal is having the binary values of the protection bits then the decoder takes the video data and sets the Hsync to high with the help of the CSM and the control signals there are total 10 state machines in our decoder with each having its own configuration as shown in the below figures the configuration and the working of each CSMs and with respective state machines as shown in the figures below.

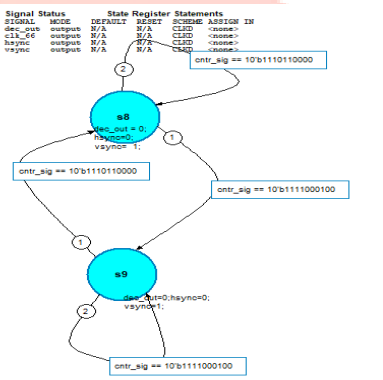
CSM1



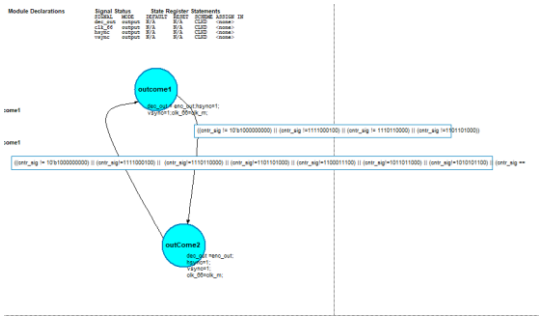
CSM2



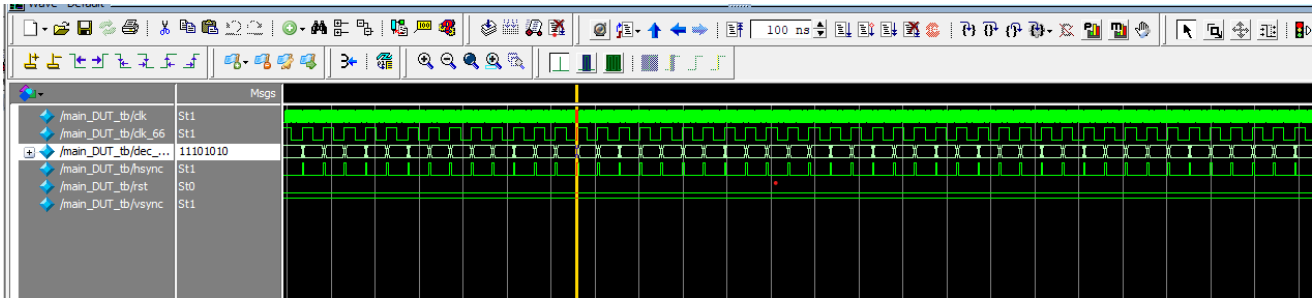
CSM3



CSM output



OUTPUT WAVE:-



In the output part we have to detect and extract the Hsync and Vsync and clock but where as per our design of BT1120 we have kept the Vsync high till the all the Hcount and Vcount values are done so we will be getting our Hysnc values at the active video and the 8 bit data values are out and we can fix the pixel clock to any values here we fixed it 66MhZ

III. CONCLUSION

The design of a BT.1120 – 8 chip, which gives HD output by implementing decoding using Verilog HDL has been described. TheBT.1120 decoding technique gives Hsync and Vsync time scaling, and with the use of Hsync and Vsync we ensure that the HD video has been decoded from the 8-bit input data The decoder has been designed as a general purpose one, and is capable of implementing HD video signals with the help of CSM. By using Hcount and Vcount each and every counter receives video signals and transmits the data to the decoder and it will be able to give output. Even though for testing the design, the methodology used is different, the overall design is not restricted to any particular software but logic remains same for any software tool.. It is provided with a standard interface so that it can be used along with any of the commercial decoders available. The behavioural description of the decoder was carried out using Verilog HDL, and a behavioural simulation of the muter was described. The structural description of decoder was carried out using the HDL designer, and compiled using the Modelsim Simulator. A test-flit is sent through all inputs of decoder to ensure that values change from time to time to give multiple inputs to the decoder we used a test bench code . If no acknowledgements are received for the test-flit, then the decoder concludes that the corresponding video data did not have any active video signals.

We implemented BT.1120 decoder as an improvement to the BT.656 decoder which only decode SD tv signals whereas BT.1120 decode HD tv signals also.

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