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Design of QCA based RS flip-flop

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Abstract: Quantum dot cellular automata (QCA) are the most upcoming technology which replaces CMOS technology. The limitations of CMOS can be overcome by using QCA technology that has many special features.

QCA provides high speed and small size, resulting in low power consumption which meets all the features of nanotechnology and is more efficient than CMOS.

In this paper, a general over view of QCA technology is presented. This paper also presents the design of RS flip-flop.

Index Terms : QCA cell, QCA technology, CMOS and Flip-flops.

I. INTRODUCTION

According to the Moore's Law , the size of transistors grows exponentially with respect to time. Somehow, the basic limitations of CMOS technology which are given by law of physics are satisfied, but better results will yield if this technology is replaced by some other new technology.

The number of IC is increasing successfully with CMOS devices for the last few decades. To fabricate CMOS transistors into smaller and smaller size, resulting in reaching to its limitations. Hence many new approaches have been proposed. QCA is suitable for computing with new technology ,that can replaces the conventional CMOS technology.[1]

QCA technology , depends on electron configurations whereas in CMOS it depends on voltage levels . The main feature of QCA is, it reduces the complexity .

The main advantages of QCA technology are:

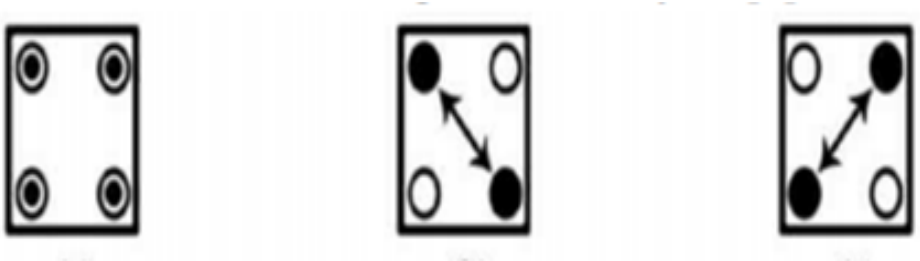
- high thickness
- very high operational recurrence
- low power utilization

II. II. QCA FUNDAMENTALS

Here the fundamental of QCA is presented which are QCA cells, QCA wires, QCA gates and QCA clocking zones. These are the basic building blocks of QCA technology.

a) QCA CELL

By using QCA cell ,circuits are designed .Each QCA cell is considered as a square and four "dots", placed at the corners .Two electrons are there in each QCA cell.[2] .These electrons are placed diagonally in quantum dots of the cell as to maintain maximum distance because of columbic repulsion of each other. The polarization of the QCA depends on electrons positions. The positions of the electrons define the polarization (p) state of the cell. A binary '0'and binary '1' is represented by p= -1 and p=+1.If electrons are present as shown in figure 1(b) polarization-1 which represent binary '0'and if electron are shown in figure 1 (c) polarization is +1 which represent binary '1'[3].



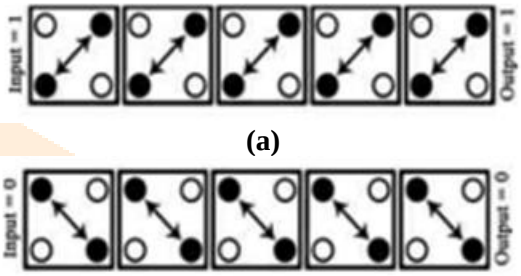
a) Empty cell **b) Polarization -1** **c)Polarization+1**

Fig.1: QCA cell

b) QCA WIRES

Wires in QCA is constructed by arranging cells in a line. The binary information (1 or 0) is transmitted from one end to another end .The binary information which enters at first cell ,reaches the last cell .QCA wires are two types a)binary wire b)inverter chain

Transmission of '1' is shown in figure 2(a) and transmission of '0' is shown in figure 2(b).



(a)

(b)

Fig.2: (a) Transmitting binary 1 (b) Transmitting binary 0

In binary wire, all the QCA cell have the same polarization .The cells polarization in an inverter chain is changed alternatively.

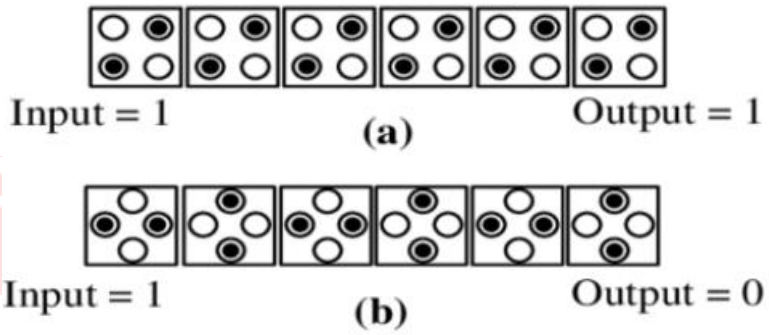


Fig.3 (a) Binary wire (b) inverter Chain

c) QCA GATES

The basic logical gates in QCA technology is majority gate and NOT gates just like in conventional logic circuits AND, OR, NOT gates are the basics gates.

i) QCA MAJORITY GATE

Majority gate is an basic element in the QCA circuits .MG is 3 input majority gate which is having five cells in which 3 are inputs ,one is output and another one is centre cell which is evaluating cell. Centre cell find the majority of binary information from 3 inputs and transmit to the output cell. A,B,C are input variables, Majority gate expression is given by

$$Y = M(A, B, C) = AB + BC + CA \quad (1)$$

If any one of the inputs of Majority gate is assigned to '0', it will be equivalent to an AND gate. A OR gate can be achieved when one of the MG inputs is set to '1'.MG shown in the figure 4(a) and 4(b)

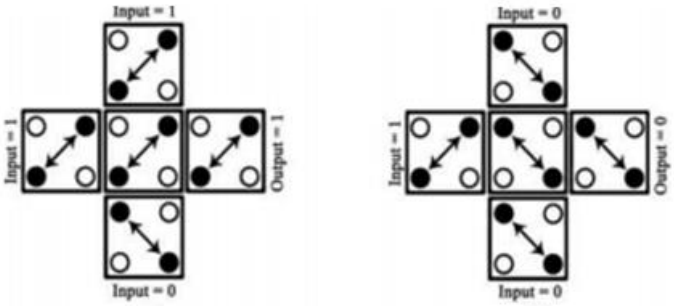


Fig.4 (a) Majority '1' **(b) Majority '0'**

iii) QCA CLOCKING

There are four clock phases to QCA cells: Switch phase, Hold phase, Release phase and Relax phase as depicted in figure5.[4]

Switch phase: The tunneling barriers between dots of QCA cell are raised. So the QCA cell becomes in polarized state. Hold phase: barrier of the cell stays high and electron can't burrow among specks and the cell keeps up its present states (settled polarization).

Release phase: barrier between dots of QCA cell are decreased and electron can tunnel through dots. So QCA cell become in un-polarized state.

Relax phase: barrier stay at lowered and cell remains in un-polarized state. Different colours mean different clock zones, beginning with green, cyan, light blue and white.

Initially in switch phase ,QCA cells are unpolarized and the potential barriers are low after that QCA cells are polarize, in switch phase and barriers become high and computation occurs in this phase .In hold phase of the clock barriers remain at high. During the clock release phase, barriers go low and QCA cells remain at unpolarized [5].When clock is on the ground state, it interacts with excited states.

Clock zone based wire crossover : There are four clock zones in QCA cells and they are clock 0 (green), clock 1 (pink), clock 2 (cyan) and clock 3 (white) is depicted in figure 5.

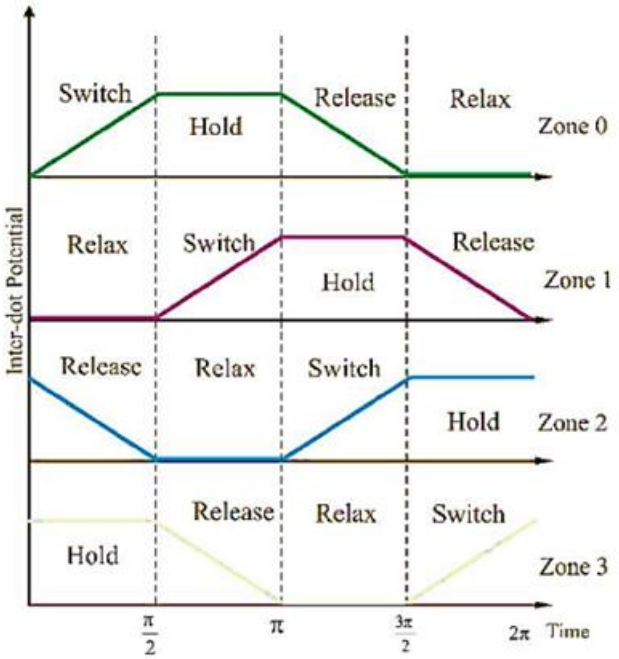


Fig.5.QCA cell four clock zones

Each clock zone defers by 90° degrees, with its adjacent or next clock zone and clock 0, clock 3 are adjacent to each other the inter section of two QCA wires can be implemented using 180° out of phase .

III. METHODOLOGY

Here flip-flops are designed using QCA technique .
Flip flops :To design sequential circuits, the conventional CMOS circuits are not suitable to direct translated into QCA architecture due to timing constraint of the sequential logic circuits. Therefore, the truth tables of each sequential circuit have been observed and the Boolean equations have been derived for each circuit. From the relationship of each variable can be clearly observed and number of required logic gates can be determined.
R-S FLIP FLOP DESIGN

The Boolean expression for an RS flip flop is given by:

$$Q_{n+1} = S + R\,\bar{Q}_n \qquad (1)$$

The block diagram of the QCA RS flip flop is shown in Fig. 3a .This block diagram is equivalent to the following equation [2]:

$$Q_{n+1} = M(S, \bar{R}, Q_n) \qquad (2)$$

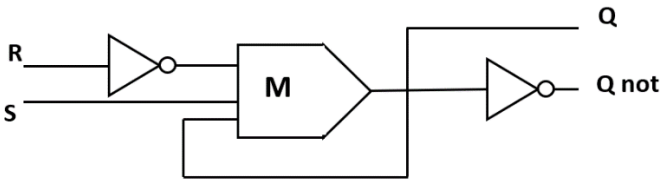


Fig.6 QCA Block diagram of RS Flip-flop

Figure 6 shows the proposed QCA RS flip flop. The inner loop of the flip flop has a delay of one clock cycle; therefore at the output, Q is available 5 clocking zones after R and S have been applied.

IV. Simulation Results:

The layout of RS flip-flop is shown in the figure7 and the simulation result is shown in figure 8.

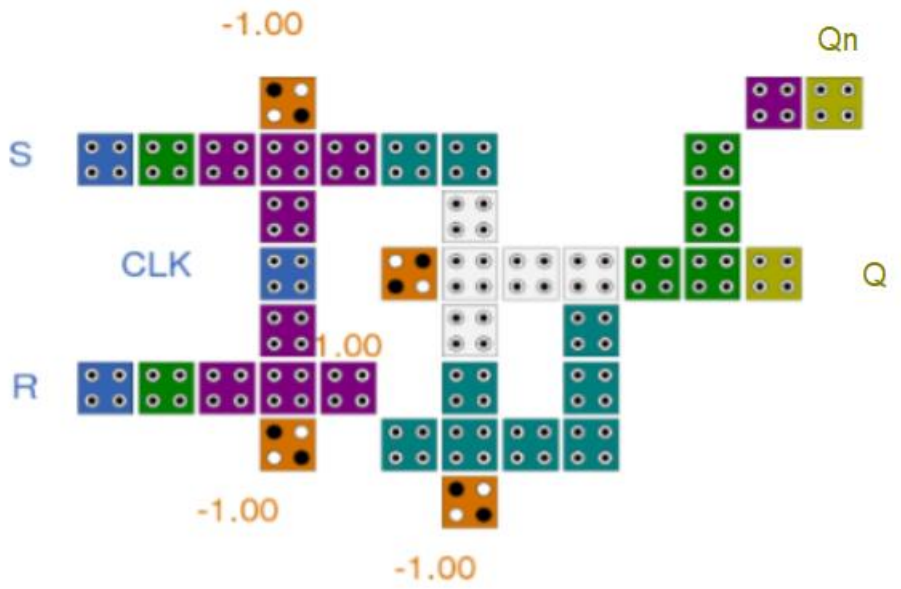


Fig.7 Layout of RS Flip-flop

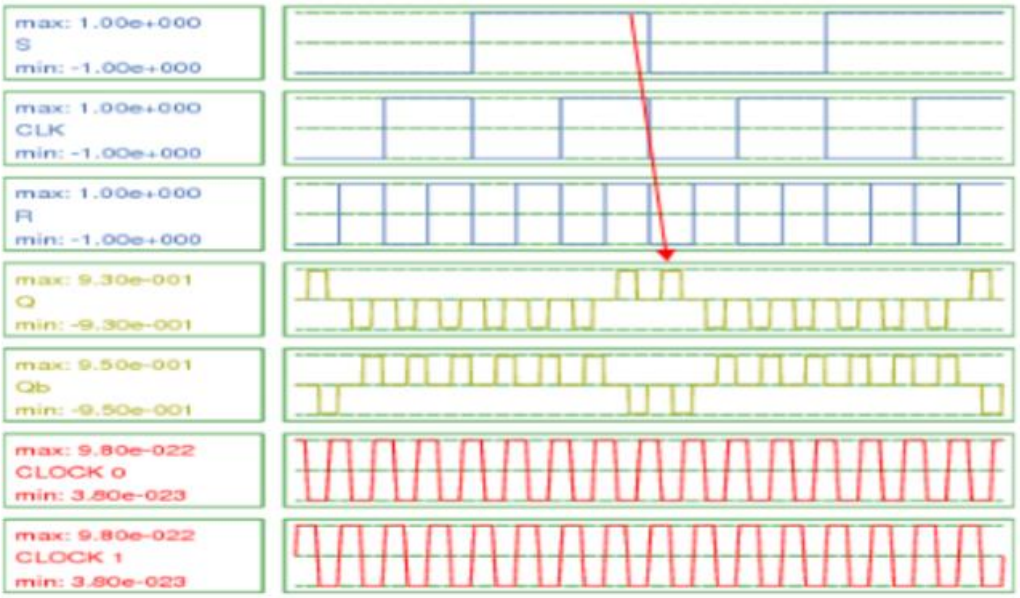


Fig.8 Simulation result of RS flip-flop

TABLE 1: CALCULATIONS OF CELL COUNT, AUF, O-COST & LATENCY OF THE DESIGNED FLIP-FLOP

QCA Structure	Length Covered (nm)	Width Covered(nm)	Cell Count (cells)
SR flip-flop	258	158	38

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