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DEVELOPMENT OF A SIMPLE SOURCE – REFERENCED CURRENT VOLTAGE MODEL

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Abstract: for Low Power CMOS Analog Design the requirements of modeling MOS Devices are both very demanding and stringent. For low power the devices operate at low voltage and low current. The operating regions of the devices pertain to strong, moderate and weak inversion modes with its characteristics device physics and model parameters. From simulation viewpoint the major concern of model development has been the continuity of current and model parameters in the transition region of these modes of operation. For a compact model for analog design these issues have to be addressed along with the effects of scaling down to submicron level. The paper discuss briefly the study of development of a simple source –referenced current voltage model, Review of two and three terminal MOS capacitor (Definition of Strong, Moderate and Weak Inversion, Threshold Voltage, Capacitance-Voltage Characteristics), and Criteria for compact MOSFET model with reference to Low Power Analog Design.

Index Terms - MOS, Sio2, CMOS, SOI, CSA, GCA, FET.

I. INTRODUCTION

Computer-aided design tools have become indispensable in integrated-circuit design. The Simulation Program with Integrated Circuit Emphasis (SPICE) program [1] has been widely accepted for circuit analysis since its introduction a decade ago. Circuit-simulation execution time has been substantially reduced through algorithm improvement and hardware enhancements in the past few years. Novel circuit-simulation algorithms, such as the iterated-timing-analysis method [2] and the waveform relaxation method [3], promise to offer more than an order of magnitude speed-up as compared with the conventional circuit simulator SPICE2. The dedicated-hardware approach, such as multiprocessor-based simulation schemes [4], [5], also drastically reduces the circuit-simulation time. Device modeling plays an important role in VLSI circuit design because computer-aided circuit analysis results are only as accurate as the models used. In the past, the SPICE2 program has provided three built-in MOS transistor models [6]. The Level-1 model, which contains fairly simple expressions, is most suitable for preliminary analysis. The Level-2 model, which contains expressions from detailed device physics, does not work well for small geometry transistors. The Level-3 model represents an attempt to pursue the semi-empirical modeling approach, which only approximates device physics and relies on the proper choice of the empirical parameters to accurately reproduce device characteristics.

Many articles on MOS transistor Many articles on MOS transistor modeling have appeared in the literature [7]–[16] and efforts to model ever smaller and more complex MOS transistors continue at a rapid pace. MOS transistor models widely used in circuit analysis are essentially semi-empirical in nature. Terms with strong physical meaning are employed to model the fundamental physical effects while parameters are judiciously introduced to embrace subtle device characteristics. This approach serves best for circuit-analysis purposes especially as two- and three-dimensional small-geometry effects become more important. In this paper, the development of a simple source –referenced current voltage model is described.

II. MOSFET DEVICE PHYSICS AND OPERATION

The most important FET is the MOSFET. In silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide (SiO2) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of a p-type substrate (n-channel device) or holes in the case of an n-type substrate (p-channel device), induced in the semiconductor at the silicon-insulator interface by the voltage applied to the gate electrode. The electrons enter and exit the channel at n+ source and drain contacts in the case of an n-channel MOSFET, and at p+ contacts in the case of a p-channel MOSFET. MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs). In recent years, the device feature size of such circuits has been scaled down into the deep sub micrometer range. Presently, the 0.13-µm technology node for complementary MOSFET (CMOS) is used for very large scale ICs (VLSIs) and, within a few years, sub-0.1-µm technology will be available, with a commensurate increase in speed and in integration scale. Hundreds of millions of transistors on a single chip are used in microprocessors and in memory ICs today. CMOS technology combines both

n-channel and p-channel MOSFETs to provide very low power consumption along with high speed. New silicon-on-insulator (SOI) technology may help achieve three-dimensional integration, that is, One of the rapidly growing areas of CMOS is in analog circuits, spanning a variety of applications from audio circuits operating at the kilohertz (kHz) range to modern wireless applications operating at gigahertz (GHz) frequencies.

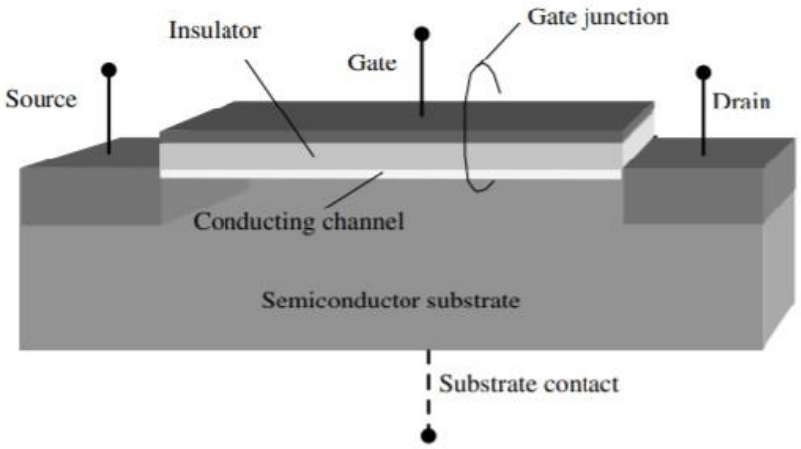


Fig.1: Generic Field Effect Transistor

III. MODELING APPROACH

For any FET, the threshold gate voltage VT is a key parameter. It separates the on- (above threshold) and the off- (subthreshold) states of operation. As indicated in Figure 1.22, the average potential energy of the channel electrons in the off-state is high relative to those of the source, creating an effective barrier against electron transport from source to drain. In the on-state, this barrier is significantly lowered, promoting a high population of free electrons in the channel region. For long-channel devices, with gate lengths of several micrometers and with high power supply voltages, the behavior in the transition region near threshold is not important in digital applications. However, for MOSFETs with deep sub micrometer feature size and reduced power supply voltages (such as in low-power operation), the transition region becomes increasingly important, and the distinction between on- and off-states becomes blurred. Accordingly, a precise modeling of all regimes of device operation, including the near-threshold regime, is needed for short-channel devices, both for digital and high-frequency analog applications.

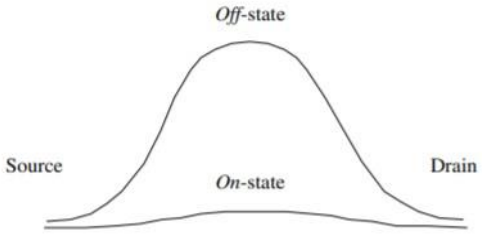


Fig 2: Schematic conduction band profile through the channel region of a short-channel MOSFET in the on-state and the off-state

In the basic MOSFET models considered in Section 1.4, the subthreshold regime is simply considered an off-state of the device, ideally blocking all drain current (although the SPICE implementations of some of these models include descriptions of this regime). In practice, however, there will always be some leakage current in the off-state owing to a finite amount of mobile charge in the channel and a finite rate of carrier injection from the source to the channel. This effect is enhanced in modern day downscaled MOSFETs owing to short-channel phenomena such as drain-induced barrier lowering. DIBL is a mechanism whereby the application of a drain-source bias causes a lowering of the source-channel junction barrier. In a long-channel device biased in the subthreshold regime, the applied drain-source voltage drop will be confined to the channel-drain depletion zone. The remaining part of the channel is essentially at a constant potential (flat energy bands), where diffusion is the primary mode of charge transport.

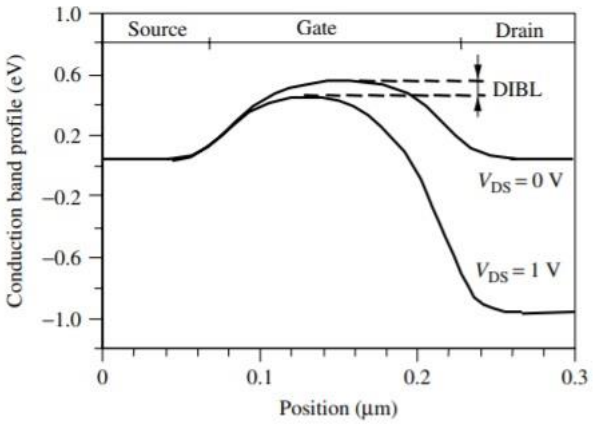


Fig 3: Conduction band profile at the semiconductor–oxide interface of a short n-channel MOSFET with and without drain bias

However, in a short-channel device the effect of the applied drain-source voltage will be distributed over the length of the channel, giving rise to a shift of the conduction band edge near the source end of the channel, as illustrated in Figure 1.23. Such a shift represents an effective lowering of the injection barrier between the source and the channel. Since the dominant injection mechanism is thermionic emission, this barrier lowering translates into a significant increase of the injected current. This phenomenon can be described in terms of a shift in the threshold voltage. Well above threshold, the injection barrier is much reduced, and the DIBL effect eventually disappears.

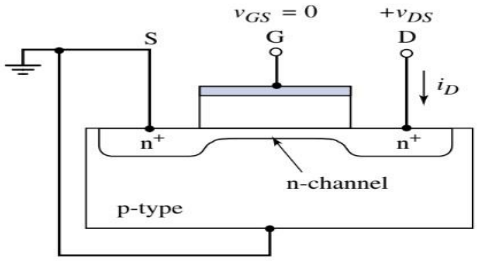
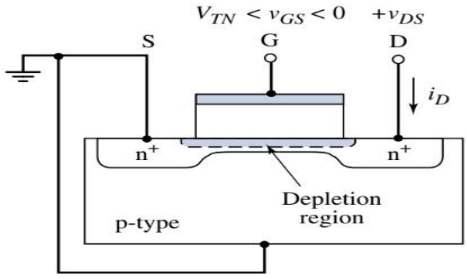


Fig 4: (a) Cross section of n-channel depletion mode MOSFET for V_{GS}= 0 Parallel plate capacitor showing electric field and conductor charges.



(b) Cross section of n-channel depletion mode MOSFET for V_{GS} < 0

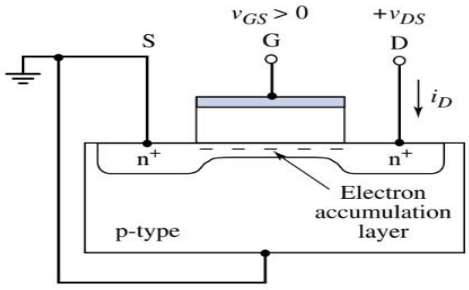


Fig6: Cross section of n-channel depletion mode MOSFET for V_{GS} > 0

The magnitude of the subthreshold current is obviously very important since it has consequences for the power supply voltages and the logic levels needed to achieve a satisfactory off-state in digital operations. Hence, it affects the power dissipation in logic circuits. Likewise, the holding time in dynamic memory circuits is affected by the level of subthreshold current.

To correctly model the subthreshold operation of MOSFETs, we need a charge control model for this regime. Also, to avoid convergence problems when using the model in circuit simulators, it is preferable to use a UCCM that covers both the above- and below threshold regimes with continuous expressions. One such model is a generalization of the UCCM that was introduced for the purpose of accurately describing the inversion charge density in MOS structures.

IV. MODEL FORMULATION

- **Incremental Charge Balanced Equation:**
  $\Delta Q'_G = -(\Delta Q'_1 + \Delta Q'_B)$
- **Gauss Law:**
  $Q'_G = C'_{ox}\Psi_{ox}$
- There are 6 variables so we have total 5 equations. from these eliminate 4 to get a relation between Ψ_S and V_{GB}
  $V_{GB} = V_{FB} + \Psi_s + \gamma\sqrt{\Psi_s + \emptyset_t \exp[\Psi_s - 2\emptyset_F/\emptyset_t]}$
- Transcendental equation cannot be solved analytically, has to be evaluated numerically
- One of the biggest bottlenecks of analytical modelling of MOSFETs
- Five basic fundamental equations :

Potential Balanced equation:

$$V_{GB} = \Psi_{ox} + \Psi_s + \emptyset_{ms}$$

Incremental Potential Balanced equation:

$$V_{GB} = \Psi_{ox} + \Psi_s$$

Charge Balance equation:

$$Q'_G + Q'_{ox} + Q'_1 + Q'_B = 0$$

Where

$Q'_G -$ gate charge, $Q'_{ox} -$ oxide charge, Q'_1 inversion charge, and $Q'_B -$ depletion charge , all per unit area

V. STRONG INVERSION MODEL

In **strong inversion**, a change in the applied voltage will primarily affect the minority carrier charge at the interface, owing to the **strong** dependence of this charge on the surface potential. This means that the depletion width reaches a maximum value with no significant further increase in the depletion charge.

- Assume that $V_{GS} > V_T$ and V_{DS}.
- Tow-dimensional field exists-one directed from source to body (along y, E_y, due to gate voltage) and the other directed from rain to source (along x, E_X due to drain voltage).
- Now consider two important assumptions:
  -Channel Sheet Assumptions (CSA): inversion layer a thin sheet of charge with negligible potential dropped across it
  -Entire surface potential Ψ_S drops across depletion layer.
  -Gradual channel approximation (GCA): Now, an important assumption is made, known as the Gradual channel approximation (GCA) which states that rate of change of lateral field (E_X) is much smaller than that of the vertical field (E_y).
  i.e. $\frac{\partial E_X}{\partial x} \ll \frac{\partial E_y}{\partial y}$.

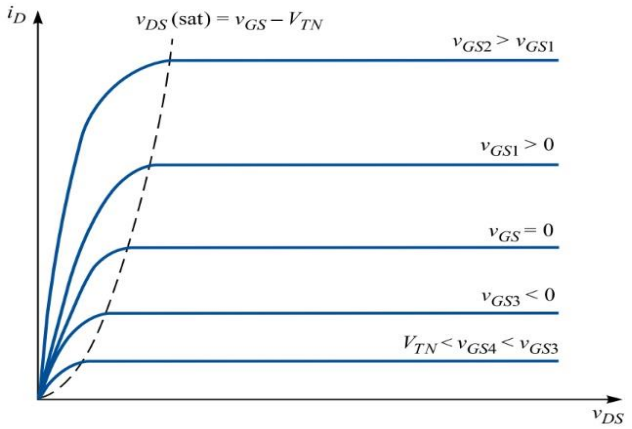


Fig 5: Current – voltage characteristics of MOSFET

Based on this assumption, the channel potential V(x) can be assumed to change linearly from 0 at the source end to V_{DS} at the drain end (this significantly simplifies mathematics)- note that this potential is measured with respect to source.

The inversion charge per unit area Q'_1 can be expressed by assuming that gate and the inversion channel behaves like a parallel plate capacitor with the potential dropped across it changing with position, i.e.

$$Q'_1(x) = -C'_{ox}[V_{GS} - V_T - V(x)]$$

Now the entire current is consider to be due to drift alone (another important assumption)

Thus, we start with the point from the ohm's law

$$|J_X| = \sigma_n |E_X|$$

Where

$|J_X|$ is the current density, $|E_X|$ is the electric field, and σ_n is the conductivity due to electrons present in the channel, with μ_n being the electron mobility and n being the concentration of the electrons in the channel per unit volume.

The electric field E_X can also be written as:

$$|E_X| = \frac{dV(X)}{dX}$$

Now the entire current is consider to be due to drift alone (another important assumption)

Thus, we start with the point from the ohm's law

$$|J_X| = \sigma_n |E_X|$$

(a) (b)

Fig 6: the n channel depletion mode MOSFET
(a) Conventional circuit symbol (b) Simplified circuit symbol

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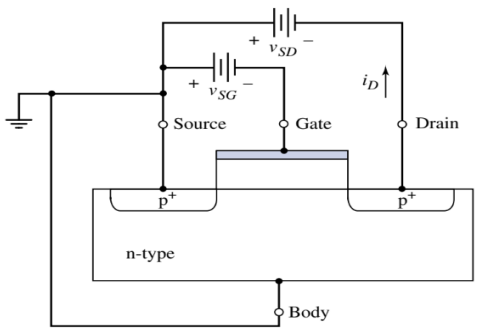

Fig 7: Cross section of p-channel enhancement mode MOSFET

The drain current I_D is given by current $I_D = |J_X| \times A$,

Where A $(= W \times \delta d)$ is the cross sectional area that the carrier face, where W is the channel width and δd is an average thickness of the inversion layer along the channel.

Also the inversion charge per unit area Q_1' can be given by

$$Q_1' = q \times n \times \delta d$$

Thus $I_D = |J_X| \times A$

$$= q\, \mu_n\, n\, W\, \delta d \left[{}^{dV(x)}/_{dx} \right]$$

$$= \mu_n\, W\, |Q_1'| \left[{}^{dV(x)}/_{dx} \right]$$

This expression has to be integrated from x = 0 (corresponding to V (0) = 0) to x = L (corresponding to V (L) =V_{DS}), i.e.

$$\int_0^L I_D\, dx = W \int_0^{V_{DS}} \mu_n\, |Q_1'|\, dV(x)$$

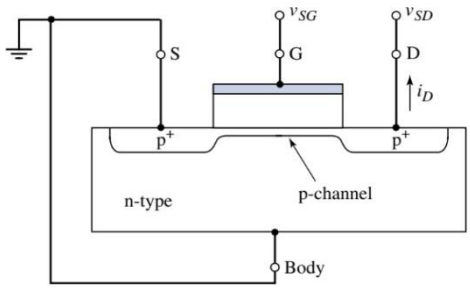

Fig 8: Cross section of n-channel depletion mode MOSFET

Now, assuming that the electron mobility μ_n is constant, we can take it out of the integral Also the inversion charge per unit area Q_1' is given by

$$|Q_1'| = -C_{ox}'[V_{GS} - V_T - V(x)]$$

Thus the drain current:

$$I_D = \frac{W}{L}\mu_n C_{ox}' \int_0^{V_{DS}} [V_{GS} - V_T - V(x)]\, dV(x)$$
$$= k_N \left[(V_{GS} - V_T)V_{DS} \frac{V_{DS}^2}{2}\right]$$

Where $k_N = (\frac{W}{L})k_N'$ is known as the device **transconductance parameter**,

With $k_N' = \mu_n C_{ox}'$ known as the **process transconductance parameter**.

Note that for small V_{DS} the quadratic term in V_{DS} can be neglected, and I_D is seen to change linearly with respect to V_{DS} − thus, this region of operation is known as the linear region.

As V_{DS} increases, the rate of increase of I_D with respect to V_{DS} slows down, since now the quadratic term has a restraining effect.

Another interesting observation can be made from the expression of $|Q_1'|$: it is seen that $|Q_1'|$ goes to zero if V(x) equals $(V_{GS} - V_T)$

Putting x = L, i.e., the drain end, corresponding value of V_{DS} is known as $V_{DS,sat}$ and is given by

$$V_{DS,sat} = V_{GS} - V_T$$

This phenomenon is known as the pinching-off of the channel at the drain end, which is also termed as **saturation**.

Based on this simple theory, for $V_{DS} > V_{DS,sat}$, the drain current does not increase anymore and is given by substituting $V_{DS,sat} = V_{GS} - V_T$ in the linear region current equation

Thus the saturated drain current:

$$I_{D,sat} = \frac{k_N}{2}[(V_{GS} - V_T)^2]$$

From these two current equations, the dependence of I_D on V_{GS} and V_{DS} is explicit, however the dependence on V_{BS} is implicit through the expression for V_T , is given by

$$V_T = V_{T0} + \gamma\left(\sqrt{2\emptyset_F + V_{SB}} - \sqrt{2\emptyset_F}\right)$$

Where V_{SB} is known as the back bias (generally positive or small negative) and $V_{T0} = V_T\,|_{V_{SB}=0}$

$$V_{T0} = V_{SB} + 2\emptyset_F + \gamma\sqrt{2\emptyset_F}$$

This increase in the threshold voltage V_T with respect to the back bias voltage V_{SB} (or, alternately V_{SB}) is known as the **body effect**, and the coefficient γ is termed as the **body effect coefficient**, and is proportional to t_{ox} and $\sqrt{N_A}$

Combining of all these equations, we get the **Level 0** model of MOSFET.

$$I_D = k_N \left[(V_{GS} - V_T)V_{DS} \frac{V_{DS}^2}{2}\right] \quad \text{(Linear region - } V_{GS} > V_T, V_{DS} < V_{GS} - V_T)$$

$$I_D = \frac{k_N}{2}(V_{GS} - V_T)^2 \quad \text{(Saturation region- } V_{GS} > V_T, V_{DS} \geq V_{GS} - V_T))$$

$$I_D = 0 \quad \text{(Cut-off region- } V_{GS} < any\ V_{DS})$$

For PMOSFETs, all voltages are negative and k_N is replaced by

$k_P = (\frac{W}{L})k_P'$,

Where

$k_P' = \mu_p C_{ox}'$ with μ_p being the hole mobility, $(\frac{W}{L})$ is known as the aspect ratio of the device

Typically, for Si, $\mu_n \cong 2.5\mu_p$, thus for the same aspect ratio, NMOSFETs can carry more current than PMOSFETs, and are inherently faster. Generally for a given fabrication process, k_N' and k_P' are somewhat constants, however the aspect ratios can be changed to obtain the desired performance.

VI. SUMMARY

The static characteristics of n-channel and p-channel MOS devices are shown, with details on the maximum current and its relationship with the sizing, the threshold voltage and various 2nd order effects. Three generations of MOS device models are introduced. Firstly, the original MOS model 1 is presented, as it was proposed in the early versions of SPICE simulator developed by the University of Berkeley, California. This model only applies for long channel devices. Secondly, we introduce the semi-empirical model 3, which is still in use for MOS device simulation with a channel length greater than 1µm. thirdly, we present a simplified version of the BSMI4 models, developed by the University of Berkeley for MOS devices with channel length down to 100nm.This paper describes a complete modeling approach for MOS VLSI circuit design especially Level 0 model which is highly automated and provides statistically relevant parameter files. A description of key model equations, which include the effects of non - uniformly doped channels, charge sharing bulk - charge terms, and lateral and vertical field mobility reduction terms, will be given.

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