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REVERSIBLE LOGIC DESIGN FOR ADDER IN CMOS VLSI DESIGN

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ABSTRACT

Reversible logic has attracted significant attention in recent years. It has applications in quantum computing, nanotechnology, low power CMOS, and optical computing. In reversible logic bit loss is recovered by unique input-output mapping where in conventional logic it is not possible. It is one of distinct feature of reversible logic. Reversible logic the input pattern is recovered from its output pattern but it fails conventional logic.It is one of distinct feature of reversible logic.The technological costs of Toffoli and Fredkin gates are comparable, it has been shown that using both types of gates results in network specifications with fewer gates. Therefore, a synthesis procedure exploiting both types of gates is of interest. In this paper, we concentrate on the synthesis of networks with these well-known gates and their straightforward generalizations.

INTRODUCTION

The overall goal of our project is to minimum number of gate, minimum quantum cost, minimum number of constant inputs, minimum number of garbage outputs, minimum delay by using a reversible logic. The following chapter consists of adders designed using reversible gates

1.1 REVERSIBLE LOGIC

In reversible logic the input pattern is recovered from its output pattern but it fails conventional logic it is not possible. It is one of distinct feature of reversible logic. In 1961, the research of R. Landauer illustrated that the amount of energy dissipated for every information bit loss is at least kTln2 joules, where k is Boltzmann constant and T is temperature at which system operation is performed. The amount of energy which is dissipated due to one-bit information loss is very small. But in high speed computational works the number of information bits is more. Then the heat dissipation is also more. This dissipation affects the performance and reduces the lifetime of system. In 1973, Bennet demonstrated that kTln2 energy will not be dissipated if the inputs are able to recover from its output. Hence the power dissipation will be zero if a network contains only reversible logic gates. Also direct fan-out is not allowed in the synthesis of reversible logic gates because oneto-many concept is not reversible. By using additional reversible logic gates the fan-out can be achieved. The synthesis of reversible logic is different from the conventional logic. First, the reversible circuit should not have fan-out i.e., the output of any gate is connected as input to any gate once only. Secondly, the input output patterns have one to one correspondence. Lastly, the circuit must be acyclic. In addition to these a circuit is called reversible if the outputs are applied at the output then inputs are reproduced at the input i.e., we are reproducing the inputs from outputs. The fault tolerant reversible gates are special gates in reversible gates. The fault tolerant gates satisfy the property of parity preserving i.e., the parity of input and output is same. A logic block is called parity preserving if every gate in that is parity preserving. If a logic block is implemented with fault tolerant gates, then those gates will not require extra circuitry to check errors which occur in computation or communication. Addition is one of the essential

operations in multiplication and division algorithms. It plays a vital role in many applications like DSP processors, Microprocessors and in computing devices. Hence, it is required to design fast adder. This paper presents a novel design of reversible optimized fault tolerant Full adder/ Full subtractor. This paper proposes an efficient approach to implement 1-bit adder which will play a vital role in future quantum computers.

1.2 REVERSIBLE LOGIC FOR GATES

The fault tolerant gates satisfies the property of parity preserving i.e., the parity of input and output is same. A logic block is called parity preserving if every gate in that is parity preserving. If a logic block is implemented with fault tolerant gates then those gates will not require extra circuitry to check errors which occur in computation or communication. Addition is one of the essential operations in multiplication and division algorithms. It plays a vital role in many applications. A reversible function (gate) is a bijection. Traditional gates such as AND, OR, and EXOR are not reversible. In fact, NOT is the only reversible gate from the traditional set of gates.

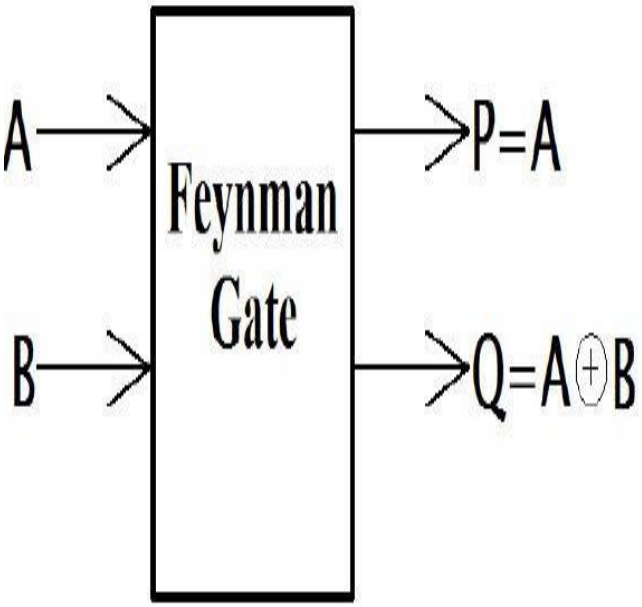
1.3 REVERSIBLE GATE

Reversible gate is a digital circuit whose number of inputs and number of outputs are equal. If there are k inputs, there will be k outputs. Each input pattern has unique output pattern. This is called as one-one correspondence. It is denoted by k*k.

There are many reversible gates available in literature. Among them few important gates are Feynman Gate (FG), Feynman Double Gate (F2G), Fred kin Gate (FRG), Toffoli Gate (TG), and Peres Gate (PG).

1.3.1 FEYNMAN GATE

Feynman gate is one of the basic reversible logic gates with 2 inputs and 2 outputs, also called as 2*2 gates, depicted. The inputs are denoted by I (A, B) and the outputs are denoted by O (P, Q). quantum cost is 1. The outputs are given by P = A ; Q = A ⊕ B ;



Inputs		Outputs	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 1.3.1 Feyman Gate

1.3.2 FEYNMAN DOUBLE GATE

Feynman Double gate is also one of the basic reversible logic gate with 3 inputs and 3 outputs also represented as 3*3 gate. The inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, R). The relation between inputs and outputs are given by

P = A; Q = A ⊕ B; R = A ⊕ C;

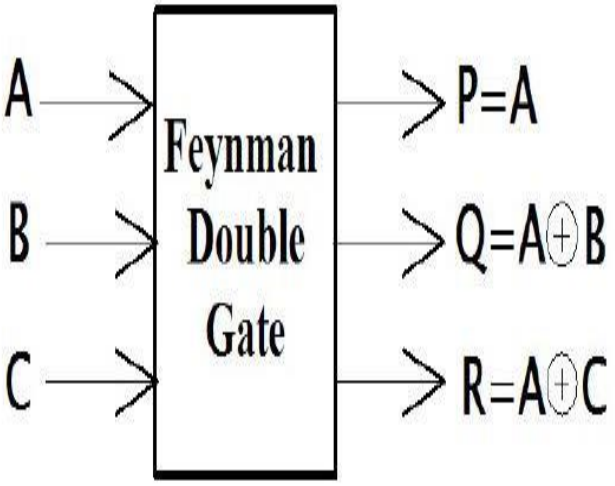


Figure 1.3.2 Feynman Double Gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

*

Quantum cost of a Feynman double gate is 2

1.3.3 TOFFOLI GATE

Toffoli gate is also one of the basic reversible logic gates with 3 inputs and 3 outputs. It also called as 3*3 gate. For a toffoli gate, the inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, R). The relationship between inputs and outputs is P = A; Q = B; R = AB $\oplus$ C;

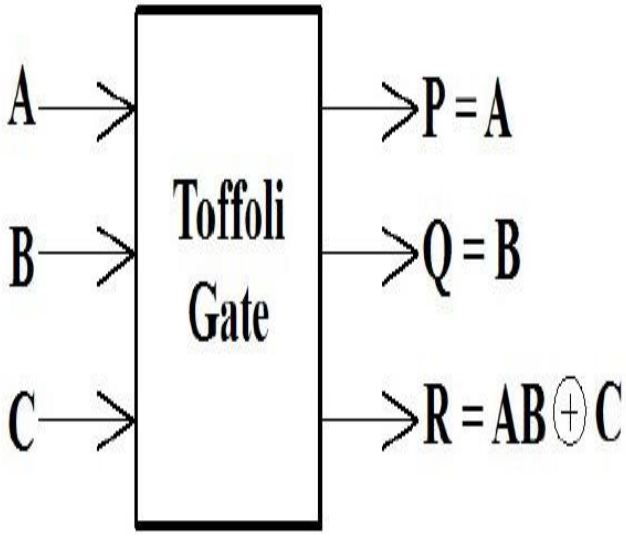


Figure 1.3.3 Toffoli Gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

The quantum cost of a Toffoli gate is 5

1.34 SCOPEOF THE PROJECT

This method focus mainly on implementation of a model which can be operated as ripple carry, mux with better performance. Here a structure is proposed with parity preserving gates which reduce testing hardware. The reversible logic concept work efficiently if number of garbage outputs, constant inputs and quantum cost is low. The power dissipation is zero if the reversible logic circuits are implemented with quantum gates. If we do that then we can save power, money as well as nature.

LITERATURE SURVEY

2.1 Minimization of reversible adder circuits

Saiful Islam and Rafiqul Islam(2005) presented losing information causes losing power. Information is lost when the input vector cannot be uniquely recovered from the output vector of a combinational circuit. The input vector of reversible circuit can be uniquely recovered from the output vector. In this study we have emphasized on the design of reversible adder circuits that is efficient in terms of gate count, garbage outputs and quantum cost and that can be technologically mapped. It has been analyzed and demonstrated that the results of our proposed adder circuits show better performance compared to similar type of existing designs. Technology independent equations required to evaluate these circuits have also been given

The reversible computing also offers fault diagnostic features. Quantum-dot cellular automata (QCA) nanotechnology owing to its unique features like very high operating frequency, extremely low power dissipation, and nanoscale feature size is emerging as a promising candidate to replace CMOS technology. This paper presents design and performance analysis of area efficient QCA based Feynman, Toffoli, and Fredkin universal reversible logic gates. The proposed designs of QCA reversible Feynman, Toffoli, and Fredkin reversible gates utilize 39.62, 21.05, and 24.74% less number of QCA cells as compared to previous best designs. The rectangular layout area of proposed QCA based Feynman, Toffoli, and Fredkin gates are 52, 28.10, and 40.23%, respectively less than previous best designs. The optimized designs are realized employing 5-input majority gates to make proposed designs more compact and area efficient. The major advantage is that the optimized layouts of reversible gates did not utilize any rotated, translated QCA cells, and offer single layer accessibility to their inputs and outputs. The proposed efficient layouts did not employ any coplanar or multilayer wire crossovers. The energy dissipation results have been computed for proposed area efficient reversible gates and thermal layouts are generated using accurate QCAPro power estimator tool. The functionality of presented designs has been performed

2.2 Fault-Tolerant Reversible Circuits

Behrooz Parhami (2006) published in ACSSC'06,Fortieth asilomar conference

Reversible hardware computation, that is, performing logic signal transformations in a way that allows the original input signals to be recovered from the produced outputs, is helpful in diverse areas such as quantum computing, low-power design, nanotechnology, optical information processing, and bioinformatics. We propose a paradigm for performing such reversible computations in a manner that renders a wide class of circuit faults readily detectable at the circuit's outputs. More specifically, we introduce a class of reversible logic gates (consisting of the well-known Fredkin gate and a newly defined Feynman double-gate) for which the parity of the outputs matches that of the inputs. Such parity-preserving reversible gates, when used with an arbitrary synthesis strategy for reversible logic circuits, allow any fault that affects no more than a single logic signal to be detectable at the circuit's primary outputs. We show the applicability of our design strategy by demonstrating how the well-known, and very useful, Toffoli gate can be synthesized from parity preserving gates and apply the results to the design of a binary full-adder circuit, which is a versatile and widely used element in digital arithmetic processing.

2.3 Reversible logic gates on physarum polycephalum

Andrew schumann(2015) AIP conference proceedings . In this paper, we consider possibilities how to implement asynchronous sequential logic gates and quantumstyle reversible logic gates on Physarum polycephalum motions. We show that in asynchronous sequential logic gates we can erase information because of uncertainty in the direction of plasmodium propagation. Therefore, quantum-style reversible logic gates are more preferable for designing logic circuits on Physarum polycephalum

2.4 A transformation based algorithm for reversible logic synthesis Daniel miller,D Maslov (2013), Design automation conference. Digital combinational logic circuit is reversible if it maps each input pattern to a unique output pattern. Such circuits are of interest in quantum computing, optical computing, nanotechnology and low-power CMOS design. Synthesis approaches are not well developed for reversible circuits even for small numbers of inputs and outputs. In this paper, a transformation based algorithm for the synthesis of such a reversible circuit in terms of n × n Toffoli gates is presented. Initially, a circuit is constructed by a single pass through the specification with minimal look-ahead and no back-tracking. Reduction rules are then applied by simple template matching. The method produces very good results for larger problems. Information is lost when the input vector cannot be uniquely recovered from the output vector of a combinational circuit. The input vector of reversible circuit can be uniquely recovered from the

output vector. In this study we have emphasized on the design of reversible adder circuits that is efficient in terms of gate count, garbage outputs and quantum cost and that can be technologically mapped. It has been analysed and demonstrated that the results of our proposed adder circuits show better performance.

2.5 Design and verification of reversible logic gates using quantum dot celler automata Shaik shabeena an jyotirmoy pathak (2015) International journal of computer applications.This paper portrays the designing of Reversible Logic gates through the use of Quantum Dot Cellular Automata (QCA) which is a nanotechnology concept and also a striking substitute for transistor based technologies. This technology helps us to rise above the confines of CMOS technology. It also gives better results in terms of digital and analog waveform, Quantum cost, garbage output. The fundamental logic in QCA is the logic state that does not compute with voltage level; rather it measures the polarity of electrons in a quantum cell. Basically Reversible logic gates are an essential building block of various computing system. Comparing with standard gates, the reversible logic gate lower the information bits use loss by reusing the logic information bits logically and realizes the goal of lowering power consumption of logic circuits. A QCA designer tool is used for simulation of different kinds of Reversible logic gates such as Toffoli gate, Fredkin gate and some others. **2.6 Design and analysis of area efficient QCA based reversible logic gates**

Gurmohan singh (2017) presented on center for development of advanced computing (CDAC).The CMOS technology has been plagued by several problems in past one decade. The ever increasing power dissipation is the major problem in CMOS circuits and systems. The reversible computing has potential to overcome this problem and reversible logic circuits serve as the backbone in quantum computing. The reversible computing also offers fault diagnostic features. Quantum-dot cellular automata (QCA) nanotechnology owing to its unique features like very high operating frequency, extremely low power dissipation, and nanoscale feature size is emerging as a promising candidate to replace CMOS technology. This paper presents design and performance analysis of area efficient QCA based Feynman, Toffoli, and Fredkin universal reversible logic gates. The proposed designs of QCA reversible Feynman, Toffoli, and Fredkin reversible gates utilize 39.62, 21.05, and 24.74% less number of QCA cells as compared to previous best designs. The rectangular layout area of proposed QCA based Feynman, Toffoli, and Fredkin gates are 52, 28.10, and 40.23%, respectively less than previous best designs. The optimized designs are realized employing 5-input majority gates to make proposed designs more compact and area efficient. The major advantage is that the optimized layouts of reversible gates did not utilize any rotated, translated QCA cells, and offer single layer accessibility to their inputs and outputs. The proposed efficient layouts did not employ any coplanar or multi-layer wire crossovers. The energy dissipation results have been computed for proposed area efficient reversible gates and thermal layouts are generated using accurate QCAPro power estimator tool. The functionality of presented designs has been performed.

PROPOSED SYSTEM REVERSIBLE LOGIC FOR ADDER USING CMOS VLSI DESIGN

3.1 N-BIT ADDER

In every digital circuit the basic components are N-Bit Adders and N-Bit Multipliers. In the above said components the basic element is 1-Bit Adder. If we worked to implement 1- Bit Adder efficiently then it indirectly helps for the optimistic design of any Digital circuit. This paper proposes a circuit which works as a Full Adder and full Subtractor.

A full adder is a combinational circuit that adds 3 input bits and produces 2 outputs. In the 3 input bits 2 bits are data bits and other bit is previous stage carry. The 3 input variables are denoted by A, B and Cin. The outputs sum and carry are denoted by 'S' and 'Cout'. The mathematical equation representing the full adder is A+B+Cin. A full subtractor is a combinational circuit that subtracts 2 input bits from first input and produces 2 outputs. In the 3 input bits 2 bits are data bits and other bit is present stage borrow. The 3 input variables are denoted by A, B and Cin (for convenience purpose present stage borrow is denoted by Cin). The outputs Difference and Borrow are denoted by 'D' and 'Bout'. The mathematical equation represents full subtractor is A-B-Cin. The Boolean expressions of Full Adder / Full Subtractor are

Sum / Difference = A $\oplus$ B $\oplus$ Cin Carry out

(Cout) = (A $\oplus$ B)Cin + AB

Borrow out (Bout) = (A B) Cin + 'AB

The carry out and borrow out expressions can be modified and rewritten as

Carry out (Cout) = (A $\oplus$ B) Cin $\oplus$ AB

Borrow out (Bout) = (A B) Cin $\oplus$ 'AB

Reversible logic adder circuits which are implemented earlier by several authors are not fault tolerant (Peres gate) i.e., the parity of input and parity of output is not same. This paper describes the fault tolerant Full adder/ Full subtractor with minimal garbage outputs and constants inputs. To implement the full adder/subtractor we are using 3 Feynman double gates and one Fredkin gate.

3.2 Design of optimal fault tolerant Full adder / Full subtractor

The circuit diagram of optimal fault tolerant Full adder / Full subtractor is shown in Fig. 7. It contains F2G-1, F2G-2, F2G-3 and one Fredkin gate. For the first Feynman double gate (F2G-
1) the inputs are B and A and one constant input '0'. By using this first Feynman double gate we are duplicating the B' input and A⊕B is generated. One 'B' output act like garbage output (G1). For second Feynman double gate (F2G-2) the inputs are 'C' and 2 constant inputs '0'. The second Feynman double gate (F2G-2) is used to triplicate the Cin. For this purpose, Cin,'0','0' are applied as inputs to second Feynman double gate (F2G-2) and it produces all outputs as Cin. Among three outputs one of the Cin acts like garbage output (G2). For third
Feynman double gate (F2G-3), the inputs are A⊕B i.e., output of first Feynman double gate
(F2G-1), Cin i.e., output of second Feynman double gate (F2G-2) and one constant input '0' then the outputs are A⊕B (garbage output G3), A⊕B⊕Cin i.e., SUM / DIFFERENCE and A⊕B. The A⊕B (output of third Feynman double gate (F2G-3)), Cin (output of second Feynman double gate (F2G-2)), B (output of first Feynman double gate (F2G-1)) are applied as inputs to the Fredkin gate. The outputs are A⊕B (garbage output G4), BORROW out and CARRY out. The symbol of Optimized Parity Preserving Full Adder / Full Substractor is shown below. The following circuit also satisfies the reversibility principle i.e., explained in Fig. 9. In the diagram two OPPFAFS are considered. For OPPFAFS-1 inputs are applied. The outputs of OPPFAFS-1 are connected to OPPFAFS-2 across output. The OPPFAFS-2 going to reproducing inputs. Hence it satisfies reversibility principle.

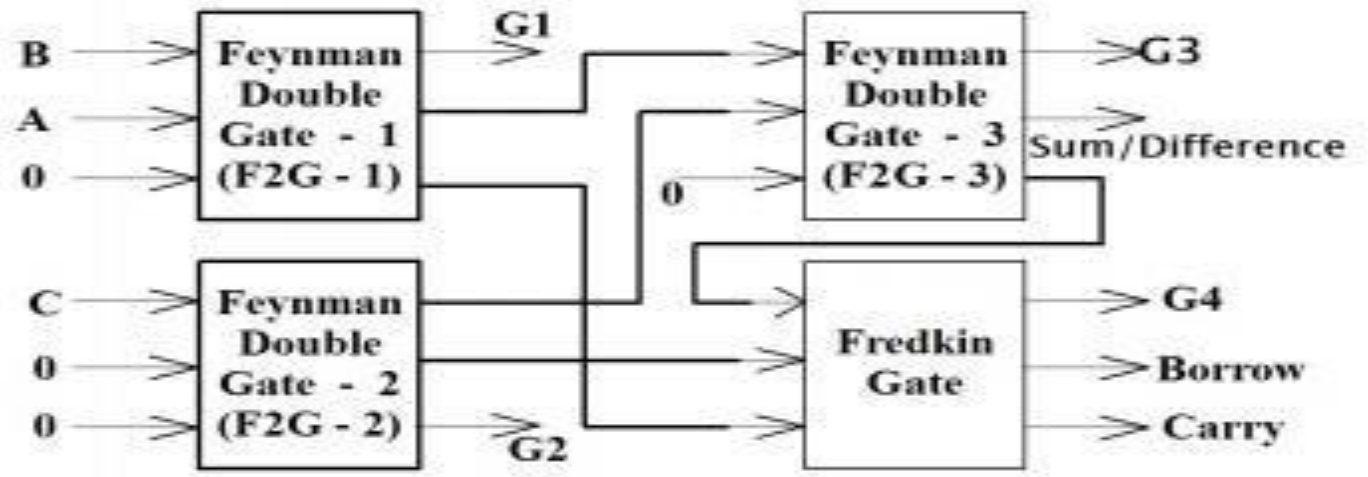


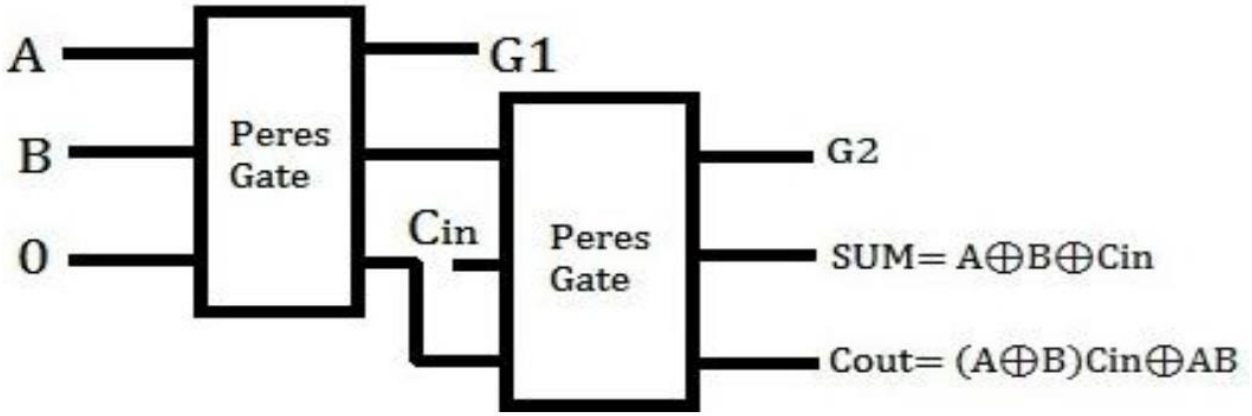
Figure 3.2 Full adder / Full Subractor 3.3 Full adder design using Peres gate

3.3.1 Ripple Carry Adder

To designing the Ripple carry adder, the basic element is full adder. So firstly we can design a modified reversible full adder for getting the optimized results by using simple 3*3 Peres gate [10] It is proved that the modified reversible full adder design can be realized with two garbage outputs and only on ancillary input. While we are designing the full adder, the 3rd input of the first Peres gate should be considered as zero. The output of the ripple carry adder is shown below.

Sum = A⊕B⊕C

Carry= (A⊕B). Cin ⊕AB



Full adder design using Peres gate

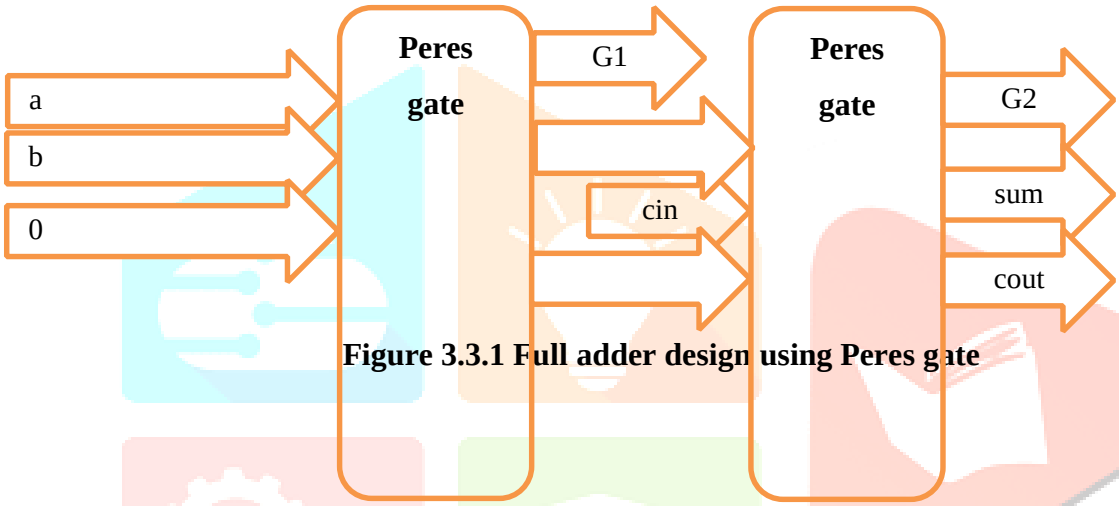


Figure 3.3.1 Full adder design using Peres gate

Truth table for full adder using peres gate

A	B	C	G1	G2	SUM	Cout
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	1	0
0	1	1	0	1	0	1
1	0	0	1	1	1	0
1	0	1	1	1	0	1
1	1	0	1	0	0	1
1	1	1	1	0	1	1

3.3.2 4 – BIT RIPPLE CARRY ADDER

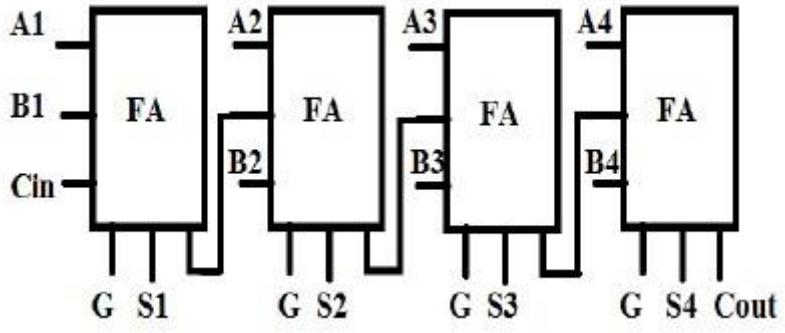


Figure 3.3.2 4-bit full adder

RCA requires n-bit full adder design circuits, ripple carry adder propagates their individual carry input through each and every full adder circuit blocks. The output carry of the ith full adder circuit is connected to (i+1) the full adder design circuit. Thus the coming next full adder circuit has to wait until the previous logic block to provide the carry for particular stage. Finally, it will provide the sum and carry afterwards the n-stages for n-bit RCA addition. The output of the first Peres gate is applied to the inputs of the second Peres gates respectively. Hence the sum and carry are generated at the final stages of the ripple carry design

3.4 CONVENTIONAL DIGITAL GATES

Implementation of the conventional digital gates can be possible by using this MUF reversible gate. The closer look at the truth table reveals that the input pattern corresponding to a specific output pattern can be uniquely determined and thereby maintaining that there is a one-to-one correspondence between the input vector and the output vector. Realization of the
AND, NOT, NAND, NOR, EXOR, EXNOR, OR are performed. Design of many combinational reversible logic circuit should include the following features. Use minimum number of reversible gates, use minimum number of garbage outputs, Use minimum constant inputs. The inputs, outputs, garbage outputs and constant inputs of a reversible gate are related as follows.
Input + constant input = output + garbage.
The total logical operation of a reversible circuit [10] is considered by together with the number of AND operations, number of EX-OR operations and number of NOT operations. If α represents the quantity of EX-OR operations, β represents the quantity of AND operations and δ represents the quantity of NOT operations then the total logical operation is expressed as the summation of EX-OR, AND and NOT operations necessary for a particular circuit and can be expressed in terms of α, ß and δ. Proposed Reversible gate and realization of its circuits can **possible by using the reversible MUF gate**.

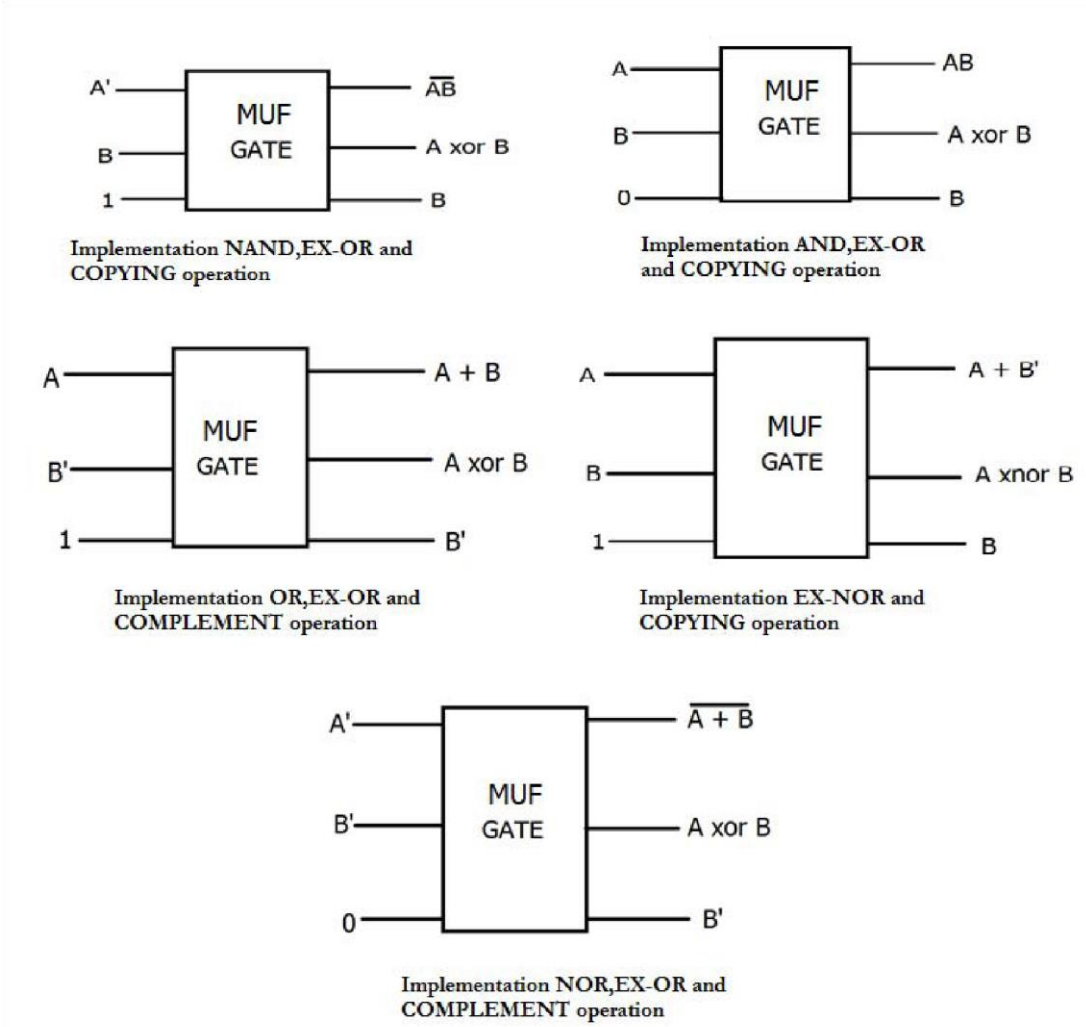
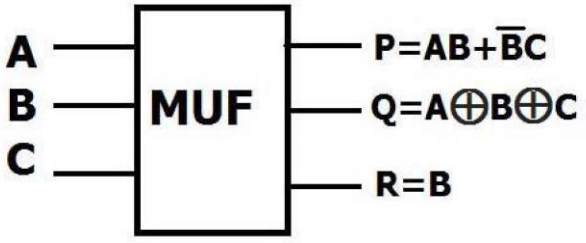


Figure 3.4 Conventional Digital Gate

3.5 DESIGN OF MUF

Reversible gate MUF has been proposed in this paper. The closer look at the truth table reveals that the input pattern corresponding to a specific output pattern can be uniquely determined and thereby maintaining that there is a one-to-one correspondence between the input vector and the output vector. In this gate the input vector is given by Iv = (A, B, C) and the corresponding output vector is Ov = (P, Q, R).



INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	1

Figure 3.5 MUF Reversible Gate

3.6 2:1 MULTIPLIXER

2:1 MUX implementation can be possible by using a single reversible MUF gate only

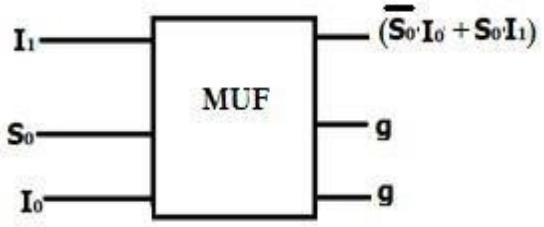


Figure 2:1 MULTIPLIXER

3.7 4:1 MULTIPLIXER

Depicts there is no change in the functionality of 4:1 reversible multiplexer with respect to the irreversible multiplexer functionality. The equation for the output Y is given as follows

Y=I0S0'S1' + I1S0S1' + I2S0'S1 + I3S0S1

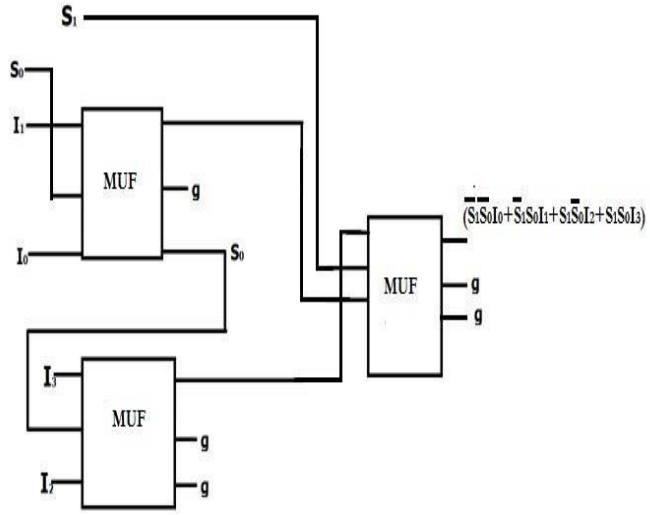


Figure 3.7 4:1 MULTIPLIXER

◦ **3.8 8:1 MULTIPLIXER**

In similar fashion 8:1 MUX has been designed

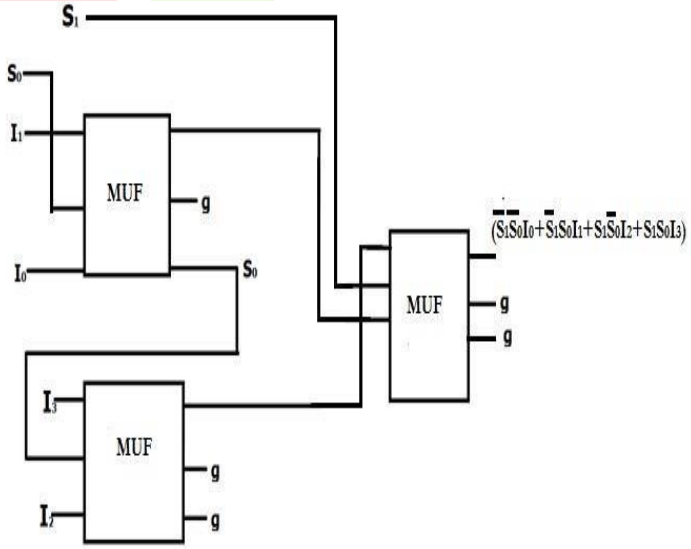


Figure 8:1 MULTIPLIXER

3.9 INTRODUCTION TO PROGRAMMABLE LOGIC:

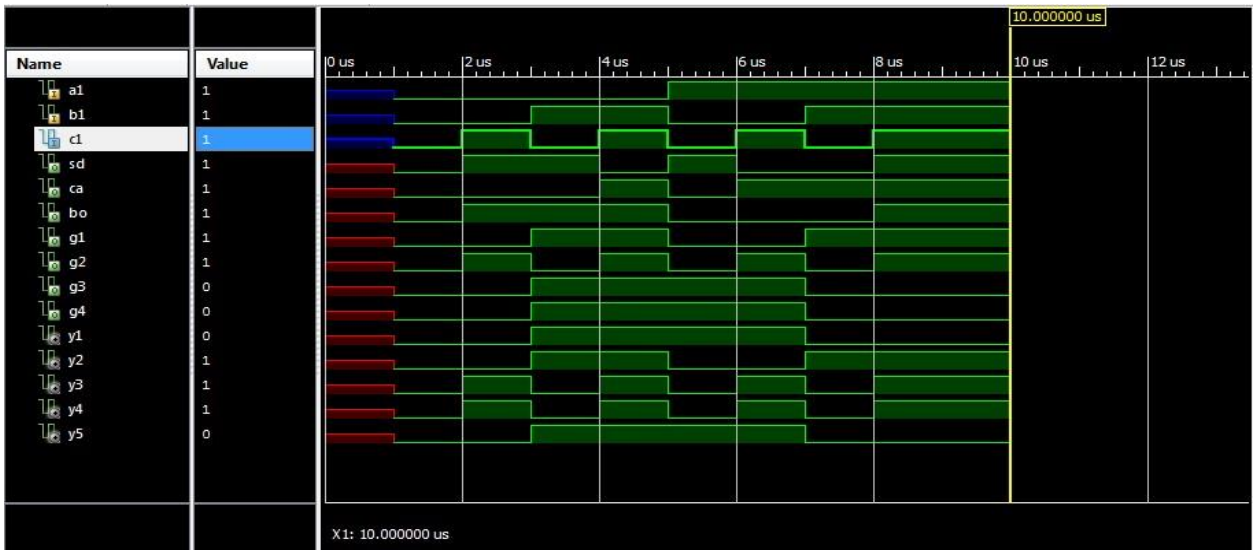
The last 15 years have witnessed the demise in the number of cell-based ASIC designs as a means for developing customized SoCs. Rising NREs, development times and risk have mostly restricted the use of cell-based ASICs to the highest volume applications; applications that can withstand the multi-million-dollar development costs associated with 1-2 design respins. Analysts estimate that the number of cell based ASIC design starts per year is now only between 2000-3000 compared to ~10,000 in the late 1990s. The FPGA has emerged as a technology that fills some of the gap left by cell-based ASICs. Yet even after 20+ years of existence and 40X more design starts per year than cell-based ASICs, the size of the FPGA market in dollar terms remains only a fraction that of cell-based ASICs. This suggests that there are many FPGA designs that never make it into production and that for the most part, the FPGA is still seen by many as a vehicle for prototyping or college education and has perhaps even succeeded in actually stifling industry innovation. This paper introduces a new technology, the second generation Structured ASIC, that is tipped to reenergize the path to innovation within the electronics industry. It brings together some of the key advantages of FPGA technology (i.e. fast turnaround, no mask charges, no minimum order quantity) and of cell-based ASIC (i.e. low unit cost and power) to deliver a new platform for SoC design. This document defines requirements for development of Application Specific Integrated Circuits (ASICs).

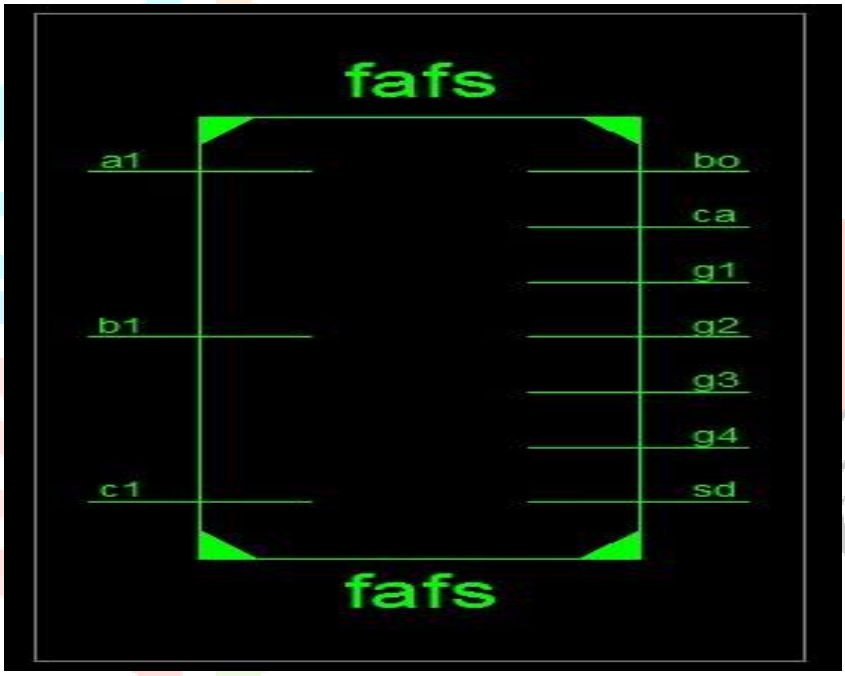
3.71 FIELD-PROGRAMMABLE GATE ARRAY (FPGA)

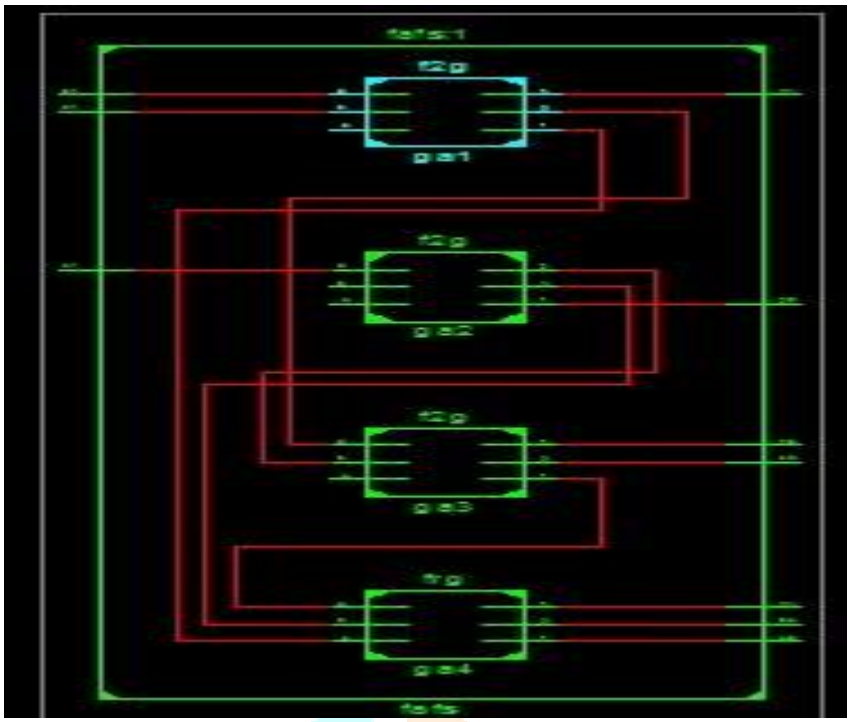
Prompted by the development of new types of sophisticated field-programmable devices (FPDs), the process of designing digital hardware has changed dramatically over the past few years. Unlike previous generations of technology, in which board-level designs included large numbers of SSI chips containing basic gates, virtually every digital design produced today consists mostly of high-density devices. This applies not only to custom devices like processors and memory, but also for logic circuits such as state machine controllers, counters, registers, and decoders. When such circuits are destined for high-volume systems they have been integrated into high-density gate arrays. However, gate array NRE costs often are too expensive and gate arrays take too long to manufacture to be viable for prototyping or other low-volume scenarios. For these reasons, most prototypes, and also many production designs are now built using FPDs. The most compelling advantages of FPDs are instant manufacturing turnaround, low start-up costs, low financial risk and (since programming is done by the end user) ease of design changes. The market for FPDs has grown dramatically over the past decade to the point where there is now a wide assortment of devices to choose from the most important terminology used below.

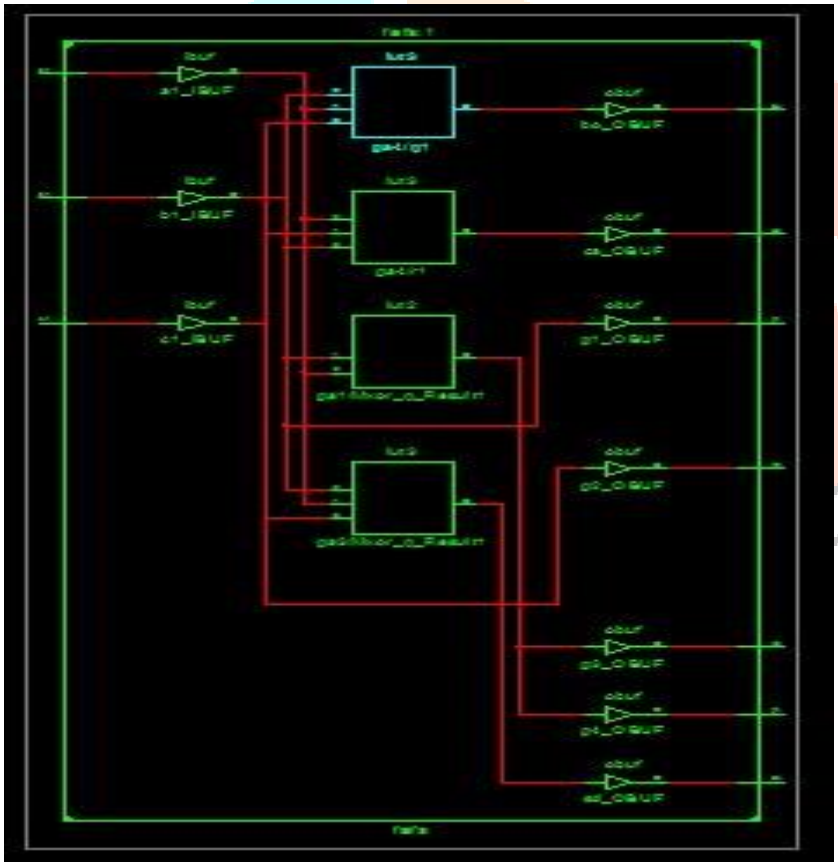
Field-Programmable Device (FPD) -A general term that refers to any type of integrated circuit used for implementing digital hardware, where the chip can be configured by the end user to realize different designs. Programming of such a device often involves placing the chip into a special programming unit, but some chips can also be configured “in-system”. Another name for FPDs is programmable logic devices (PLDs); although PLDs encompass the same types of chips as FPDs, we prefer the term FPD because historically the word PLD has referred to relatively simple types of devices. Programmable Logic Array (PLA)-A Programmable Logic Array (PLA) is a relatively small FPD that contains two levels of logic, an AND-plane and an OR-plane, where both levels are programmable (note: although PLA structures are sometimes embedded into full-custom chips, we refer here only to those PLAs that are provided as separate integrated circuits

RESULTS AND OUTPUT 4.1 Existing Design of optimal fault tolerant Full adder / Full subtractor

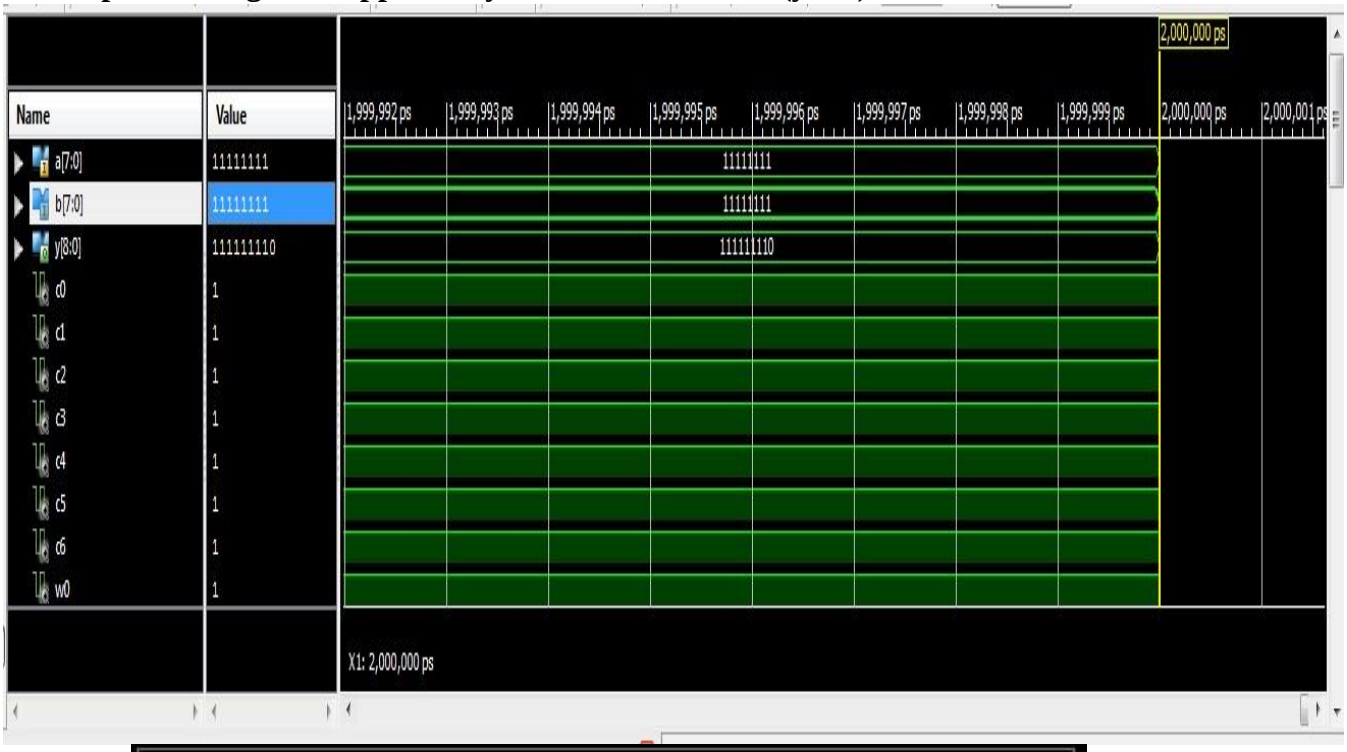


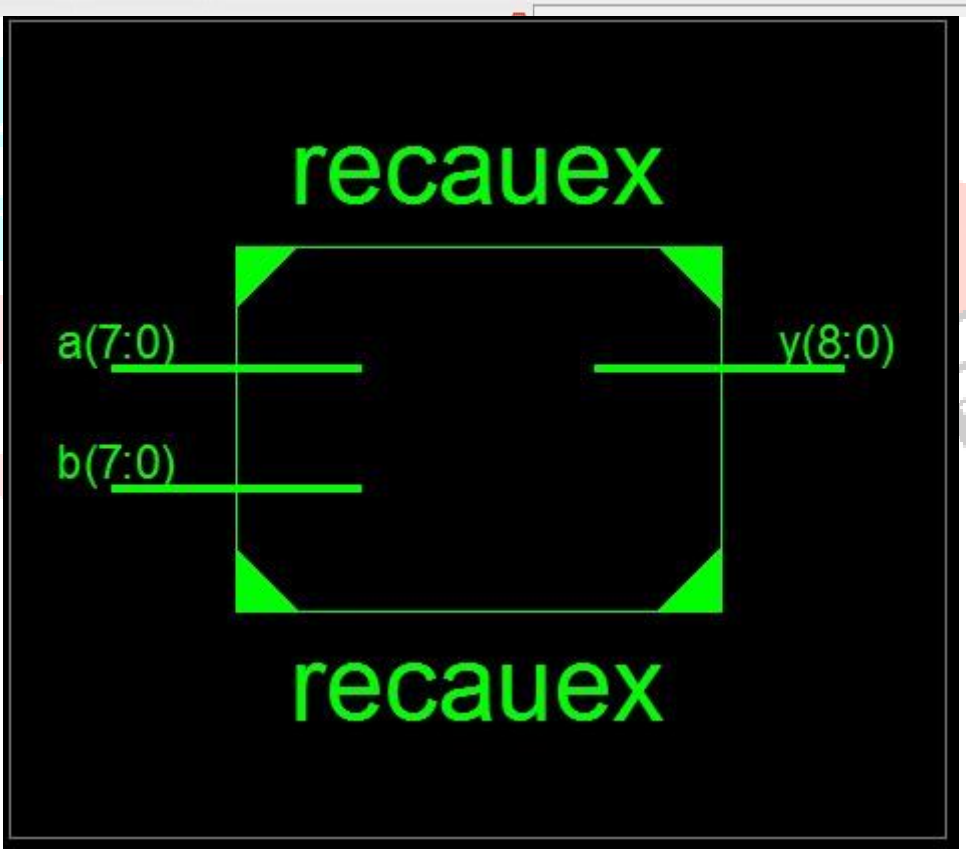


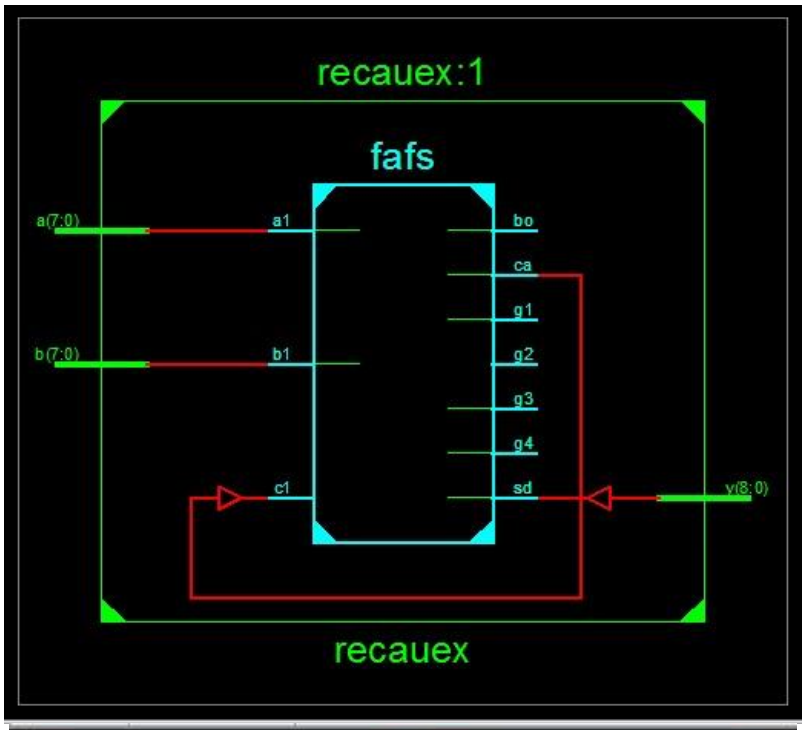


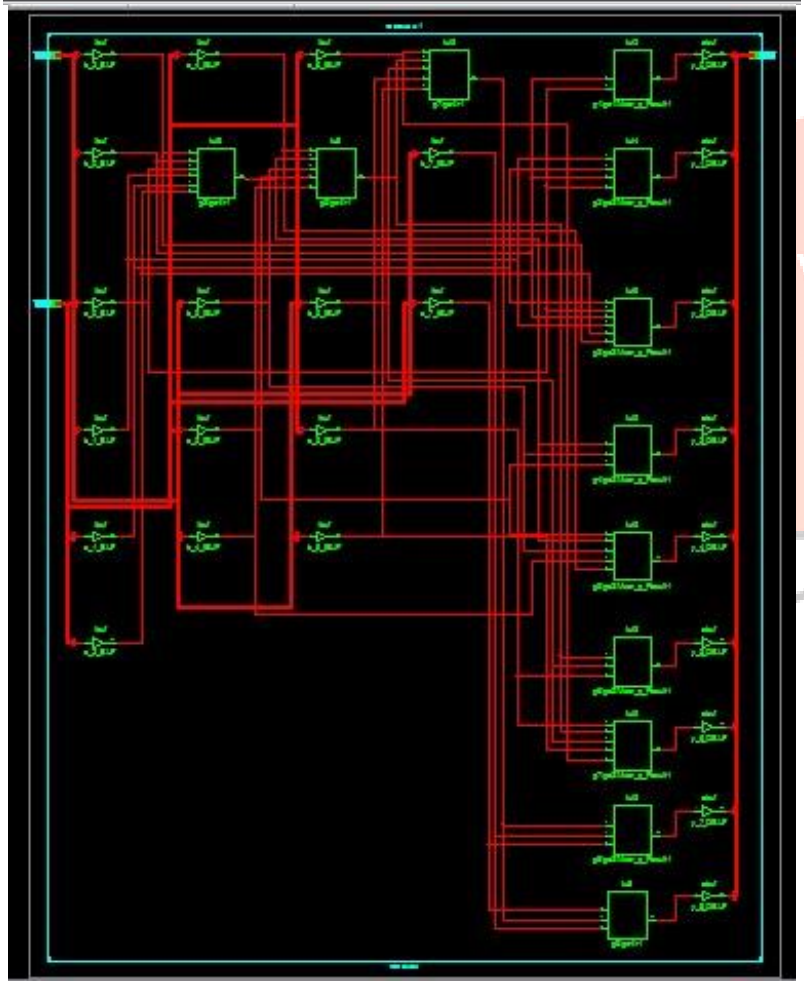


4:2 Proposed Design for ripple carry adder module recue(y,a,b);







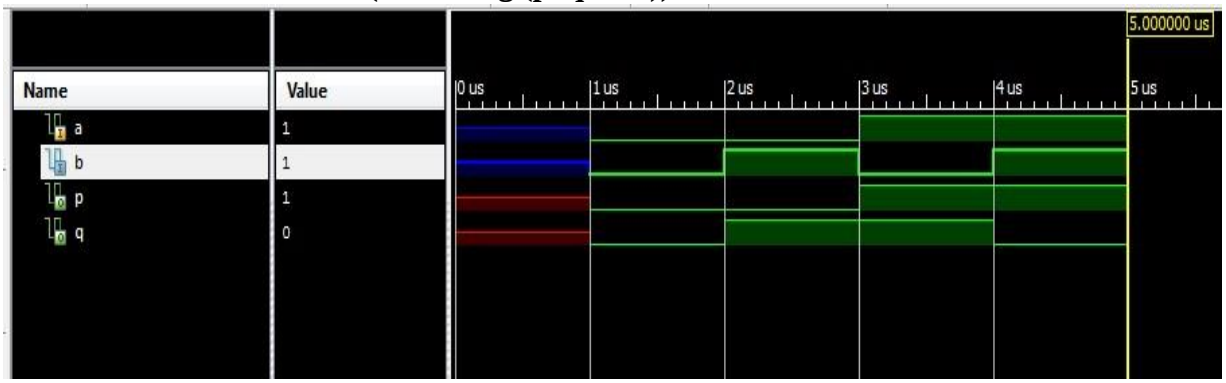


Total 5.855ns (3.182ns logic, 2.673ns route) (54.3% logic, 45.7% route)

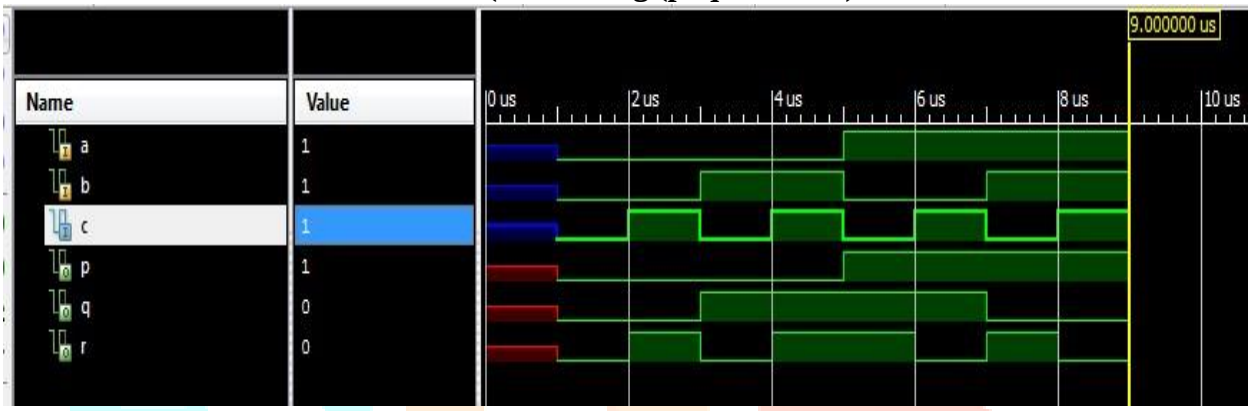
Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	12	12480	0%
Number of fully used LUT-FF pairs	0	12	0%
Number of bonded IOBs	25	172	14%

4.4 REVERSIBLE GATE OUTPUT

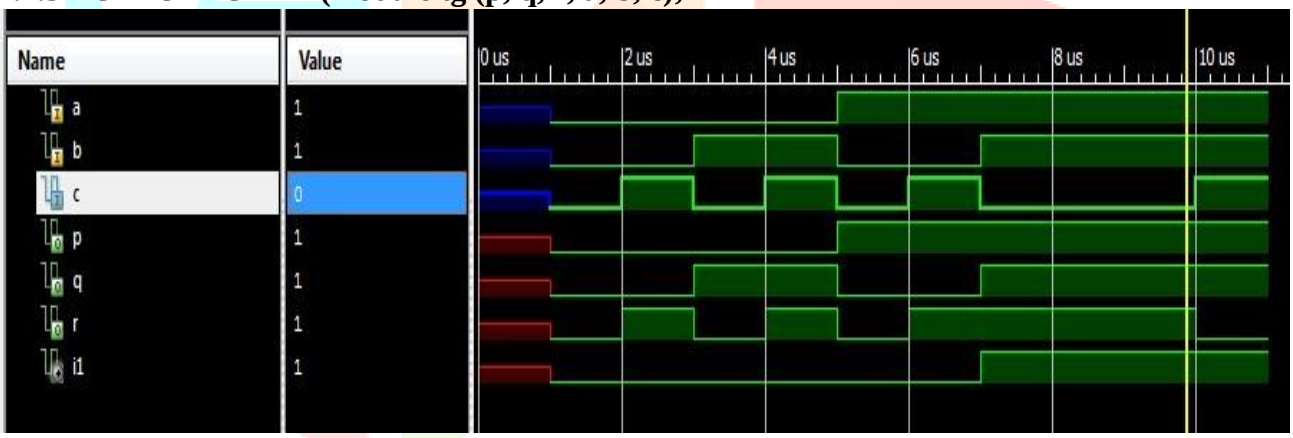
4.4.1 FEYNMAN GATE (module fg (p, q, a, b));



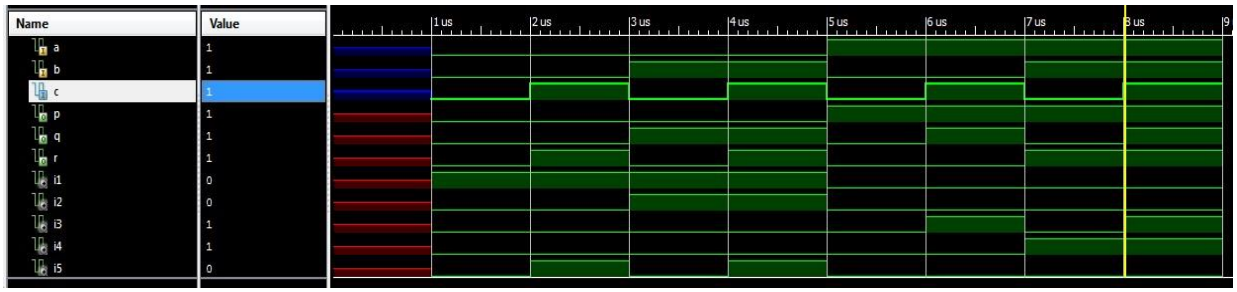
4.4.2 FEYNMAN DOUBLE GATE (module f2g (p, q, r, a, b, c);



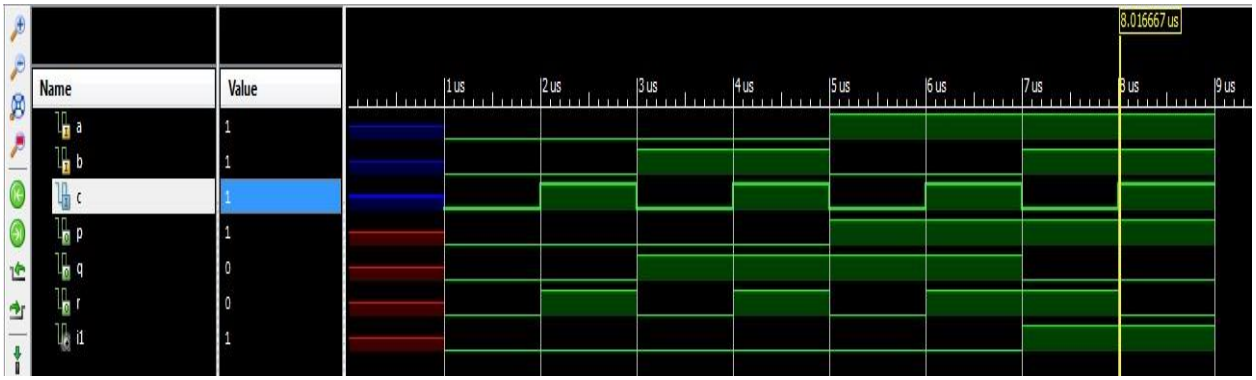
4.4.3 TOFFOLI GATE (module tg (p, q, r, a, b, c);



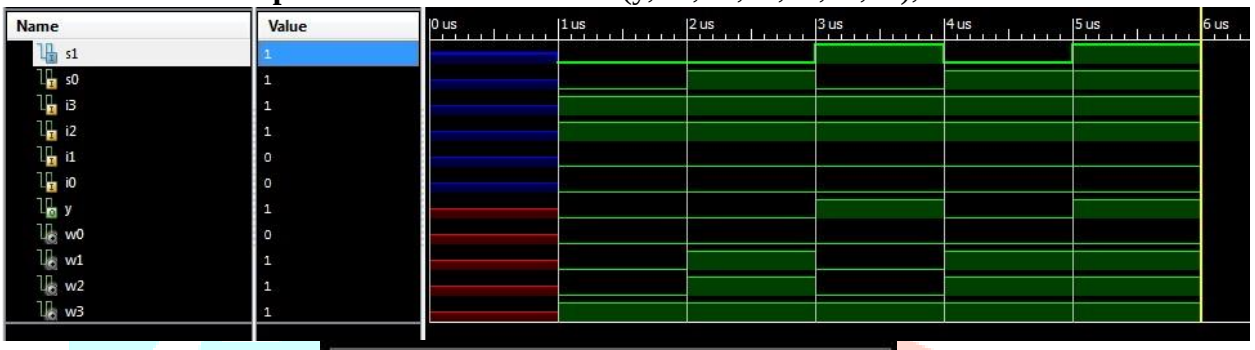
4.4.4 FREDKIN GATE (module frg (p, q, r, a, b, c))

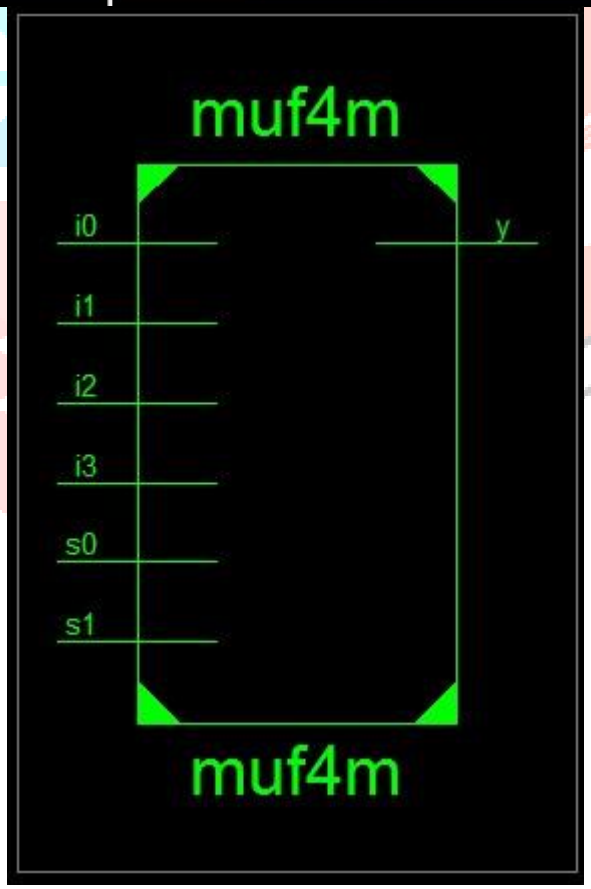


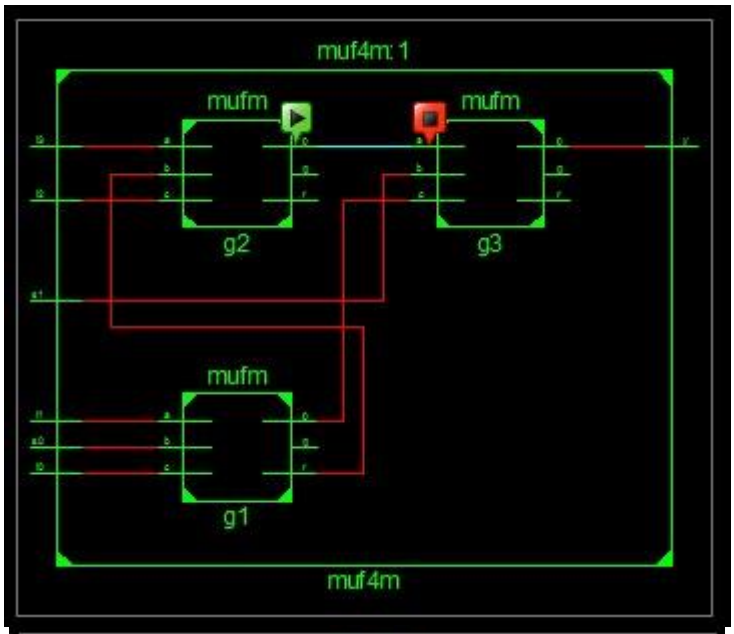
4.4.5 PERES GATE (module prg (p, q, r, a, b, c))

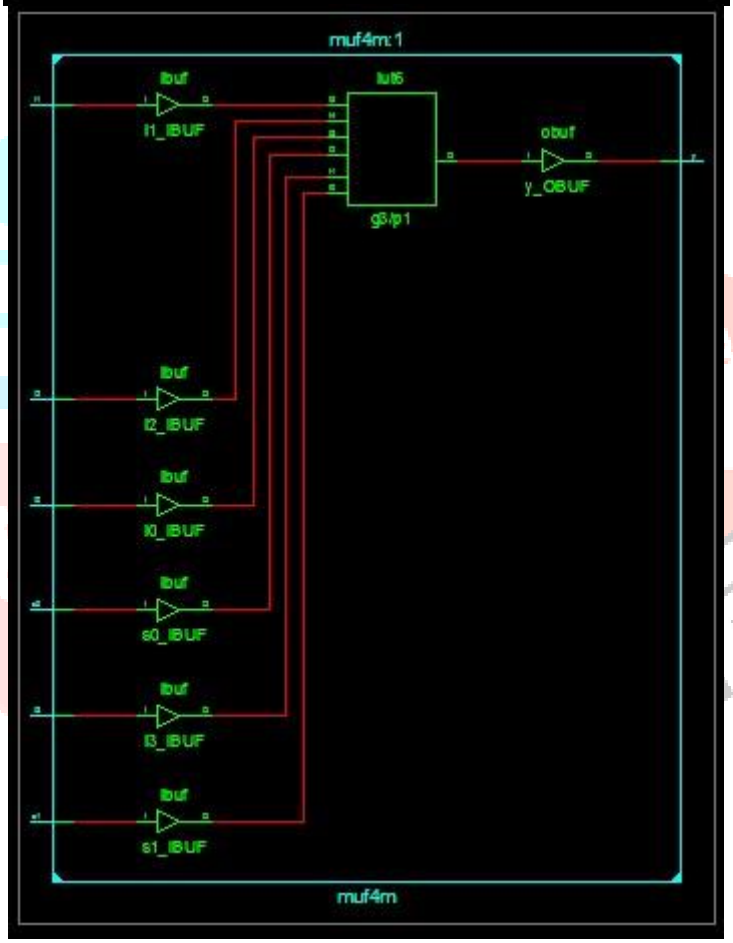


4.5 Reversible multiplexer 4:1 module muf4m (y, s1, s0, i3, i2, i1, i0);

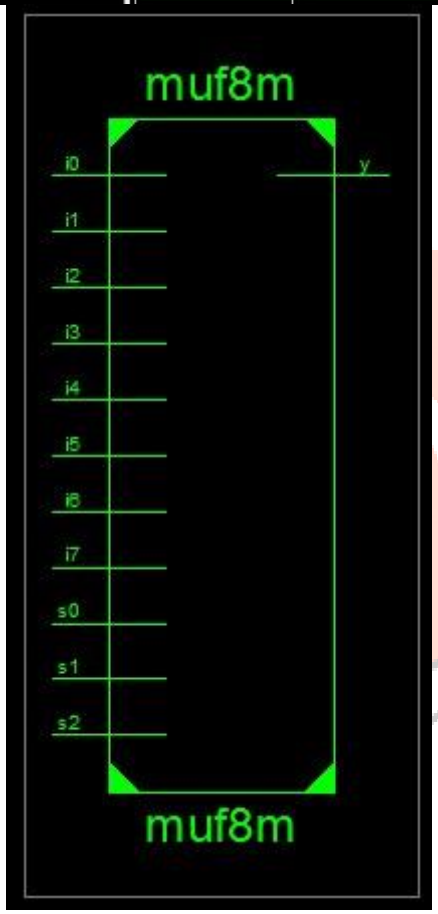


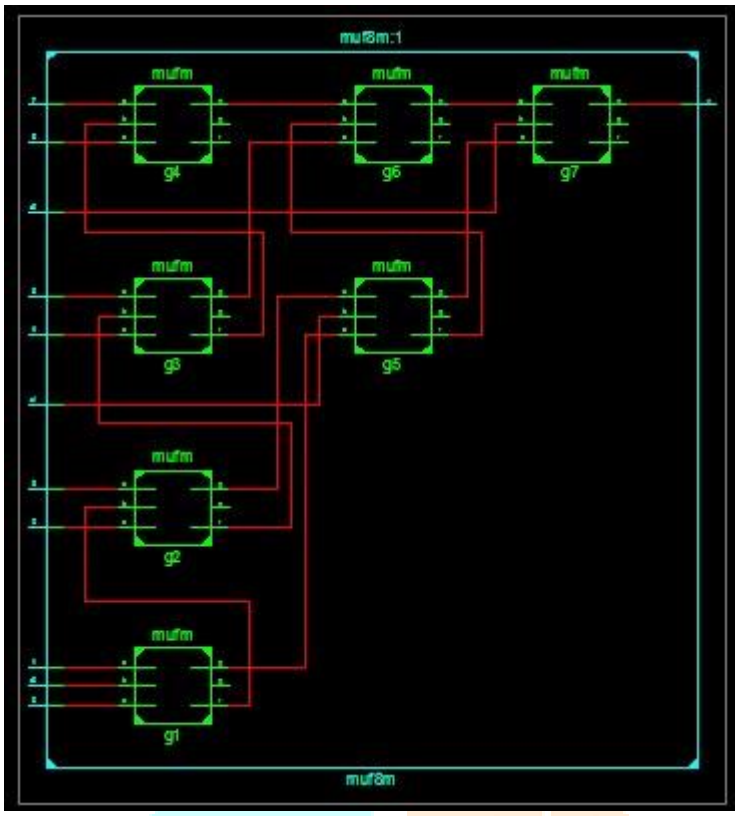



muf4m:1
mufm
mufm
g2
g3
mufm
g1
muf4m


muf4m:1
ibuf
I1_IBUF
lut6
g3/p1
obuf
y_OBUF
ibuf
I2_IBUF
ibuf
I0_IBUF
ibuf
s0_IBUF
ibuf
I3_IBUF
ibuf
s1_IBUF
muf4m

4.6 Reversible multiplexer 8:1





CONCLUSION

The structure is proposed with parity preserving gates which reduce testing hardware. Reversible logic concept work efficiently if number of garbage outputs, constant inputs and quantum cost is low. The power dissipation is zero if the reversible logic circuits are implemented with quantum gates. Our proposed reversible logic can provide very improved speed, low garbage output. The power dissipation is almost zero if the reversible logic circuits are implemented with quantum gates. If we do that then we can save power, money as well as nature.

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